MAXIM

1993 NEW RELEASES DATA BOOK Volume II

Featuring:

- ***Product Selection Tables/Trees***
- ***Data Sheets***
- ***Free Sample Request Cards***

Other Data Books Available from Maxim:

- ***Maxim 1992 New Releases Data Book, Vol. I***
- ***Maxim 1992 Applications & Product Highlights Book***
- ***Maxim 1993 Applications & Product Highlights Book***

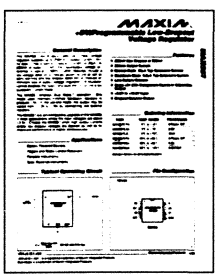
HOW TO USE THE 1993 NEW RELEASES DATA BOOK

Maxim's 1993 New Releases Data Book (Vol. II) brings together over 170 new devices from 11 product groups in a single, easy-to-use "Design-Guide" format. Each product group section contains: (1) Data sheets for all products in the group (2) Product tables and trees.

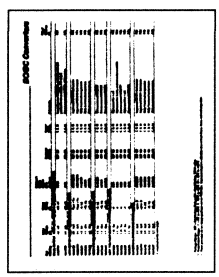
If, after reviewing this information, you need samples for further evaluation, all you need to do is fill out and send one of the sample request cards at the front of the book or call 1-800-998-8800 for prompt fulfillment.

There are several ways to locate a specific product or product group:

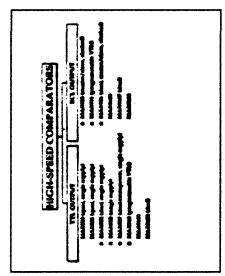
1	Multiplexers, Switches, Military
2	Interface Products
3	Op Amps
4	DC-DC Converters, Power Supplies
5	µP Supervisory
6	Analog Filters
7	A/D Converters
8	High Speed: Video, Comparators
9	D/A Converters
10	Display Drivers
11	Voltage References



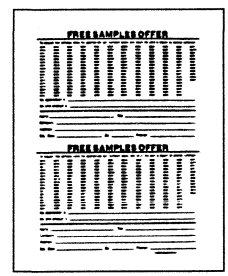
DATA SHEETS



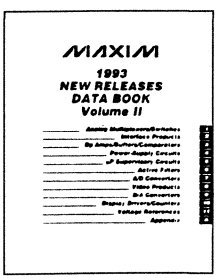
SELECTION TABLES WITH SPECS, COMMENTS, PRICING



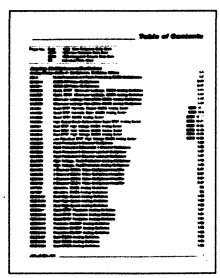
PRODUCT TREES



FREE SAMPLES



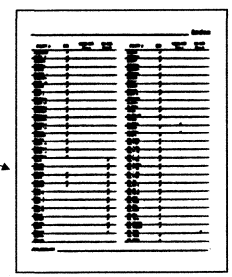
LOCATE PRODUCT SECTIONS BY TAB NUMBER



MAXIM PART NUMBER INDEX

*Data sheets included in this book indicated in **bold** face*

Cross reference to data sheets on Maxim parts not included in this book



ALPHA-NUMERIC PART INDEX CROSS REFERENCED TO OTHER MAXIM BOOKS

MAXIM

1993 NEW RELEASES DATA BOOK Volume II

Introduction

Maxim Integrated Products designs, develops, manufactures and markets a broad range of linear and mixed-signal integrated circuits (ICs) for use in a variety of electronic products. These ICs "connect" the real (analog) world to the digital world. They detect, measure, amplify and convert real-world signals, such as temperature, pressure or sound, into digital signals a computer can process. Over the past 9 years, Maxim has introduced over 500 analog ICs - more than any other company.

Maxim is committed to meeting the needs of the industry through aggressive product development and superior quality. Our product lines include: microprocessor supervisory circuits, data converters, references, RS-232 interface circuits, amplifiers, power-control circuits, timers and counters, display circuits, multiplexers, switches, voltage detectors and analog filters. Recognizing the growing demand for BiCMOS, the emerging technology of the future, Maxim has focused increasingly on CMOS- and BiCMOS-based products. These circuits are marketed worldwide, principally through distributors and independent sales representatives, and are available in several different packages and temperature ranges to meet varying customer requirements.

New Releases

During the past year, Maxim has released more than 70 new devices. These and other older but unique Maxim products are collected into this new data book. We hope this will give you quick access to "what is new and exciting from Maxim." Older products and some recently introduced second-source products do not appear in this book, but are identified in the Table of Contents and the Index. Free samples and data sheets for these products are available from your local sales representative, or directly from the factory by calling 1-800-998-8800.

Customer Service

This year, Maxim introduced a toll-free service number and a credit-card payment program. Ordering free samples and literature is easy – just call 1-800-998-8800. And, you can order evaluation kits or a small quantity of parts using your VISA or MasterCard.

Customer service representatives are available during normal business hours to provide you with information on orders placed directly with the factory or by any of our franchised distributors. Please see the Appendix for a list of domestic and international sales representatives and distributors.

Technical Support

The technical literature in this volume discusses the operation and applications of Maxim products as they apply to design problems. In addition to the individual data sheets in this book, Maxim offers a full-line Integrated Circuits Data Book, a High-Reliability Products Data Book, an Applications and Product Highlights Book, and a free subscription to the Maxim Engineering Journal - a quarterly magazine covering the application of Maxim analog ICs. For on-line technical support, you can talk with a senior applications engineer at (408) 737- 7600 extension 4000 or FAX in your questions at (408) 736-1831.

Reliability

Maxim's mission is to provide reliable, innovative analog ICs that solve customer problems. Our programs offering complete lot traceability, life test, and humidity life qualification are unique in the industry.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

Analog Multiplexers/Switches

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

Interface Products

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

Op Amps/Buffers/Comparators

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

Power-Supply Circuits

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

µP Supervisory Circuits

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

* Advance Information – first page of data sheet in preparation. **Partial data sheet.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

Video Products

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

D/A Converters

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

Display Drivers/Timers/Counters

Voltage References

* Advance Information – first page of data sheet in preparation.

Table of Contents

Edition Key: **Bold - 1993 New Releases Data Book, Vol. II**
92NR - 1992 New Releases Data Book, Vol. I
DS - Individual Data Sheet

* Advance Information – first page of data sheet in preparation.

MAXIM

Analog Multiplexers/Switches

1

* Advance Information – first page of data sheet in preparation.

Part Number	Function	Plug-In Replacement for	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current I+/I- (mA max)	Price† 1000-up ($)
MAX326	4 SPST NC	DG201A/211	2500	0.01	1000	500	0.8/2.4	0.25/0.1	3.63
MAX327	4 SPST NO	DG202/212	2500	0.01	1000	500	0.8/2.4	0.25/0.1	3.63
MAX331	4 SPST NC	DG201A/211	175	1	600	450	0.8/2.4	0.01/0.01	6.73
MAX332	4 SPST NO	DG202/212	175	1	600	450	0.8/2.4	0.01/0.01	6.73
MAX333	4 SPDT	DG211& DG212 pair	175	5	1000	500	0.8/2.4	0.25/0.25	4.47
MAX334	4 SPST NC	DG201A/211/271	50	1	100	50	0.8/3.0	4.5/3.5	3.20
DG401	2 SPST NO	DG401, IH5041/5141	35	0.25	150	100	0.8/2.4	0.001/0.001	††
DG403	2 SPDT	DG403, IH5043/5143	35	0.25	150	100	0.8/2.4	0.001/0.001	††
DG405	2 DPST NO	DG405, IH5045/5145	35	0.25	150	100	0.8/2.4	0.001/0.001	††
DG411	4 SPST NC	DG201A-2/211-12/411	35	0.25	175	145	0.8/2.4	0.001/0.001	2.96
DG412	4 SPST NO	DG201A-2/211-12/412	35	0.25	175	145	0.8/2.4	0.001/0.001	2.96
DG413	4 SPST	DG413	35	0.25	175	145	0.8/2.4	0.001/0.001	2.96
DG417	SPST NC	DG417	35	0.25	175	145	0.8/2.4	0.001/0.001	††
DG418	SPST NO	DG418	35	0.25	175	145	0.8/2.4	0.001/0.001	††
DG419	SPDT	DG419	35	0.25	175	145	0.8/2.4	0.001/0.001	††
DG421	2SPST	DG421	35	0.25	250	200	0.8/2.4	0.001/0.001	††
DG423	2SPDT	DG423	35	0.25	250	200	0.8/2.4	0.001/0.001	††
DG425	2DPST	DG425	35	0.25	250	200	0.8/2.4	0.001/0.001	††
DG441	4 SPST NC	DG201A-202/441	85	0.5	250	120	0.8/2.4	0.1/0.001	2.48
DG442	4 SPST NO	DG201A-202/442	85	0.5	250	120	0.8/2.4	0.1/0.001	2.63
DG444	4 SPST NC	DG211-212/444	85	0.5	250	120	0.8/2.4	0.001/0.001	1.19
DG445	4 SPST NO	DG211-212/445	85	0.5	250	120	0.8/2.4	0.001/0.001	1.44
DG200A	2 SPST NC	DG200A	70	2	1000	500	0.8/2.4	0.3/0.01	1.78
DG201A	4 SPST NC	DG201A	175	1	600	450	0.8/2.4	0.1/0.1	1.97
DG202	4 SPST NO	DG202	175	1	600	450	0.8/2.4	0.1/0.1	2.21
DG211	4 SPST NC	DG211	175	5	1000	500	0.8/2.4	0.1/0.1	1.47
DG212	4 SPST NO	DG212	175	5	1000	500	0.8/2.4	0.1/0.1	1.47
DG300A	2 SPST NC	DG300A	50	1	300	250	0.8/4.0	0.5/0.1	2.15
DG301A	SPDT	DG301A	50	1	300	250	0.8/4.0	0.1/0.1	2.15
DG302A	2 DPST NC	DG302A	50	1	300	250	0.8/4.0	0.1/0.1	2.78
DG303A	2 SPDT	DG303A	50	1	300	250	0.8/4.0	0.1/0.1	2.78

–Continued on the next page–

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.

Analog Switches (continued)

Part Number	Function	Plug-In Replacement for	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}$ (ns max)	$t_{(OFF)}$ (ns max)	V_{IL}/V_{IH} (V)	Supply Current I+/I- (mA max)	Price† 1000-up ($)
DG304A	2 SPST NC	DG304A	50	1	250	150	3.5/11.0	0.1/0.1	2.42
DG305A	SPDT	DG305A	50	1	250	150	3.5/11.0	0.1/0.1	2.55
DG306A	2 DPST NC	DG306A	50	1	250	150	3.5/11.0	0.1/0.1	4.06
DG307A	2 SPDT	DG307A	50	1	250	150	3.5/11.0	0.1/0.1	2.78
DG308A	SPST NO	DG308A	100	1	200	150	3.1/11.0	0.1/0.1	2.16
DG309	SPST NC	DG309	100	1	200	150	3.5/11.0	0.1/0.1	2.16
HI201	4 SPST NC	DG201A, HI201	70	5	400	300	0.8/2.4	0.3/0.1	2.00
DG381A	2 SPST NO	DG381A	50	1	300	250	0.8/4.0	0.1/0.1	3.24
DG384A	2 DPDT NC	DG384A	50	1	300	250	0.8/4.0	0.1/0.1	4.06
DG387A	SPDT	DG387A	50	1	300	250	0.8/4.0	0.1/0.1	3.24
DG390A	2 SPDT	DG390A	50	1	300	250	0.8/4.0	0.1/0.1	3.26
IH5041	2 SPST NC	IH5041	75	1	400	200	0.8/2.4	0.001/0.001	1.84
IH5043	2 SPDT	IH5043	75	1	400	200	0.8/2.4	0.001/0.001	2.36
IH5045	2 DPST NC	IH5045	75	1	400	200	0.8/2.4	0.001/0.001	2.44
IH5047	2 DPST NC	IH5045	75	1	400	200	0.8/2.4	0.001/0.001	2.44

Analog Multiplexers

Part Number	Function	Plug-In Replacement for	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}/t_{(OFF)}$ (µs max)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
MAX328	1-of-8	DG508	2500	0.02	1	±15	Ultra-low leakage	4.72
MAX329	2-of-8	DG509	2500	0.02	1	±15	Ultra-low leakage	4.72
MAX358	1-of-8	DG508, HI508A	1500	1.0	0.5	-12.5 to +13.5	Fault protected to ±35V	3.75
MAX359	2-of-8	DG509, HI509A	1500	1.0	0.5	-12.5 to +13.5	Fault protected to ±35V	3.75
MAX368	1-of-8	DG528	1500	2	1.5/1.0	-12.5 to +13.5	Fault protected with latches to ±35V	4.75
MAX369	2-of-8	DG529	1500	1.0	1.5/1.0	-12.5 to +13.5	Fault protected with latches to ±35V	4.75
MAX378	1-of-8	DG508, HI508A	3000	1.0	0.75/0.5	-12.5 to +13.5	Fault protected to ±75V	5.50
MAX379	2-of-8	DG509, HI509A	3000	1.0	0.75/0.5	-12.5 to +13.5	Fault protected to ±75V	5.50
MAX388	1-of-8	DG528, MAX368	3000	1.0	1	-12.5 to +13.5	Fault protected with latches to ±100V	6.00
MAX389	2-of-8	DG529, MAX369	3000	1.0	1	-12.5 to +13.5	Fault protected with latches to ±100V	6.00

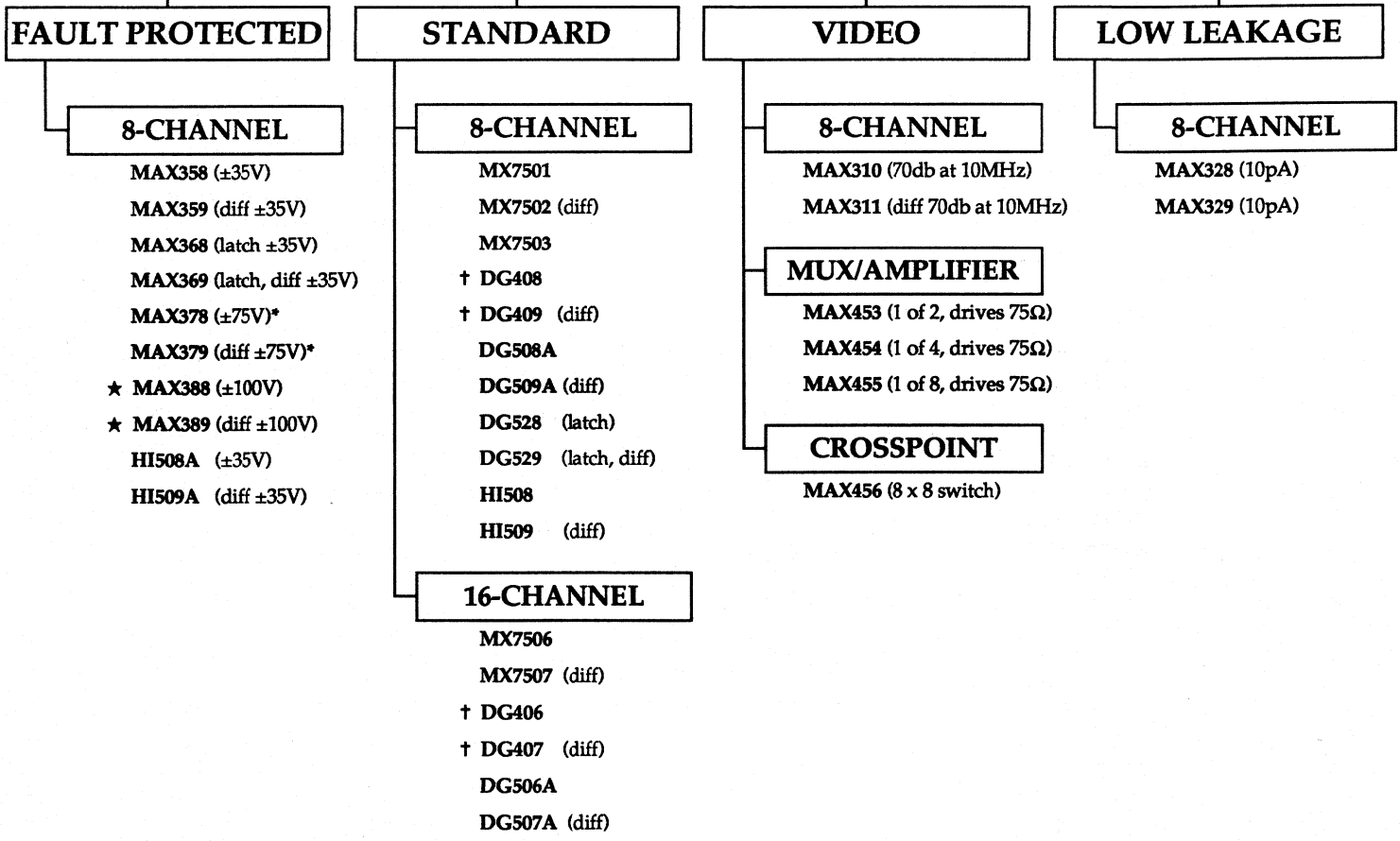
–Continued on the next page–

† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.

Part Number	Function	Plug-In Replacement for	$r_{DS(ON)}$ (Ω max)	$I_{D(OFF)}$ (nA max)	$t_{(ON)}/t_{(OFF)}$ (µs max)	Analog-Signal Voltage Range (V)	Features	Price† 1000-up ($)
MX7501	1-of-8	AD7501	300	5	1.5/1.0	±15	Industry standard	5.58
MX7502	2-of-8	AD7502	300	3	1.5/1.0	±15	Industry standard	5.58
MX7503	1-of-8	AD7503	300	5	1.5/1.0	±15	Industry standard	5.58
MX7506	1-of-16	AD7506	400	5	1.5/1.0	±15	Industry standard	10.25
MX7507	2-of-16	AD7507	400	5	1.5/1.0	±15	Industry standard	10.25
DG406	1-of-16	DG406/506A	100	2	0.2/0.15	±15	Industry standard	††
DG407	2-of-16	DG407/507A	100	2	0.2/0.15	±15	Industry standard	††
DG408	1-of-8	DG408/508A	100	1	0.225/0.150	±15	Industry standard	††
DG409	2-of-8	DG409/509A	100	1	0.225/0.150	±15	Industry standard	††
DG506A	1-of-16	DG506A, HI506	400	5	1.0/0.4 (typ)	±15	Industry standard	4.79
DG507A	2-of-16	DG507A, HI507	400	5	1.0/0.4 (typ)	±15	Industry standard	4.79
DG508A	1-of-8	DG508A, HI508	300	2	1.0/1.7	±15	Industry standard	2.09
DG509A	2-of-8	DG509A, HI509	300	2	1.0/1.7	±15	Industry standard	2.09
DG528	1-of-8	DG528	400	10	1.5	±15	Industry standard	3.19
DG529	2-of-8	DG529	400	10	1.5	±15	Industry standard	3.19
HI508A	1-of-8	HI508A	1500	2	0.5	-12.5 to +13.5	Overvoltage	5.88
HI509A	2-of-8	HI509A	1500	2	0.5	-12.5 to +13.5	Overvoltage	5.88
IH5108	Use MAX358 (pin for pin compatible upgrade)							
IH5208	Use MAX359 (pin for pin compatible upgrade)							
IH6108	Use DG508A (pin for pin compatible upgrade)							
IH6208	Use DG509A (pin for pin compatible upgrade)							
IH6116	Use DG506A (pin for pin compatible upgrade)							
IH6216	Use DG507A (pin for pin compatible upgrade)							
HI506	Use DG506A (pin for pin compatible upgrade)							
HI507	Use DG507A (pin for pin compatible upgrade)							
HI508	Use DG508A (pin for pin compatible upgrade)							
HI509	Use DG509A (pin for pin compatible upgrade)							

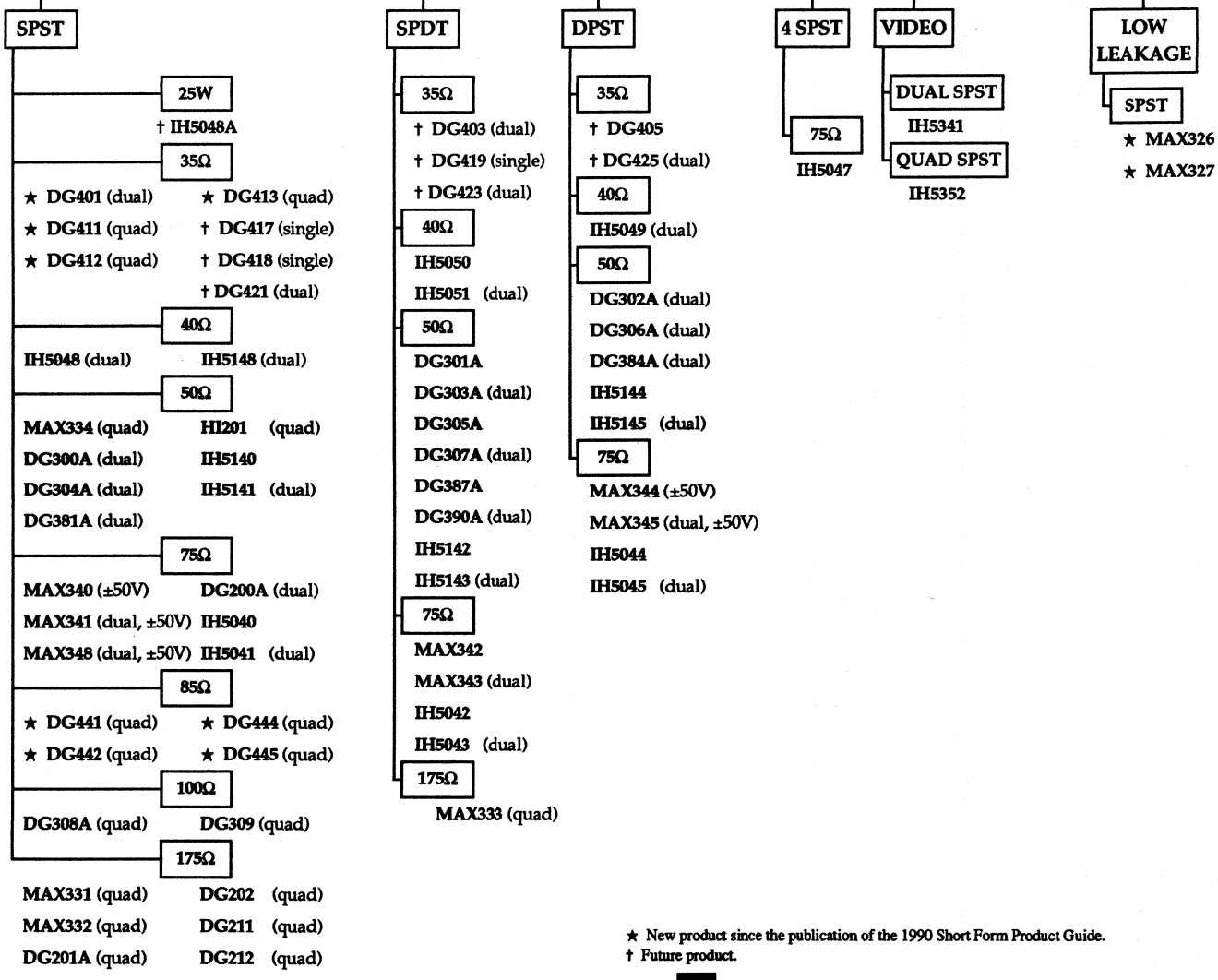
† Prices provided are for design guidance only and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.

ANALOG MULTIPLEXERS



★ New product since the publication of the 1990 Short Form Product Guide.
† Future product.
* Withstands quoted input or output voltage indefinitely with/without supply voltage present.

ANALOG SWITCHES



★ New product since the publication of the 1990 Short Form Product Guide.
† Future product.

19-0014; Rev 0; 6/92

MAXIM

High-Voltage, Fault-Protected Analog Multiplexers

General Description

The MAX388 8-channel single-ended (1-of-8) and the MAX389 4-channel differential (2-of-8) multiplexers (muxes) with internal data latches use a high-voltage series N-channel, P-channel, N-channel structure that significantly improves fault protection over previous devices. If power is removed with input voltages still applied, all channels turn off, allowing only a few nanoamperes of input leakage current. This protects the mux and output circuitry, as well as the signal sources connected to the channel inputs.

When an overvoltage signal up to ±100V (typically ±110V) is applied to an analog input or output, the channel turns off. To further protect output circuitry from on-channel overvoltage, outputs are clamped to less than the power-supply voltage. Since there is no increase in supply current during fault conditions, power dissipation does not increase. The MAX388/MAX389 withstand full overvoltage on any combination of channels, including all channels simultaneously.

All channel selection and control inputs are TTL and CMOS compatible. And, break-before-make switch operation is guaranteed.

Applications

Data-Acquisition Systems

Industrial Process Control Systems

Avionics Test Equipment

Signal Routing Between Systems

Computer-Controlled Analog Data Logging

Features

- ♦ **Fault and Overvoltage Protection**
- ♦ **Fail-Safe with Power Loss (No Latchup)**
- ♦ **Break-Before-Make Switching**
- ♦ **All Channels Off when Power Off**
- ♦ **Internal Data Latches**
- ♦ **TTL and CMOS Compatible**
- ♦ **Operates from ±4.5V to ±18V Supplies**
- ♦ **On-Channels Turn Off during Overvoltage**
- ♦ **Nanoamperes Leakage in Overvoltage**

Ordering Information

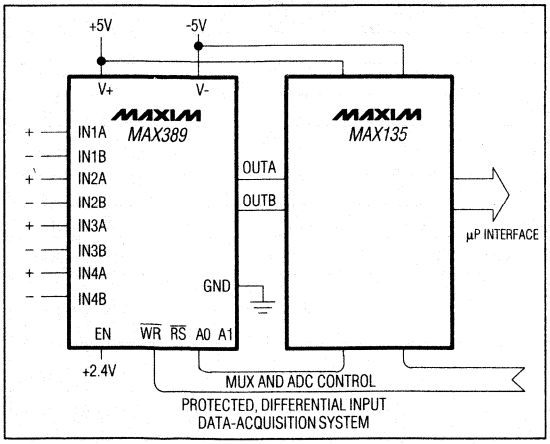
PART	TEMP. RANGE	PIN-PACKAGE
MAX388CPN	0°C to +70°C	18 Plastic DIP
MAX388CJN	0°C to +70°C	18 CERDIP
MAX388C/D	0°C to +70°C	Dice*
MAX388EPN	-40°C to +85°C	18 Plastic DIP
MAX388EJN	-40°C to +85°C	18 CERDIP
MAX388MJN	-55°C to +125°C	18 CERDIP**

Ordering Information continued on last page.

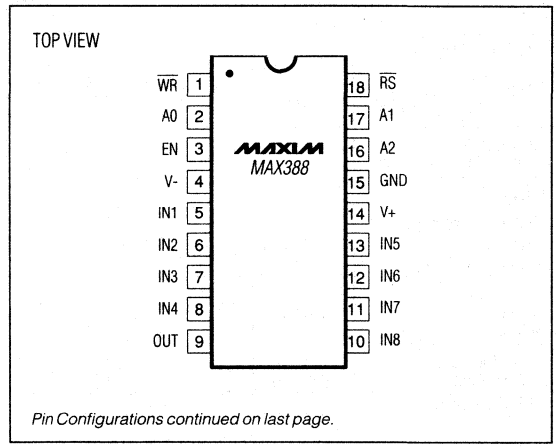
* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configurations



Pin Configurations continued on last page.

High-Voltage, Fault-Protected Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

V+ to V- 44V
V+ to GND 22V
V- to GND ..... -22V
EN, $\overline{WR}$, $\overline{RS}$, A0-A2 ..... V+ + 4V to V- - 4V
Analog Input with V+ = 15V, V- = -15V ..... ±100V
Analog Input with V+ = V- = 0V ..... ±115V
Continuous Current, IN or OUT 20mA
Peak Current, IN or OUT (Note 1) 40mA

Continuous Power Dissipation
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
CERDIP (derate 10.53mW/°C above +70°C) 842mW
Operating Temperature Ranges:
MAX38_C _ _ ..... 0°C to +70°C
MAX38_E _ _ ..... -40°C to +85°C
MAX38_MJN ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Pulsed at 1ms, 10% maximum duty cycle.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, GND = $\overline{WR}$ = 0V, $\overline{RS}$ = +2.4V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			C, E SUFFIXES MIN	C, E SUFFIXES TYP	C, E SUFFIXES MAX	M SUFFIX MIN	M SUFFIX TYP	M SUFFIX MAX	UNITS
Analog Signal Range	V_{ANALOG}	(Note 4)			-15		15	-15		15	V
Drain-Source On Resistance	$r_{DS(ON)}$	V_D = ±10V, V_{AL} = 0.8V, I_S = 100µA, V_{AH} = 2.4V				2.0	3.0		2.0	3.0	kW
				T_{MAX}		3.0	4.0		3.0	4.0	
Greatest Change in $r_{DS(ON)}$ Between Channels	$\Delta r_{DS(ON)}$	-10V < VS < 10V				10			10		%
Source-Off Leakage Current (Note 2)	$I_{IN(OFF)}$	V_{EN} = 0.8V, V_{IN} = ±10V, V_{OUT} = ±10V			-1.00	0.03	1.00	-0.50	0.03	0.50	nA
				T_{MAX}	-50		50	-50		50	
Drain-Off Leakage Current (Note 2)	$I_{OUT(OFF)}$	V_{EN} = 0.8V, V_{IN} = ±10V, V_{OUT} = ∓10V	MAX388		-2.0	0.1	2.0	-1.0	0.1	1.0	nA
				T_{MAX}	-200		200	-200		200	
			MAX389		-2.0		2.0	-1.0		1.0	
				T_{MAX}	-100		100	-100		100	
Drain-On Leakage Current (Note 2)	$I_{OUT(ON)}$	V_{EN} = V_{AH} = 2.4V, V_{OUT} = V_{IN} = ±10V, V_{AL} = 0.8V	MAX388		-5.0		5.0	-2.0		2.0	nA
				T_{MAX}	-200		200	-200		200	
			MAX389		-5.0		5.0	-2.0		2.0	
				T_{MAX}	-100		100	-100		100	
LOGIC INPUT											
Logic Input Current (Input Voltage High)	I_{AH}	V_A = 2.4V (Note 3)			-1		1	-1		1	µA
		V_A = 14V (Note 3)			-1		1	-1		1	
Logic Input Current (Input Voltage Low)	I_{AL}	V_{EN} = 0V or 2.4V, V_A = $\overline{RS}$ = $\overline{WR}$ = 0V			-1		1	-1		1	µA
FAULT											
Output Leakage Current with Overvoltage	$I_{OUT(OFF)}$	V_{OUT} = 0V, V_{IN} = ±60V, (Note 5)			-0.05		0.05	-0.02		0.02	µA
				T_{MAX}			20			10	µA
Input Leakage Current with Overvoltage	$I_{IN(OFF)}$	V_{IN} = ±60V, V_{OUT} = ±10V, (Note 5)					40			25	µA
Input Leakage Current with Power Supplies Off	$I_{IN(OFF)}$	V_{IN} = ±100V, V_{EN} = V_{OUT} = 0V, A0 = A1 = A2 = 0V or 5V					20			10	mA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, GND = $\overline{WR}$ = 0V, $\overline{RS}$ = +2.4V, T_A = +25°C, unless otherwise noted.)

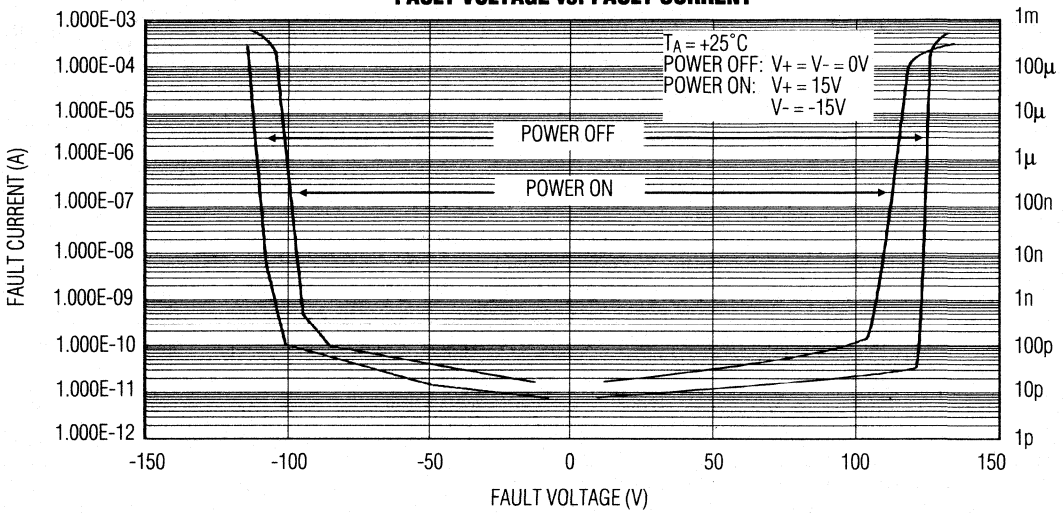
PARAMETER	SYMBOL	CONDITIONS		C, E SUFFIXES MIN	C, E SUFFIXES TYP	C, E SUFFIXES MAX	M SUFFIX MIN	M SUFFIX TYP	M SUFFIX MAX	UNITS
DYNAMIC										
Multiplexer Switching Time	t_{TRANS}	Figure 2			0.5	1.0		0.5	1.0	µs
Break-Before-Make Interval	t_{OPEN}	Figure 3			0.2			0.2		µs
Enable or Write Turn-On Time	$t_{ON(EN)}$ $t_{ON(\overline{WR})}$	Figures 4 and 5			1.0	1.5		1.0	1.5	µs
Enable or Write Turn-Off Time	$t_{OFF(EN)}$ $t_{OFF(\overline{WR})}$	Figures 4 and 6			0.4	1.0		0.4	1.0	µs
Charge Injection	Q	Figure 7, Tables 1a and 1b			55			55		pC
Off Isolation	OIRR	V_{EN} = 0V, R_L = 1kΩ, C_L = 15pF, V_{IN} = $7V_{RMS}$, f = 100kHz			68			68		dB
Logic Input Capacitance with Switch Off	C_{IN}	f = 1MHz			5			5		pF
Input Capacitance with Switch Off	$C_{S(OFF)}$	VEN = 0V, V_{IN} = 0V, f = 140kHz			5			5		pF
Output Capacitance with Switch Off	$C_{D(OFF)}$	V_{EN} = 0V, f = 140kHz, V_{OUT} = 0V	MAX388		25			25		pF
			MAX389		12			12		
$\overline{WR}$ Pulse Width	t_{WW}	Figure 1		300			300			ns
Ax, EN Data Valid to $\overline{WR}$	t_{DW}	Setup time, Figure 1		210			180			ns
Ax, EN Data Valid after $\overline{WR}$	t_{WD}	Hold time, Figure 1		30			10	0		ns
$\overline{RS}$ Pulse Width	t_{RS}	V_{IN} = 5V, Figure 1		500			300			ns
SUPPLY										
Supply Range		(Note 6)		±4.5		±18.0	±4.5		±18.0	V
Positive Supply Current	I+	V_{EN} = 2.4V, V_A = 0V or 5V			1.0	2.0		1.0	2.0	mA
Negative Supply Current	I-				1.2	2.5		1.2	2.5	

Note 2: Leakage currents at T_{MIN} guaranteed, but not tested.
Note 3: Digital input leakage is primarily due to the clamp diodes. Typical leackage is less than 1nA at +25°C.
Note 4: When the analog signal exceeds +13.5V or -12V, the blocking action of Maxim's gate structure operates. Only leakage currents flow, and the channel on resistance rises.
Note 5: The value shown is the steady-state value. The transient leakage is typically 50µA. See *Detailed Description.*
Note 6: Electrical characteristics such as $r_{DS(ON)}$ will change when power supplies other than ±15V are used.

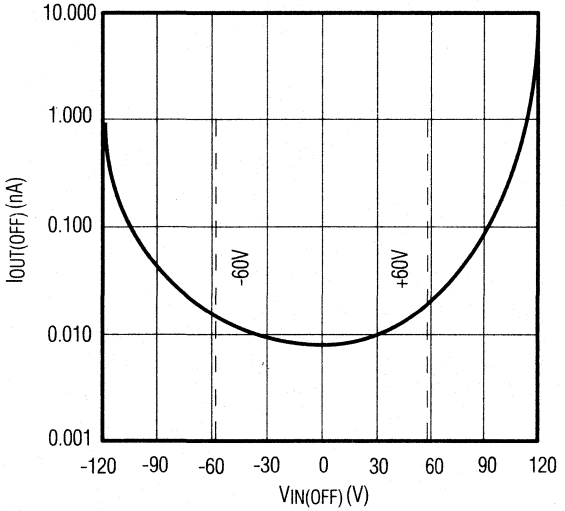
High-Voltage, Fault-Protected Analog Multiplexers

Typical Operating Characteristics

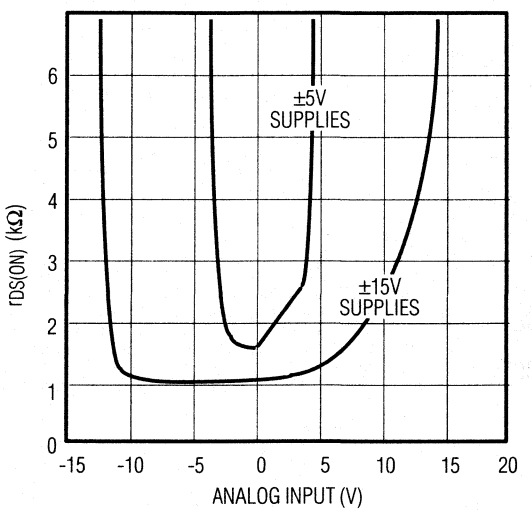
FAULT VOLTAGE vs. FAULT CURRENT



OUTPUT LEAKAGE vs. OFF-CHANNEL OVERVOLTAGE WITH ±15V SUPPLIES



$r_{DS(ON)}$ vs. ANALOG INPUT VOLTAGE



Detailed Description

Fault-Protection Circuitry

The MAX388/MAX389 are fully fault-protected for continuous input voltages up to ±100V, whether or not the V+ and V- power supplies are present (±115V with power off). These muxes use a "series FET" switching scheme that protects the mux output from overvoltage while limiting the input current to sub-microamp levels. Figures 7 and 8 show input leakage-current levels during overvoltage (Figure 7) and with power off (Figure 8).

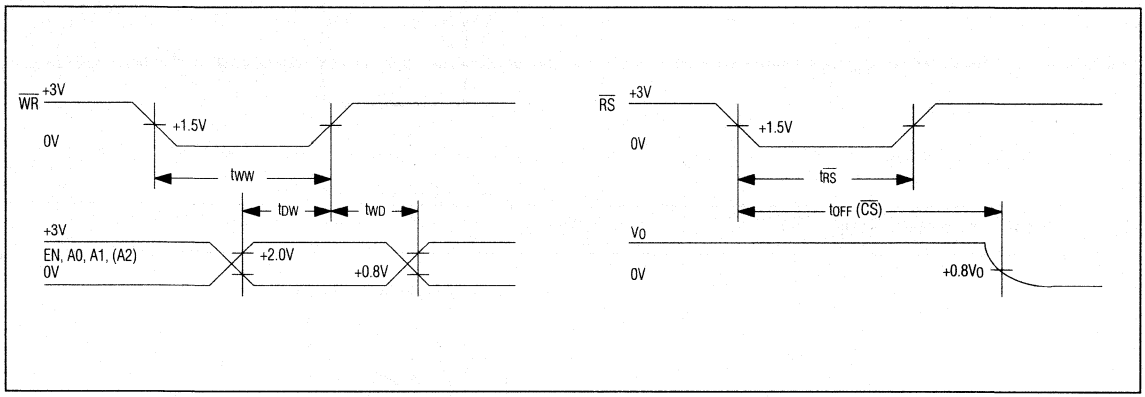


Figure 1. MAX388/MAX389 Typical Timing Diagrams

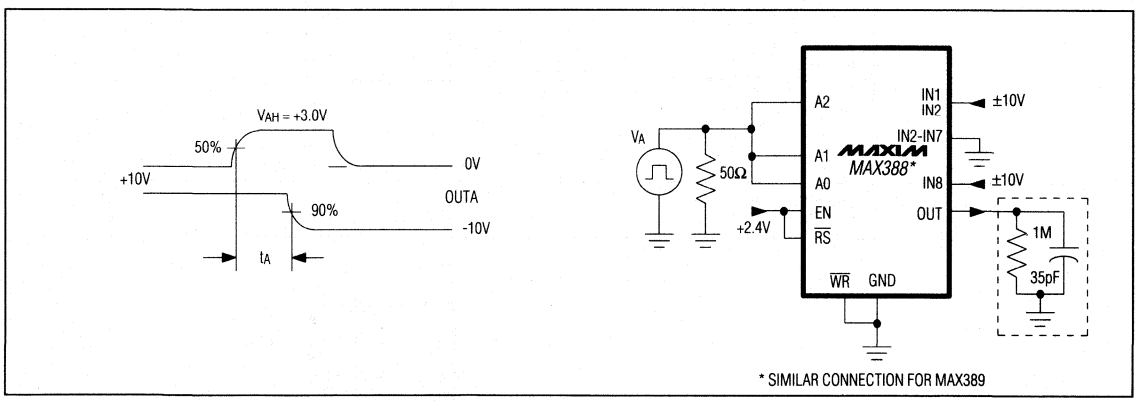


Figure 2. Access Time vs. Logic Level (High)

High-Voltage, Fault-Protected Analog Multiplexers

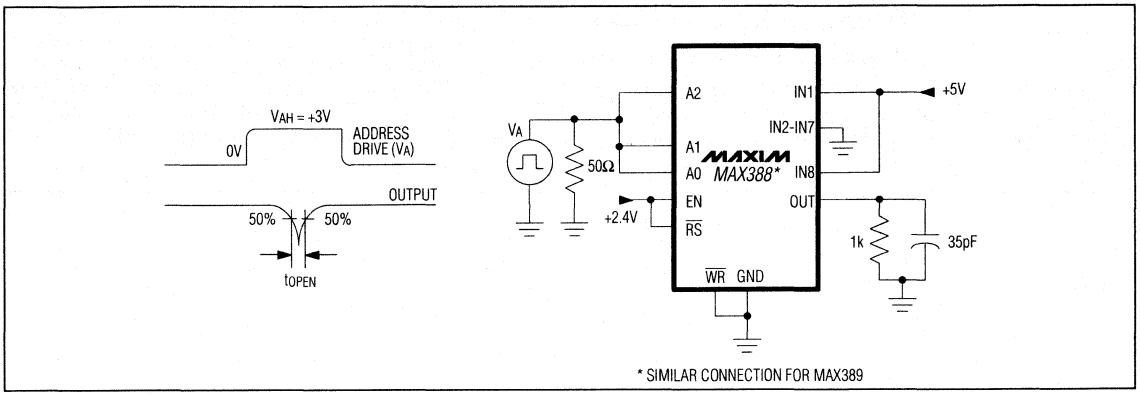


Figure 3. Break-Before-Make Delay (t_{OPEN})

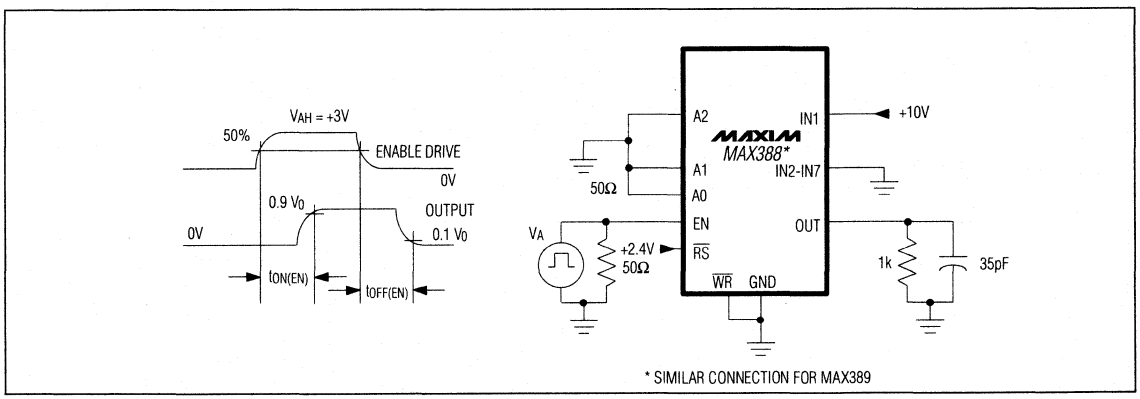


Figure 4. Enable Delay ($t_{ON(EN)}$, $t_{OFF(EN)}$)

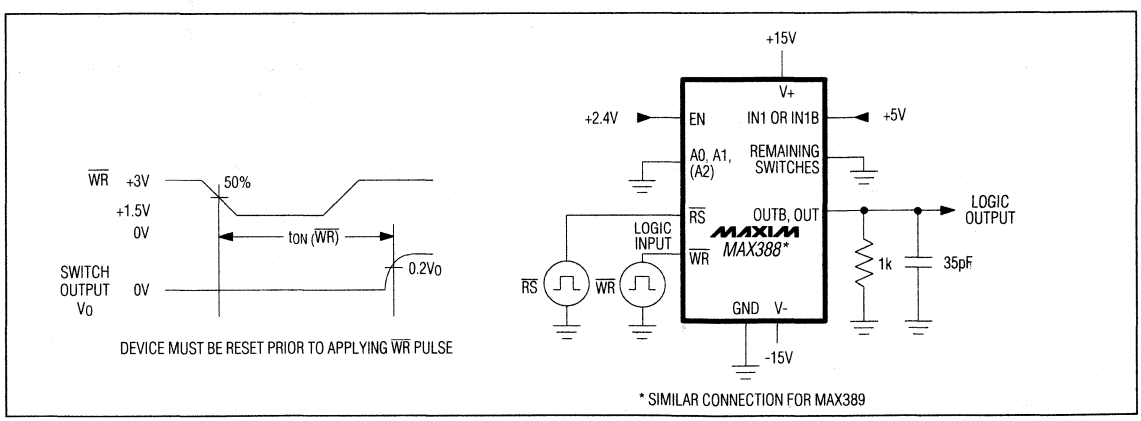


Figure 5. Write Turn-On Time ($t_{ON(\overline{WR})}$)

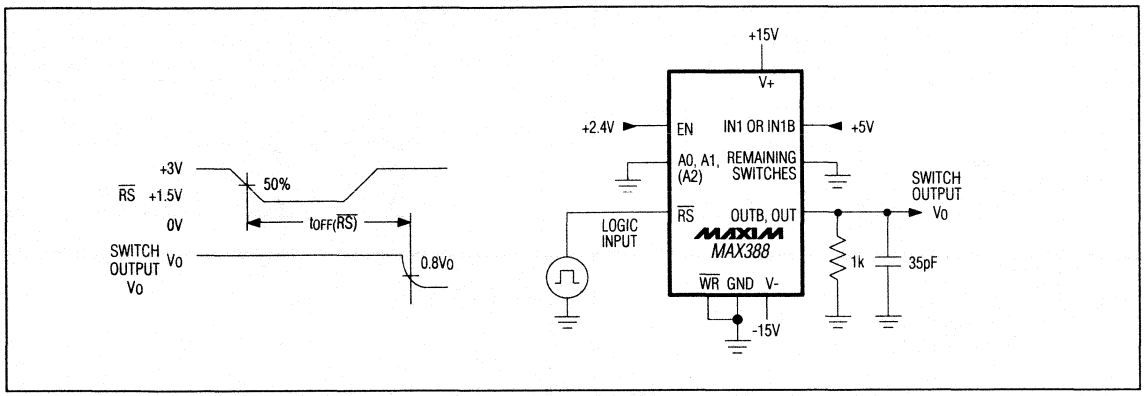


Figure 6. Reset Turn-Off Time ($t_{OFF(\overline{RS})}$)

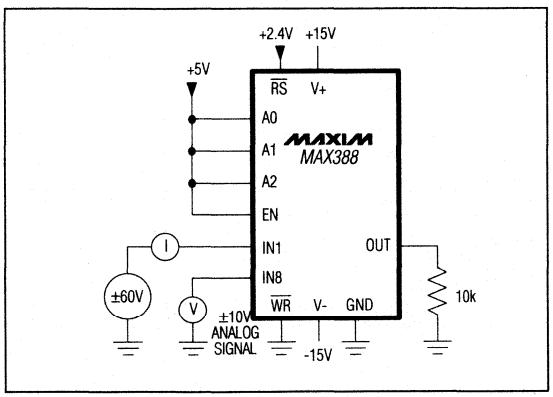


Figure 7. Input Leakage Current (Overvoltage)

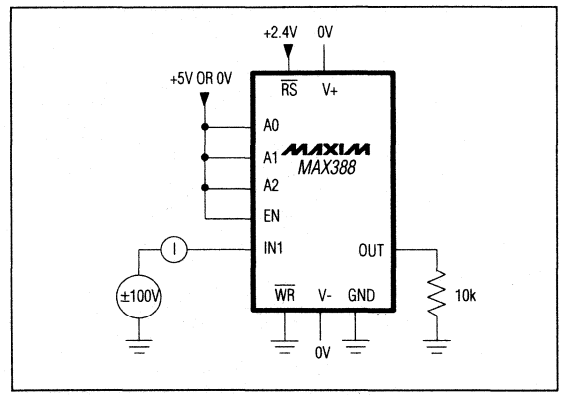


Figure 8. Input Leakage Current (Power Supplies Off)

Figures 9 and 10 show how the series FET circuit protects against overvoltage conditions. When power is off, the gates of all three FETs are at ground. With a -100V input, N-channel FET Q1 is turned on by the +100V gate-to-source voltage. However, the P-channel device Q2 with a V_{GS} of +100V turns off, thereby preventing the input signal from reaching the output. If the input voltage is +100V, Q1 has a negative V_{GS}, which turns it off. Similarly, with overvoltage on the output, only sub-microamp leakage currents flow from the output back to the input, since overvoltages turn off either Q1 or Q2.

Figure 11 shows an off channel with V+ and V- present. As with Figures 9 and 10, either an N-channel or a P-channel device will be off for any input voltage from -100V to +100V. The leakage current with negative overvoltages immediately drops to a few nanoamps at +25°C. The fault current for positive overvoltages is initially 40µA to 50µA, decaying over a few seconds to the nanoamp level. The time constant of this decay is due to stored charge on internal nodes and does not compromise fault-protection.

Figure 12 shows an on channel with V+ and V- present. With input voltages less than ±10V, all three FETs are on, and the input signal appears at the output. If the input voltage exceeds V+ minus the N-channel threshold voltage (V_{TN}), the N-channel FET will turn off. Since V_{TN} is typically 1.5V and the P-channel threshold voltage (V_{TP}) is typically 3V, the muxes' output swing is limited to approximately -12V to +13.5V with ±15V supplies.

High-Voltage, Fault-Protected Analog Multiplexers

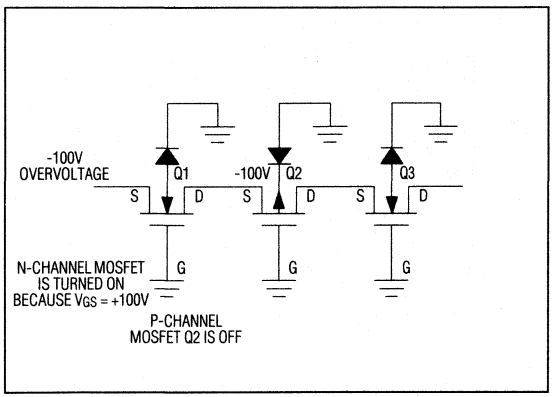


Figure 9. -100V Overvoltage with Mux Power Off

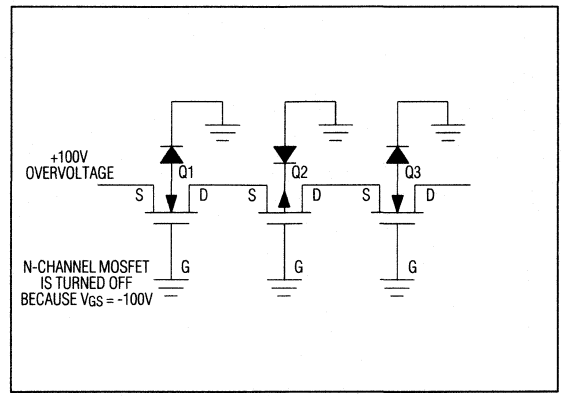


Figure 10. +100V Overvoltage with Mux Power Off

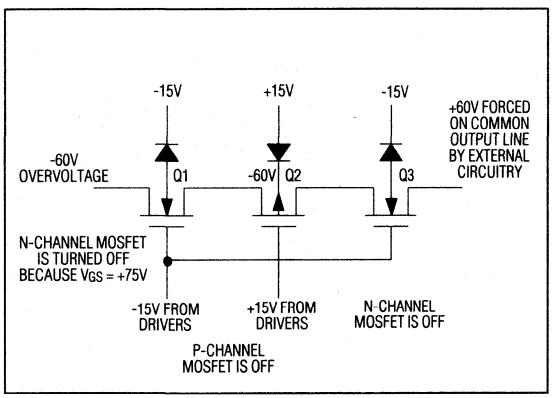


Figure 11. Off-Channel Overvoltage (-60V) with Mux Power On

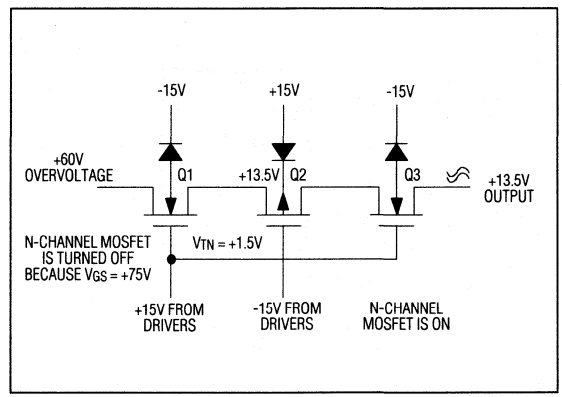


Figure 12. On-Channel Overvoltage (+60V) with Mux Power On

The *Typical Operating Characteristics* graphs show typical fault leakage vs. fault voltage curves. The MAX388/MAX389 muxes perform well up to the ±115V maximum rating, providing an additional safety margin.

Switching Characteristics and Charge Injection

MAX388/MAX389 channel-to-channel switching time is typically 600ns, including approximately 200ns of break-before-make delay. This delay prevents the input-to-input short that would occur if two input channels were simultaneously connected to the output. In a typical data-acquisition system (Figure 13), the dominant delay is not the MAX388 mux switching time, but the settling time of the following amplifiers and sample-and-hold (S/H). Another limiting factor is the RC time constant formed by the mux $r_{DS(ON)}$ plus the signal source impedance times the load capacitance on the mux output. Even with low signal-source impedances, 100pF capacitance on the mux output approximately doubles the settling time to 0.01% accuracy.

Tables 2a and 2b show typical charge injection levels vs. power-supply voltage and analog input voltages. Note: Since channels are well matched, differential charge injection for the MAX389 is typically less than 5pC. Charge injection that occurs during switching creates a voltage transient with a magnitude inversely proportional to mux output capacitance.

Table 1a. MAX388 Truth Table

A2	A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching						
X	X	X	X	↑	1	Maintains previous switch condition
Reset						
X	X	X	X	X	0	NONE (latches cleared)
Transparent Operation						
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

Table 1b. MAX389 Truth Table

A1	A0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching					
X	X	X	↑	1	Maintains previous switch condition
Reset					
X	X	X	X	0	NONE (latches cleared)
Transparent Operation					
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

NOTE: Logic "1" : $V_{AH} \geq 2.4V$, Logic "0" : $V_{AL} \leq 0.8V$

Operation from Supply Voltages Other than ±15V

The main limitation of supply voltages other than ±15V is a reduction in output signal range. The MAX388 limits the output voltage to typically 1.5V below V+ and 3V above V-. Output swing is limited to +3.5V to -2V when operating from ±5V. The *Typical Operating Characteristics* graphs show typical $r_{DS(ON)}$ for ±15V, ±10V, and ±5V supplies. Operation is guaranteed for ±4.5V to ±18V supplies. Switching delays increase by a factor of two or more at ±5V, but break-before-make operation is preserved.

The MAX388/MAX389 may be powered from a single +9V to +22V supply, as well as from unbalanced supplies such as +15V and -5V. Connect V- to 0V when operating with a +9V to +22V single supply. The digital threshold remains approximately 1.6V above GND, and analog characteristics (such as $r_{DS(ON)}$) are determined by total voltage difference between V+ and V-. This means the MAX388/MAX389 operate with standard TTL logic levels, even with ±5V power supplies.

Table 2a. MAX388 Charge Injection

Supply Voltage (V)	Analog Input Level (V)	Injected Charge (pC)
±5	1.7 0.0 -1.7	100 70 45
±10	5.0 0.0 -5.0	200 130 60
±15	10.0 0.0 -10.0	500 180 50

Test Conditions: C_L = 1000pF on mux output; the tabulated analog input level is applied to channel 1; channels 2 through 8 inputs are open circuited. EN = +5V, A1 = A2 = 0V, A0 is toggled at 2kHz rate between 0V and 3V. +100pC of charge creates a +100mV step when injected into a 1000pF load capacitance.

High-Voltage, Fault-Protected Analog Multiplexers

Table 2b. MAX389 Charge Injection

Supply Voltage (V)	Analog Input Level (V)	Injected Charge (pC)		
		OUTA	OUTB	Differential A-B
±5	1.7	105	107	-2
	0.0	73	74	-1
	-1.7	48	50	-2
±10	5.0	215	220	-5
	0.0	135	139	-4
	-5.0	62	63	-1
±15	10.0	525	530	-5
	0.0	180	185	-5
	-10.0	55	55	0

Test Conditions: C_L = 1000pF on OUTA and OUTB; the tabulated analog input level is applied to inputs 1A and 1B; channels 2 through 4 are open circuited. EN = +5V, A1 = 0V, A0 is toggled from 0V to 3V at a 2kHz rate.

Digital-Interface Levels

The typical digital threshold of both the address lines and the Enable (EN) input is 1.6V, with a temperature coefficient of about -3mV/°C. This ensures compatibility with a 0.8V to 2.4V TTL logic swing over the entire temperature range. The digital threshold is relatively independent of the supply voltages, typically moving from 1.6V to 1.5V as the power supplies are reduced from ±15V to ±5V. In all cases, digital thresholds are referenced to GND.

The digital inputs can also be driven with CMOS logic levels swinging from either V+ to V- or from V+ to GND. Digital input current is just a few nanoamps leakage at all input voltage levels, with a guaranteed maximum of 1µA. The digital inputs are protected from ESD by a 30V zener diode between the input and V+, and can be driven ±4V beyond the supplies without drawing excessive current.

Operation as Demultiplexers

The MAX388/MAX389 function as demultiplexers when an input is applied to the Output (OUT) pin, and channel inputs are used as outputs. Break-before-make operation and full fault protection are provided when operating as demultiplexers, unlike first-generation fault-protected muxes.

Table 3a. Typical Off-Isolation Rejection Ratio

Frequency (Hz)	100k	500k	1M
One Channel Driven (dB)	74	72	66
All Channels Driven (dB)	64	48	44

Test Conditions: V_{IN} = $20V_{p-p}$ at the tabulated frequency, R_L = 1.5k between OUT and GND, EN = 0V.

$$OIRR = 20\log\frac{20V}{V_{OUT}}$$

Table 3b. Typical Crosstalk Rejection Ratio

Frequency (Hz)	100k	500k	1M
F_L = 1.5k (dB)	70	68	64
R_L = 10k (dB)	62	46	42

Test Conditions: Specified R_L connected from OUT to Ground, EN = +5V, A0 = A1 = A2 = +5V (channel 1 selected). 20Vp-p at the tabulated frequency is applied to channel 2. All other channels are open circuited. Similar crosstalk rejection can be observed between any two channels.

Leakage, Crosstalk, and Isolation

At DC and low frequencies, channel-to-channel crosstalk is caused by variation in output leakage currents as the off-channel input voltages are varied. The MAX388 ouput leakage varies only a few picoamps as all seven off inputs are toggled from -10V to +10V. The output voltage change depends on the impedance level at the MAX388 output ($r_{DS(ON)}$ plus the input-signal source resistance), since the load driven by the MAX388 is usually a high impedance. For a signal source impedance of 10kΩ or lower, DC crosstalk exceeds 120dB.

Tables 3a and 3b show typical AC crosstalk and off-isolation performance. Digital feedthrough is masked by analog charge injection when the output is enabled. When the output is disabled, digital feedthrough is virtually unmeasurable, since the digital pins are physically isolated from the analog section by the GND and V- pins. The guard formed by these lines is continued onto the MAX388/MAX389 die to provide over 100dB isolation between the digital and analog sections at f = 100kHz.

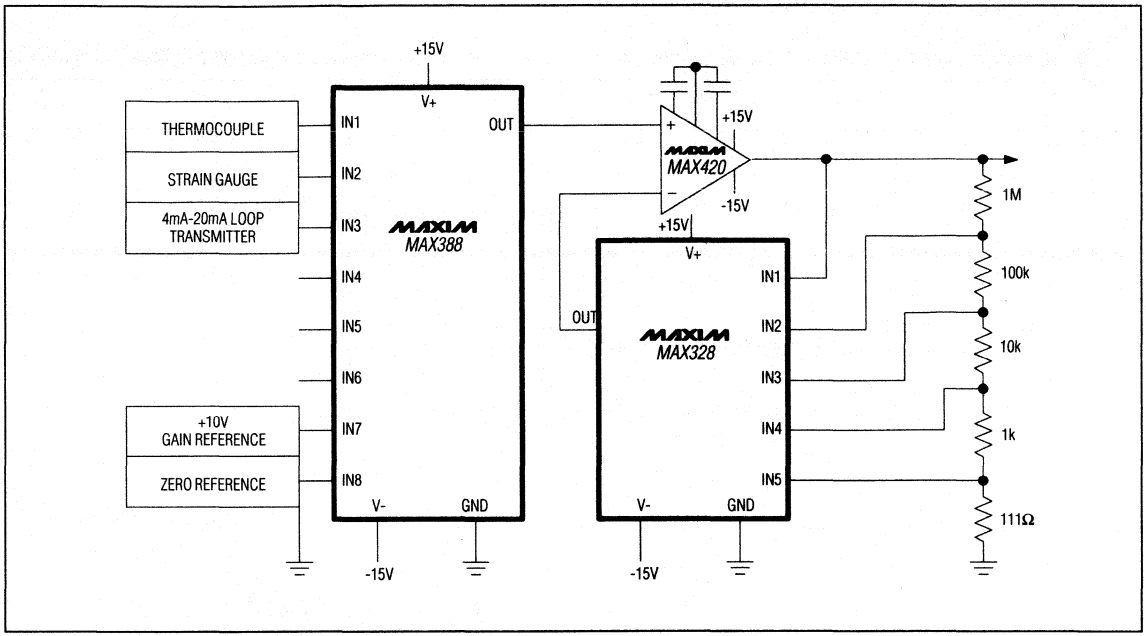


Figure 13. Typical Data-Acquisition Front End

Applications Information

Figure 13 shows a typical data-acquisition system incorporating the MAX388. Since the mux is driving a high-impedance input, the error is a function of the mux on resistance ($r_{DS(ON)}$) times the leakage current ($I_{OUT(ON)}$) and the amplifier bias current (I_{BIAS}):

$$V_{ERR} = [r_{DS(ON)}] [I_{OUT(ON)} + I_{BIAS}(MAX420)]$$
$$= (3k\Omega) (2nA + 30pA)$$
$$= 6.1\mu V \text{ maximum error}$$

In most cases, this error is low enough that preamplification of input signals is not needed, even with very low-level signals, such as 40µV/°C from type J thermocouples.

In systems with fewer than eight inputs, an unused channel can be connected to the system ground reference point for software-zero correction. A second channel connected to the system voltage reference allows gain correction of the entire data-acquisition system as well.

A MAX420 precision op amp is connected as a programmable gain amplifier, with gains ranging from 1 to 10,000. The guaranteed 5µV unadjusted MAX420 offset voltage maintains high-signal accuracy, while programmable gain allows the output signal level to be scaled to the optimum range for the remainder of the data-acquisition system, normally an S/H and an ADC. Since the gain-changing mux is not connected to external sensors and this point in the circuit does not require fault protection, the MAX328 low-leakage mux works well here.

Input switching, however, needs fault protection to provide the protection and isolation required for most data-acquisition inputs. Since external signal sources may continue to supply voltage when the system power is off, non-fault-protected muxes, or even first-generation fault-protected devices, allow many milliamps of fault current to flow from outside sources into the mux.

The MAX388/MAX389 eliminate these problems by limiting output voltage to safe levels (with or without power applied) and by turning all channels off when power is removed. Consequently, only sub-microamp fault currents are maintained for continuous input levels up to ±100V with power supplies off.

High-Voltage, Fault-Protected Analog Multiplexers

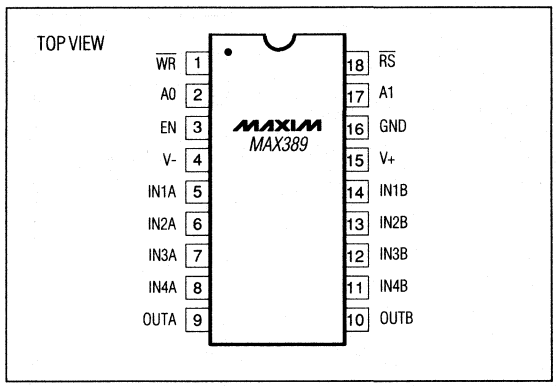
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX389CPN	0°C to +70°C	18 Plastic DIP
MAX389CJN	0°C to +70°C	18 CERDIP
MAX389C/D	0°C to +70°C	Dice*
MAX389EPN	-40°C to +85°C	18 Plastic DIP
MAX389EJN	-40°C to +85°C	18 CERDIP
MAX389MJN	-55°C to +125°C	18 CERDIP**

* *Contact factory for dice specifications.*

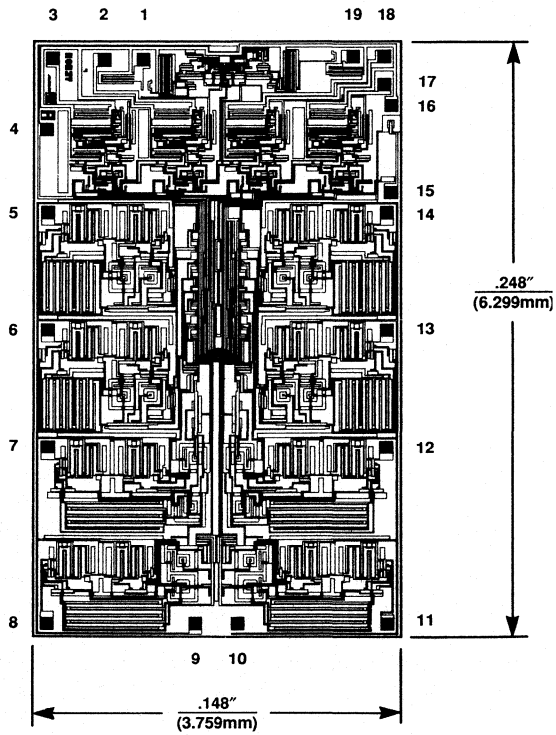
** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations (continued)



Chip Topography

DIE PAD #	MAX388	MAX389
1	$\overline{WR}$	$\overline{WR}$
2	A0	A0
3	EN	EN
4	V-	V-
5	IN1	IN1A
6	IN2	IN2A
7	IN3	IN3A
8	IN4	IN4A
9	OUT	OUTA
10	N.C.	OUTB
11	IN8	IN4B
12	IN7	IN3B
13	IN6	IN2B
14	IN5	IN1B
15	V+	V+
16	GND	GND
17	A2	N.C.
18	A1	A1
19	$\overline{RS}$	$\overline{RS}$



19-4727; Rev. 0; 12/91

MAXIM

Dual High-Speed Analog Switches

General Description

The DG401/DG403/DG405 are dual high-speed analog switches. The DG401 and DG405 dual switches are normally closed, (SPST, NC) and (DPST, NC), respectively. The DG403 has one normally open and one normally closed pole (DPST). All three parts offer low on resistance (less than 35Ω), low leakage (less than 250pA), and fast switching – turn-on time less than 150ns and turn-off time less than 100ns.

The DG401/DG403/DG405 are fabricated with Maxim's new improved silicon gate process for high system accuracy. A 44V maximum breakdown voltage allows rail-to-rail switch-off blocking capability.

These switches can be used with a single positive supply (+12V to +30V) or split supplies (±4.5V to ±20V) while retaining CMOS logic input compatibility and fast switching. CMOS inputs provide reduced input loading and very low leakage currents.

Applications

Sample-and-Hold Circuits
Test Equipment
Winchester Disk Drives
Heads-Up Displays
Guidance and Control Systems
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

Features

- ◆ $r_{DS(ON)}$ < 35Ω
- ◆ Leakage < 250pA
- ◆ Single- or Bipolar-Supply Operation
- ◆ TTL/CMOS Logic Compatible
- ◆ Rail-to-Rail Switch-Off Blocking Capability
- ◆ Monolithic, Low-Power Design

Ordering Information

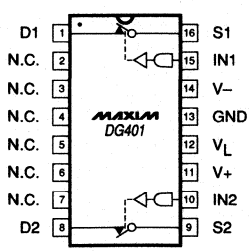
PART	TEMP. RANGE	PIN-PACKAGE
DG401C/D	0°C to +70°C	Dice*
DG401DJ	-40°C to +85°C	16 Plastic DIP
DG401DY	-40°C to +85°C	16 Narrow SO
DG401DK	-40°C to +85°C	16 CERDIP
DG401AK	-55°C to +125°C	16 CERDIP**
DG401AZ	-55°C to +125°C	20 LCC**
DG403C/D	0°C to +70°C	Dice*
DG403DJ	-40°C to +85°C	16 Plastic DIP
DG403DY	-40°C to +85°C	16 Narrow SO
DG403DK	-40°C to +85°C	16 CERDIP
DG403AK	-55°C to +125°C	16 CERDIP**
DG403AZ	-55°C to +125°C	20 LCC**

Ordering Information continued on last page.

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

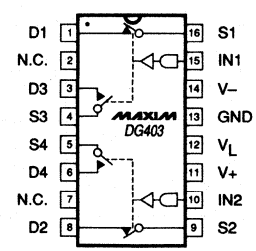
Pin Configurations/Block Diagrams/Truth Tables*

TOP VIEW



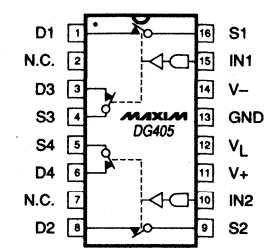
DIP/SO

DG401	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

DG403		
LOGIC	SWITCH 1, 2	SWITCH 3, 4
0	OFF	ON
1	ON	OFF



DIP/SO

DG405	
LOGIC	SWITCH
0	OFF
1	ON

*SWITCHES SHOWN FOR LOGIC "1" INPUT

LCC on last page

Dual High-Speed Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
Digital Inputs V_S, V_D (Note 1) ..... V- -2V to V+ +2V or 20mA (whichever occurs first)
Current (any terminal, except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(pulsed at 1ms, 10% duty cycle max) 70mA

Continuous Power Dissipation (T_A = +70°C) (Note 2)
16-Pin Plastic DIP (derate 7.5mW/°C above +70°C) ..470mW
16-Pin Narrow SO (derate 8.7mW/°C above +70°C) ..696mW
16-Pin CERDIP (derate 10mW/°C above +70°C) 900mW
20-Pin LCC (derate 9.09mW/°C above +70°C) 727mW
Operating Temperature Ranges:
DG40_C ..... 0°C to +70°C
DG40_D ..... -40°C to +85°C
DG40_A ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Signals on Sx, Dx or INx exceeding V+ or V– are clamped by internal diodes. Limit forward current to maximum current rating.

Note 2: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		TEMP. RANGE	MIN	TYP	MAX (Note 2)	UNITS
SWITCH								
Analog-Signal Range	V_{ANALOG}	(Note 3)			–15		15	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = –10mA, V_D = ±10V, V+ = 13.5V, V– = –13.5V	T_A = +25°C	C,D		20	45	Ω
				A		20	35	
			T_A = T_{MIN} to T_{MAX}	C,D			55	
				A			45	
ΔDrain-Source On Resistance (Note 4)	$\Delta r_{DS(ON)}$	I_S = –10mA, V_D = 5V, 0V, or –5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C				3	Ω
			T_A = T_{MIN} to T_{MAX}				5	
Source-Off Leakage Current	$I_{S(OFF)}$	V_D = ∓15.5V, V_S = ±15.5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C	A	–0.25	–0.01	0.25	nA
				C,D	–0.50	–0.01	0.50	
			T_A = T_{MIN} to T_{MAX}	C,D	–20		20	
				A	–20		20	
Drain-Off Leakage Current	$I_{D(OFF)}$	V_D = ±15.5V, V_S = ∓15.5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C	A	–0.25	–0.01	0.25	nA
				C,D	–0.50	–0.01	0.50	
			T_A = T_{MIN} to T_{MAX}	C,D	–20		20	
				A	–20		20	
Channel-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = ±15.5V, V_S = ±15.5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C	C,D	–1.0	–0.04	1.0	nA
				A	–0.4	–0.04	0.4	
			T_A = T_{MIN} to T_{MAX}	C,D	–40.0		40.0	
				A	–40.0		40.0	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I_{INH}	IN_ = 2.4V, all others = 0.8V		-1.000	0.005	1.000	µA
Input Current with Input Voltage Low	I_{INL}	IN_ = 0.8V, all others 2.4V		-1.000	0.005	1.000	µA
SUPPLY							
Power-Supply Range				±4.5		±20	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C		0.01	1.00	µA
			T_A = T_{MIN} to T_{MAX}			5.00	
Negative Supply Current	I-	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1.00	-0.01		µA
			T_A = T_{MIN} to T_{MAX}	-5.00			
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C		0.01	1.00	µA
			T_A = T_{MIN} to T_{MAX}			5.00	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V- = -16.5V	T_A = +25°C	-1.00	-0.01		µA
			T_A = T_{MIN} to T_{MAX}	-5.00			
DYNAMIC							
Turn-On Time	t_{ON}	Figure 1	T_A = +25°C		100	150	ns
Turn-Off Time	t_{OFF}	Figure 1	T_A = +25°C		60	100	ns
Break-Before-Make Time Delay (Note 3)	t_D	DG403 Only, Figure 2	T_A = +25°C	10	20		ns
Charge Injection	Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 5	T_A = +25°C		60		pC
Off Isolation (Note 5)	OIRR	R_L = 100Ω, C_L = 5pF, f = 1MHz, Figure 4	T_A = +25°C		72		dB
Crosstalk (Note 6)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		90		dB
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		12		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 6	T_A = +25°C		12		pF
Channel-On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	f = 1MHz, Figure 7	T_A = +25°C		39		pF

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta r_{DS(ON)} = \Delta r_{DS(ON)}MAX - \Delta r_{DS(ON)}MIN$

Note 5: See Figure 4. Off isolation = $20\log_{10} V_D/V_S$, V_D = output, V_S = input to off switch.

Note 6: Between any two switches. See Figure 5.

Dual High-Speed Analog Switches

Pin Description

DG401 PIN DIP/SO	LCC	NAME	FUNCTION
1,8	2,10	D1, D2	Drain Outputs
2-7	1, 3-9,11,16	N.C.	No Connect
9,16	5, 7,12, 20	S2, S1	Source Outputs
10,15	13,19	IN2, IN1	Inputs
11	14	V+	Positive Supply Voltage Input–connected to substrate
12	15	V_L	Logic Supply Voltage
13	17	GND	Ground
14	18	V–	Negative Supply Voltage Input

DG403/DG405 PIN DIP/SO	LCC	NAME	FUNCTION
1,8,3,6	2, 4, 8,10	D1-D4	Drain Outputs
2,7	1, 3, 6, 9,11,16	N.C.	No Connect
11	14	V+	Positive Supply Voltage Input–connected to substrate
12	15	V_L	Logic Supply Voltage
13	17	GND	Ground
14	18	V-	Negative Supply Voltage Input
15,10	19,13	IN1, IN2	Inputs
16,9,4,5	5, 7,12, 20	S1-S4	Source Outputs

Test Circuits/Timing Diagrams

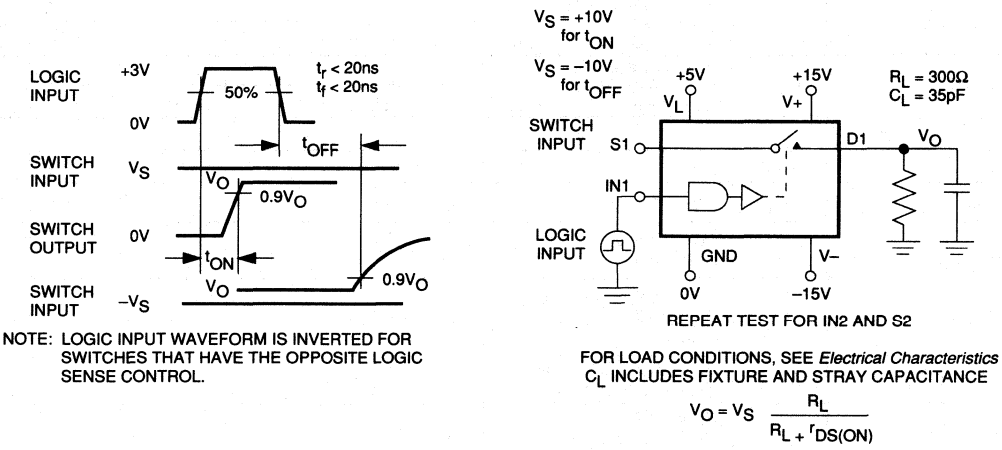


Figure 1. Switching-Time Test Circuit

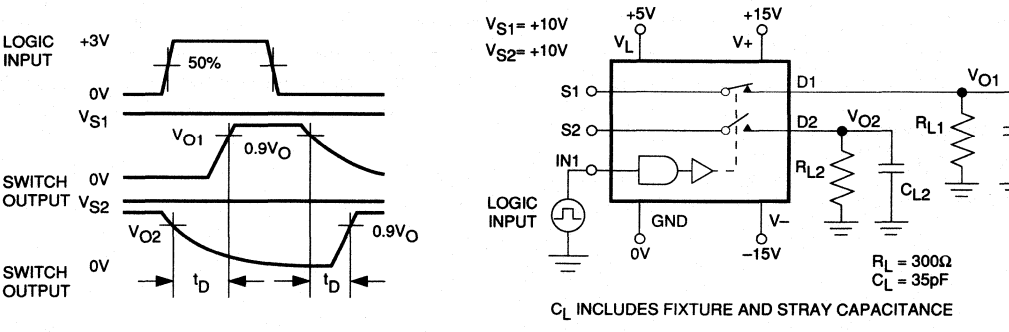


Figure 2. Break-Before-Make Test Circuit

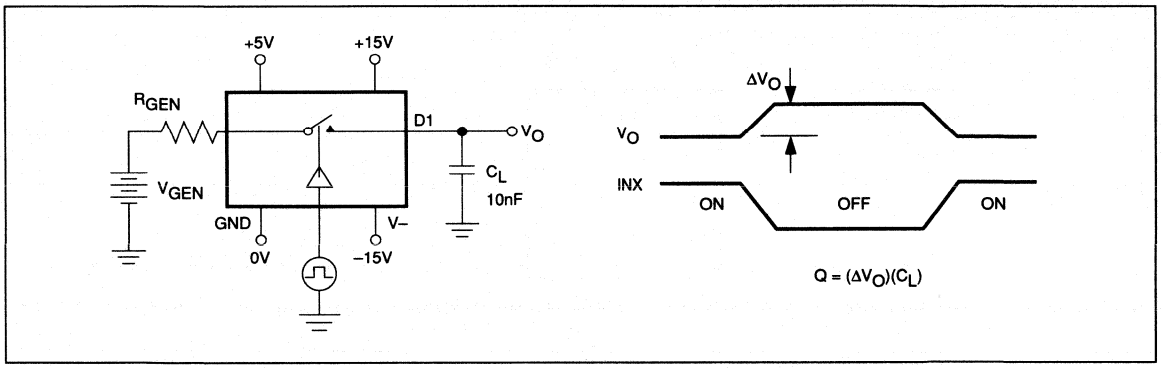
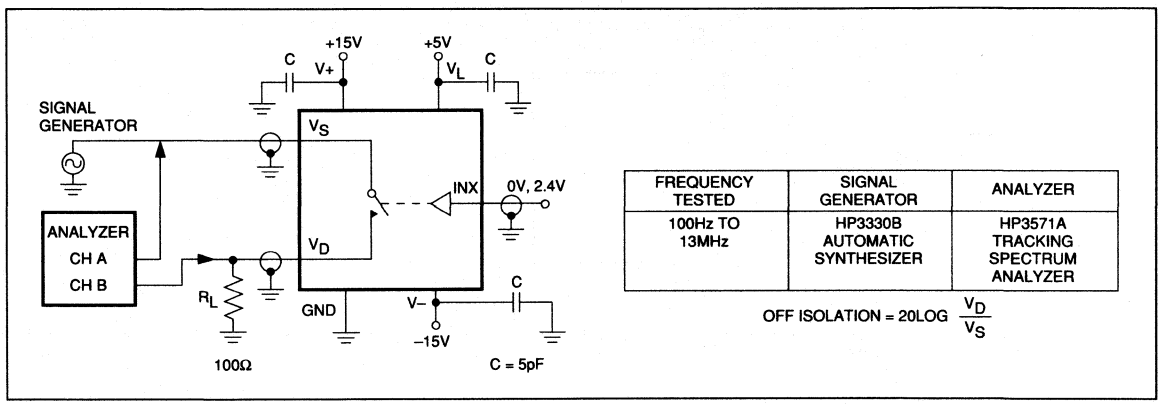


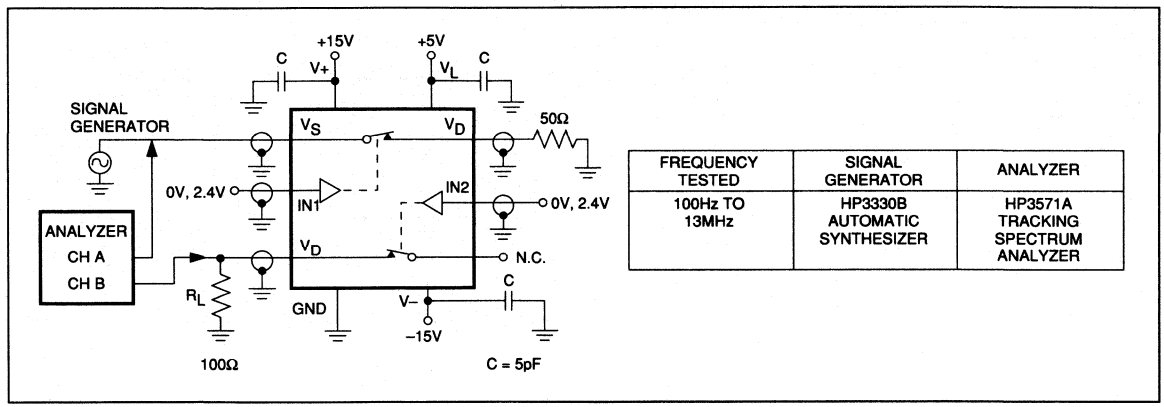
Figure 3. Charge-Injection Test Circuit



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100Hz TO 13MHz	HP3330B AUTOMATIC SYNTHESIZER	HP3571A TRACKING SPECTRUM ANALYZER

$$\text{OFF ISOLATION} = 20\log\frac{V_D}{V_S}$$

Figure 4. Off-Isolation Test Circuit



FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100Hz TO 13MHz	HP3330B AUTOMATIC SYNTHESIZER	HP3571A TRACKING SPECTRUM ANALYZER

Figure 5. Crosstalk Test Circuit

Dual High-Speed Analog Switches

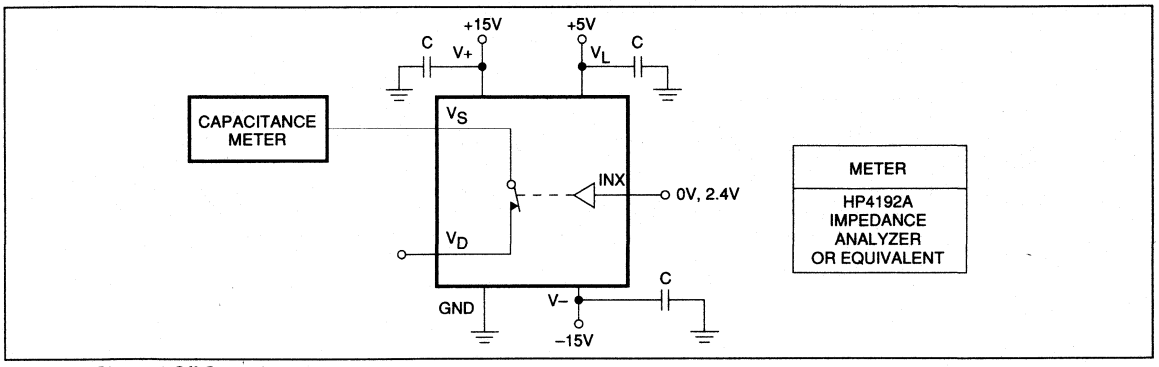


Figure 6. Channel-Off Capacitance

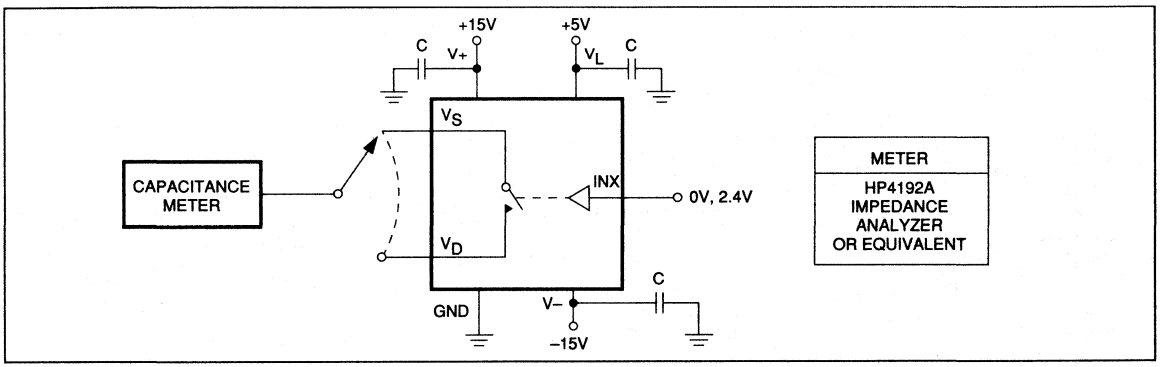


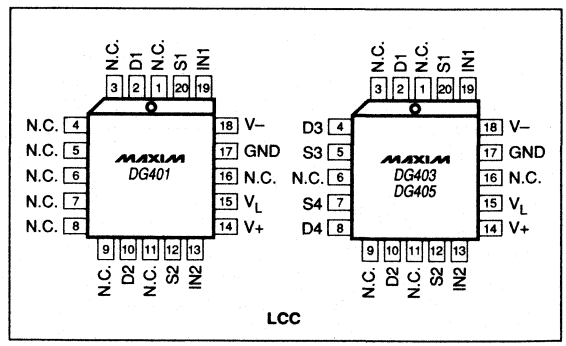
Figure 7. Channel-On Capacitance

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
DG405C/D	0°C to +70°C	Dice*
DG405DJ	-40°C to +85°C	16 Plastic DIP
DG405DY	-40°C to +85°C	16 Narrow SO
DG405DK	-40°C to +85°C	16 CERDIP
DG405AK	-55°C to +125°C	16 CERDIP**
DG405AZ	-55°C to +125°C	20 LCC**

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations (continued)



19-4729; Rev. 0; 12/91

MAXIM

16-Channel/Dual 8-Channel High Performance CMOS Analog Multiplexers

General Description

The DG406/DG407 are monolithic CMOS analog multiplexers (muxes). The DG406 is a single-ended 1-of-16 device, and the DG407 is a differential 2-of-8 device. Both are pin and functionally compatible with the industry-standard DG506A/DG507A.

The DG406/DG407 are fabricated with Maxim's new improved silicon gate process. Both parts offer low on resistance (100Ω max), improved leakage over temperature, low power consumption (I_{SUPPLY} = 75µA max) and fast switching speeds (t_{TRANS} = 250ns max). The 44V maximum breakdown voltage allows switch-off blocking capability rail-to-rail.

These muxes can be used with a single positive supply (+12V to +30V) or split supplies (±4.5V to ±20V) while retaining CMOS logic input compatibility. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits

Test Equipment

Winchester Disk Drives

Heads-Up Displays

Guidance and Control Systems

Military Radios

Communications Systems

Battery-Operated Systems

PBX, PABX

Features

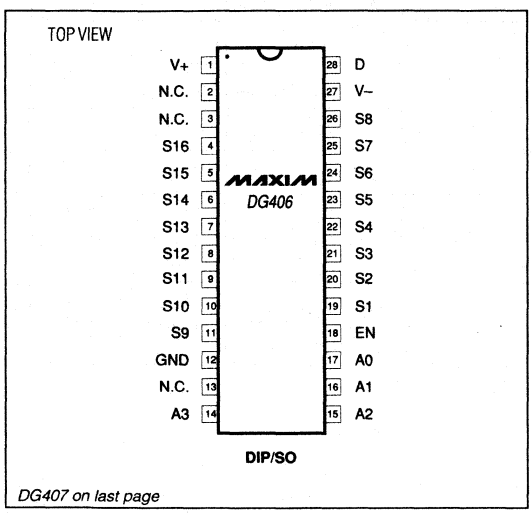
- ◆ $r_{DS(ON)}$: 100Ω Max, $\Delta r_{DS(ON)}$: 15Ω Max
- ◆ t_{TRANS}: 250ns Max
- ◆ Leakage - $T_A = T_{MIN}$ to T_{MAX}
  $I_{S(OFF)}$: 50nA Max
  $I_{D(OFF)}$: 100nA Max (DG407), 200nA Max (DG406)
  $I_{-(ON)}$: 100nA Max (DG407), 200nA Max (DG406)
- ◆ Q: 20pC Typ
- ◆ I_{SUPPLY}: 75µA Max
- ◆ Single- or Bipolar-Supply Operation
- ◆ TTL/CMOS Logic Compatible

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
DG406C/D	0°C to +70°C	Dice*
DG406DJ	-40°C to +85°C	28 Plastic DIP
DG406DN	-40°C to +85°C	28 PLCC
DG406DK	-40°C to +85°C	28 CERDIP
DG406AK	-55°C to +125°C	28 CERDIP**
DG407C/D	0°C to +70°C	Dice*
DG407DJ	-40°C to +85°C	28 Plastic DIP
DG407DN	-40°C to +85°C	28 PLCC
DG407DK	-40°C to +85°C	28 CERDIP
DG407AK	-55°C to +125°C	28 CERDIP**

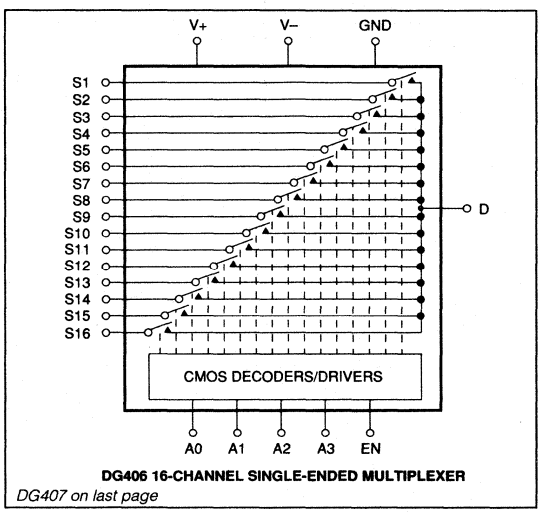
* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



DG407 on last page

Functional Diagrams



DG406 16-CHANNEL SINGLE-ENDED MULTIPLEXER

DG407 on last page

16-Channel/Dual 8-Channel High Performance CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
Digital Inputs V_S, V_D (Note 1) ..... V- -2V to V+ +2V or 30mA (whichever occurs first)
Current (any terminal, except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(pulsed at 1ms, 10% duty cycle max) 40mA

Continuous Power Dissipation (T_A = +70°C) (Note 2)
28-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ..727mW
28-Pin PLCC (derate 10.53mW/°C above +70°C) 842mW
28-Pin CERDIP (derate 16.67mW/°C above +70°C) ..1333mW
Operating Temperature Ranges:
DG406/407C/D ..... 0°C to +70°C
DG406/407D_ ..... -40°C to +85°C
DG406/407AK ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Signals on Sx, Dx, or INx exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.
Note 2: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Dual Supplies)

(V+ = 15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX (Note 3)	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 4)			–15		15	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = –10mA, V_D = ±10V		T_A = +25°C		50	100	Ω
				T_A = T_{MIN} to T_{MAX}			125	
$r_{DS(ON)}$ Matching Between Channels	$\Delta r_{DS(ON)}$	V_D = ±10V (Note 5)		T_A = +25°C			15	Ω
Source-Off Leakage Current	$I_{S(OFF)}$	V_D = ±10V, V_S = ∓10V, V_{EN} = 0V		T_A = +25°C	–0.5		0.5	nA
				T_A = T_{MIN} to T_{MAX}	–50		50	
Drain-Off Leakage Current	$I_{D(OFF)}$	V_S = ±10V, V_D = ∓10V, V_{EN} = 0V	DG406	T_A = +25°C	–2		2	nA
				T_A = T_{MIN} to T_{MAX}	–200		200	
			DG407	T_A = +25°C	–2		2	nA
				T_A = T_{MIN} to T_{MAX}	–100		100	
Drain-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = ±10V, V_S = ±10V, sequence each switch on	DG406	T_A = +25°C	–2		2	nA
				T_A = T_{MIN} toT_{MAX}	–200		200	
			DG407	T_A = +25°C	–2		2	nA
				T_A = T_{MIN} toT_{MAX}	–100		100	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX (Note 3)	UNITS
INPUT								
Input Current with Input Voltage High	I_{AH}	V_A = 2.4V, 15V			–10		10	µA
Input Current with Input Voltage Low	I_{AL}	V_{EN} = 0V, 2.4V, V_A = 0V			–10		10	µA
SUPPLY								
Power-Supply Range					±4.5		±20	V
Positive Supply Current	I+	V_{EN} = V_A = 0V					75	µA
Negative Supply Current	I–	V_{EN} = V_A = 0V			–75			µA
Positive Supply Current	I+	V_{EN} = 2.4V, V_A = 0V		T_A = +25°C			0.5	mA
				T_A = T_{MIN} to T_{MAX}			2	
Negative Supply Current	I–	V_{EN} = 2.4V, V_A = 0V			–500			µA
DYNAMIC								
Transition Time	t_{TRANS}	Figure 1		T_A = +25°C			250	ns
Break-Before-Make Interval	t_{OPEN}	Figure 2		T_A = +25°C	10			ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3		T_A = +25°C			200	ns
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3		T_A = +25°C			150	ns
Charge Injection	Q	C_L = 1nF, V_S = 0V, R_S = 0Ω		T_A = +25°C		20		pC
Off Isolation (Note 6)		V_{EN} = 0V, R_L = 1kΩ, f = 100kHz		T_A = +25°C		–65		dB
Logic Input Capacitance	C_{IN}	f = 1MHz		T_A = +25°C		8		pF
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, V_{EN} = V_S = 0V		T_A = +25°C		11		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, V_{EN} = V_D = 0V	DG406	T_A = +25°C		70		pF
			DG407			35		
Channel-On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	f = 1MHz, V_{EN} = V_D = 0V	DG406	T_A = +25°C		100		pF
			DG407			50		

16-Channel/Dual 8-Channel High Performance CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS (Single Supply)

(V+ = 12V, V- = 0V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN TYP MAX (Note 3)	UNITS
SWITCH						
Analog Signal Range	V_{ANALOG}	(Note 4)		T_A = +25°C	0 12	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = -1mA, V_D = 3V, 10V		T_A = +25°C	90	Ω
DYNAMIC						
Transition Time	t_{TRANS}	Figure 1, V_{S1} = 8V, V_{S8} = 0V, V_{IN} = 2.4V		T_A = +25°C	300	ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V		T_A = +25°C	250	ns
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V		T_A = +25°C	150	ns
Charge Injection	Q	C_L = 1nF, V_S = 6V, R_S = 0Ω		T_A = +25°C	5	pC

Note 3: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 4: Guaranteed by design.

Note 5: $\Delta r_{DS(ON)} = \Delta r_{DS(ON)}MAX - \Delta r_{DS(ON)}MIN$

Note 6: Worst-case isolation is on channel 4 because of its proximity to the drain pin. Off isolation = $20\log_{10} V_D/V_S$, V_D = output, V_S = input to off switch.

Truth Tables

A3	A2	A1	A0	EN	ON Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG406

A2	A1	A0	EN	ON Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG407

LOGIC "0" $V_{AL} \leq$ 0.8 V, LOGIC "1" = $V_{AH} \geq$ 2.4 V

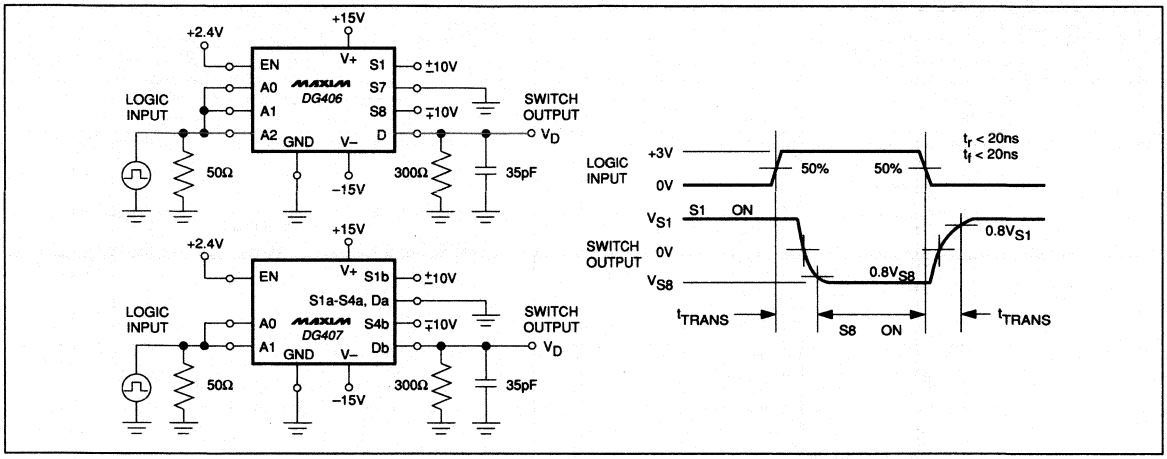


Figure 1. Transition-Time Test Circuit

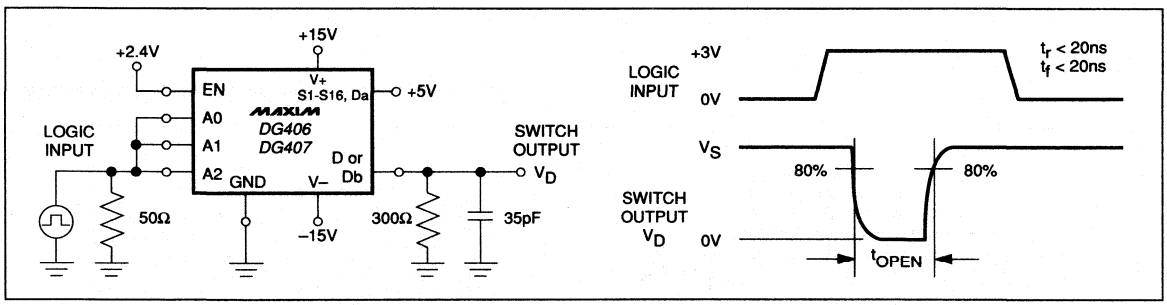


Figure 2. Break-Before-Make Interval Test Circuit

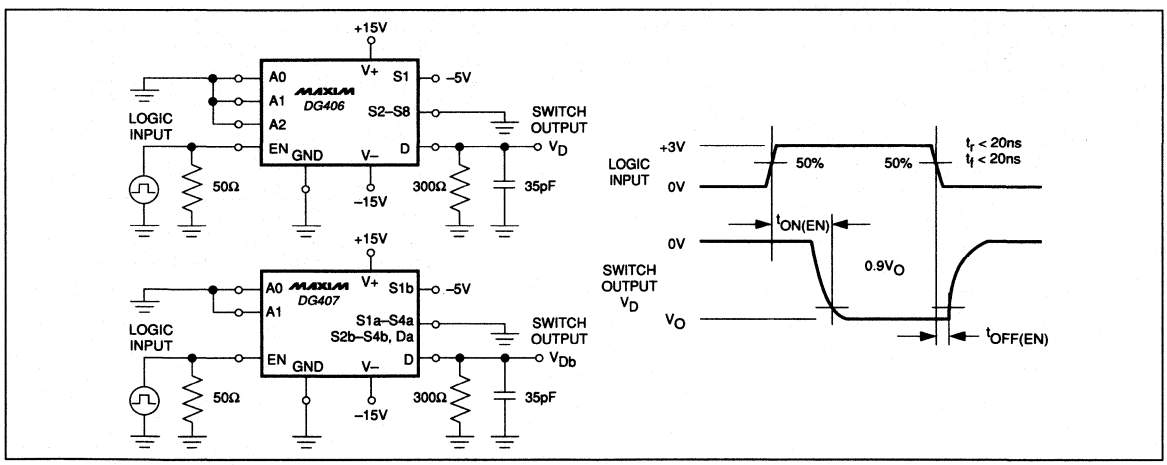
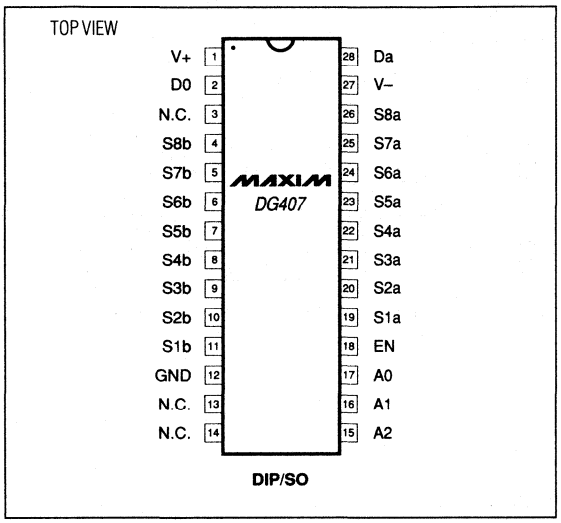
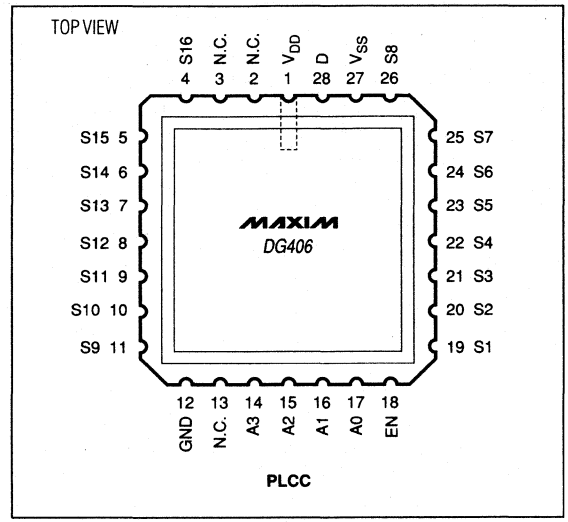


Figure 3. $t_{ON(EN)}$, $t_{OFF(EN)}$ Test Circuit

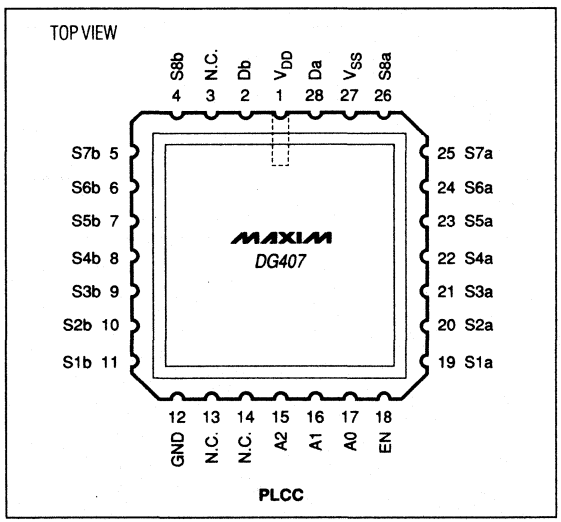
16-Channel/Dual 8-Channel High Performance CMOS Analog Multiplexers

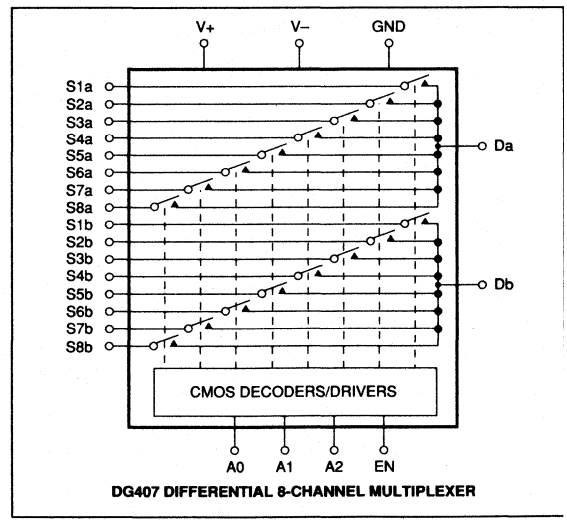
Pin Configurations (continued)





Functional Diagrams (continued)





19-4725; Rev. 0; 12/91

MAXIM

8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

General Description

The DG408 and DG409 are monolithic CMOS analog multiplexers (muxes). The DG408 is a single-ended 1-of-8 device, and the DG409 is a differential 2-of-4 device. Both devices are pin and functionally compatible with the industry standard DG508A/DG509A.

The DG408/DG409 are fabricated with Maxim's new improved silicon gate process. These muxes offer low on resistance (100Ω max), low leakage over temperature, low power consumption (I_{SUPPLY} = 75µA), and fast switching speeds (t_{TRANS} = 250ns max). The 44V maximum breakdown voltage allows rail-to-rail switch-off blocking capability.

The DG408/DG409 can be used with a single positive supply (+12V to +30V) or split supplies (±4.5V to ±20V) while retaining CMOS logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits

Test Equipment

Winchester Disk Drives

Heads-Up Displays

Guidance and Control Systems

Military Radios

Communications Systems

Battery-Operated Systems

PBX, PABX

Features

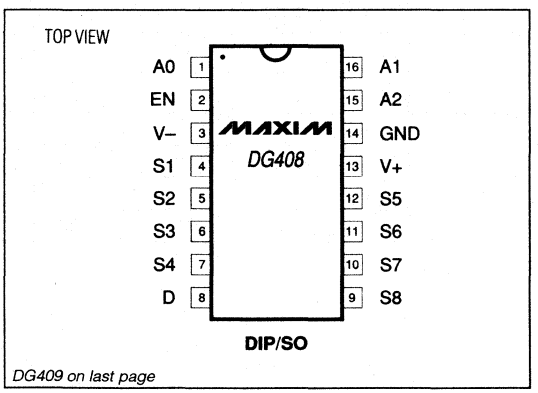
- ◆ $r_{DS(ON)}$: 100Ω Max
- ◆ t_{TRANS}: 250ns Max
- ◆ $\Delta r_{DS(ON)}$: 15Ω Max
- ◆ Leakage - $T_A = T_{MIN}$ to T_{MAX}
  $I_{S(OFF)}$: 50nA Max
  $I_{D(OFF)}$: 100nA Max (DG409), 200nA Max (DG408)
  $I_{D(ON)}$: 100nA Max (DG409), 200nA Max (DG408)
- ◆ Q: 20pC Typ
- ◆ Single-Supply Operation (+12V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ◆ TTL/CMOS Logic Compatible
- ◆ Rail-to-Rail Switch-Off Blocking Capability

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
DG408C/D	0°C to +70°C	Dice*
DG408DJ	-40°C to +85°C	16 Plastic DIP
DG408DY	-40°C to +85°C	16 Narrow SO
DG408DK	-40°C to +85°C	16 CERDIP
DG408AK	-55°C to +125°C	16 CERDIP**
DG409C/D	0°C to +70°C	Dice*
DG409DJ	-40°C to +85°C	16 Plastic DIP
DG409DY	-40°C to +85°C	16 Narrow SO
DG409DK	-40°C to +85°C	16 CERDIP
DG409AK	-55°C to +125°C	16 CERDIP**

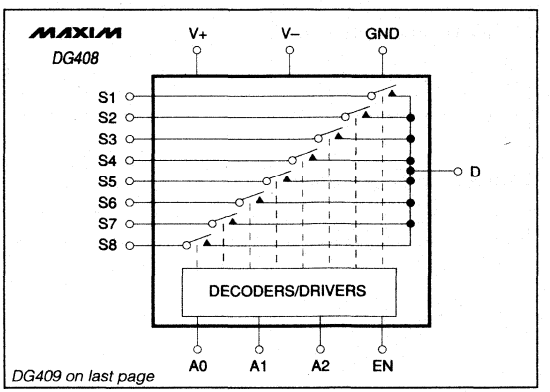
* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



DG409 on last page

Functional Diagrams



DG409 on last page

8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
Digital Inputs V_S, V_D (Note 1) ..... V- -2V to V+ +2V or 30mA (whichever occurs first)
Current (any terminal, except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(pulsed at 1 ms, 10% duty cycle max) 40mA

Continuous Power Dissipation (T_A = +70°C) (Note 2)
16-Pin Plastic DIP (derate 7.5 mW/°C above +70°C) .. 470mW
16-Pin Narrow SO (derate 8.7mW/°C above +70°C) .. 696mW
16-Pin CERDIP (derate 10mW/°C above +70°C) 900mW
Operating Temperature Ranges:
DG408/DG409C_ ..... 0°C to +70°C
DG408/DG409D_ ..... -40°C to +85°C
DG408/DG409AK ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Signals on Sx, Dx, or INx exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Note 2: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Dual Supplies)

(V+ = 15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX (Note 3)	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 4)			-15		15	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = -10mA, V_D = ±10V		T_A = +25°C		40	100	Ω
				T_A = T_{MIN} to T_{MAX}			125	
$r_{DS(ON)}$ Matching Between Channels	$\Delta r_{DS(ON)}$	V_D = ±10V (Note 5)		T_A = +25°C			15	Ω
Source-Off Leakage Current	$I_{S(OFF)}$	V_D = ∓10V, V_S = ±10V, V_{EN} = 0V		T_A = +25°C	-0.5		0.5	nA
				T_A = T_{MIN} to T_{MAX}	-50		50	
Drain-Off Leakage Current	$I_{D(OFF)}$	V_S = ±10V, V_D = ∓10V, V_{EN} = 0V	DG408	T_A = +25°C	-1		1	nA
				T_A = T_{MIN} to T_{MAX}	-100		100	
		V_S = ∓10V, V_D = ±10V, V_{EN} = 0V	DG409	T_A = +25°C	-1		1	
				T_A = T_{MIN} to T_{MAX}	-50		50	
Drain-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = ±10V, V_S = ±10V, sequence each switch on	DG408	T_A = +25°C	-1		1	nA
				T_A = T_{MIN} to T_{MAX}	-100		100	
			DG409	T_A = +25°C	-1		1	
				T_A = T_{MIN} to T_{MAX}	-50		50	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX (Note 3)	UNITS
INPUT								
Input Current with Input Voltage High	I_{AH}	V_A = 2.4V, 15V			-10		10	µA
Input Current with Input Voltage Low	I_{AL}	V_{EN} = 0V, 2.4V V_A = 0V			-10		10	µA
SUPPLY								
Power-Supply Range					±4.5		±20	V
Positive Supply Current	I+	V_{EN} = V_A = 0V					75	µA
Negative Supply Current	I-	V_{EN} = V_A = 0V			-75			
Positive Supply Current	I+	V_{EN} = 2.4V, V_A = 0V		T_A = +25°C			0.5	mA
				T_A = T_{MIN} to T_{MAX}			2	
Negative Supply Current	I-	V_{EN} = 2.4V, V_A = 0V			-500			µA
DYNAMIC								
Transition Time	t_{TRANS}	Figure 1					250	ns
Break-Before-Make Interval	t_{OPEN}	Figure 2		T_A = +25°C	10			ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3		T_A = +25°C			150	ns
				T_A = T_{MIN} to T_{MAX}			225	
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3		T_A = +25°C			150	ns
Charge Injection	Q	C_L = 10nF, V_S = 0V, R_S = 0Ω		T_A = +25°C		20		pC
Off Isolation (Note 6)		V_{EN} = 0V, R_L = 1kΩ, f = 100kHz		T_A = +25°C		-75		dB
Logic Input Capacitance	C_{IN}	f = 1MHz		T_A = +25°C		8		pF
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, V_{EN} = V_S = 0V		T_A = +25°C		11		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, V_{EN} = V_D = 0V	DG408	T_A = +25°C		40		pF
			DG409			20		
Channel-On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	f = 1MHz, V_{EN} = V_D = 0V	DG408	T_A = +25°C		54		pF
			DG409			34		

8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

ELECTRICAL CHARACTERISTICS (Single Supply)

(V+ = 12V, V- = 0V, GND = 0V, V_{AH} = +2.4V, V_{AL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX (Note 3)	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 3)			0		12	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = -1mA, V_D = 3V, 10V		T_A = +25°C		90		Ω
DYNAMIC								
Transition Time	t_{TRANS}	Figure 1, V_{S1} = 8V, V_{S8} = 0V, V_{IN} = 2.4V		T_A = +25°C		180		ns
Enable Turn-On Time	$t_{ON(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V		T_A = +25°C		180		ns
Enable Turn-Off Time	$t_{OFF(EN)}$	Figure 3, V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V		T_A = +25°C		120		ns
Charge Injection	Q	C_L = 10nF, V_S = 0V, R_S = 0Ω		T_A = +25°C		5		pC

Note 3: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 4: Guaranteed by design.

Note 5: $\Delta r_{DS(ON)} = \Delta r_{DS(ON)}MAX - \Delta r_{DS(ON)}MIN$

Note 6: Worst-case isolation is on channel 4 because of its proximity to the drain pin. Off isolation = $20\log_{10} V_D/V_S$, V_D = output, V_S = input to off switch.

Pin Description

DG408 PIN	NAME	FUNCTION
1,16,15	A0, A1, A2	Address Inputs
2	EN	Enable Input
3	V-	Negative Supply Voltage Input
4-7, 12-9	S1-S8	Source Outputs
8	D	Drain Output
13	V+	Positive Supply Voltage Input
14	GND	Ground

DG409 PIN	NAME	FUNCTION
1,16	A0, A1	Address Inputs
2	EN	Enable Input
3	V-	Negative Supply Voltage Input
4-7	S1a-S4a	Source Outputs
8,9	Da, Db	Drain Outputs
13-10	S1b-S4b	Source Outputs
14	V+	Positive Supply Voltage Input
15	GND	Ground

8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

Truth Tables

DG408

A2	A1	A0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG409

A1	A0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

LOGIC "0" $V_{AL} \leq +0.8$ V, LOGIC "1" $V_{AH} \geq +2.4$ V

Timing Diagrams

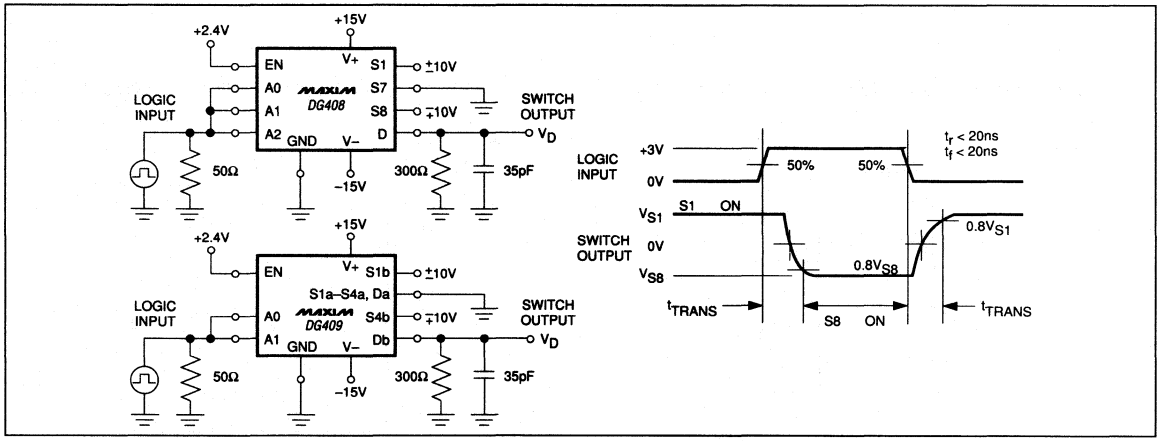


Figure 1. Transition-Time Test Circuit

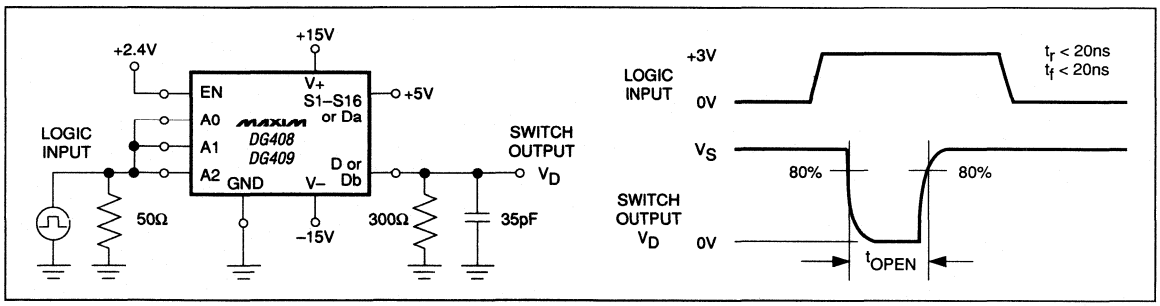


Figure 2. Break-Before-Make Interval Test Circuit

8-Channel/Dual 4-Channel High Performance CMOS Analog Multiplexers

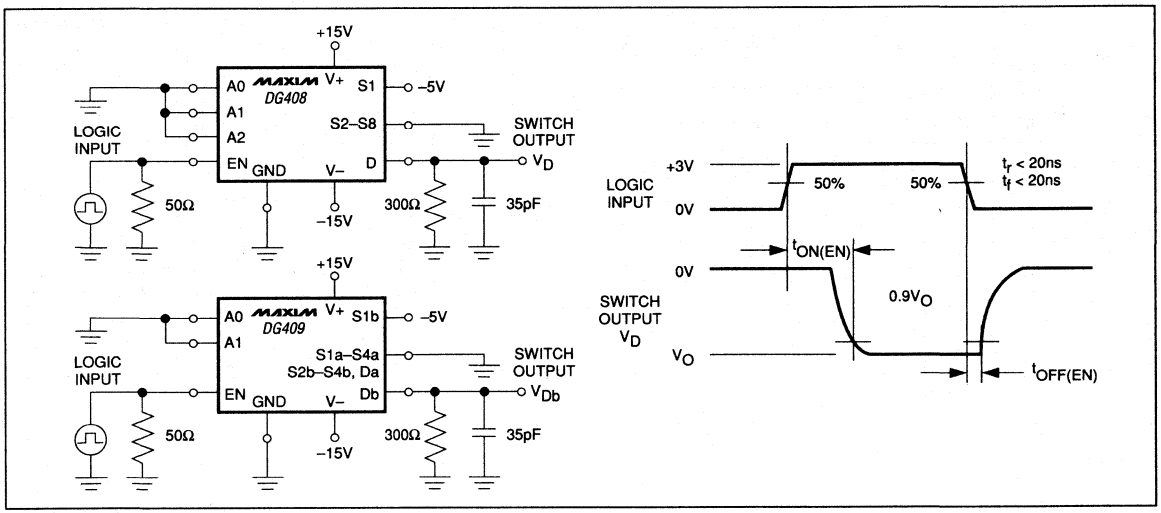
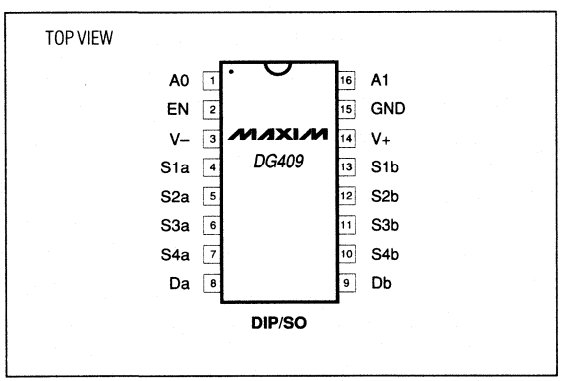
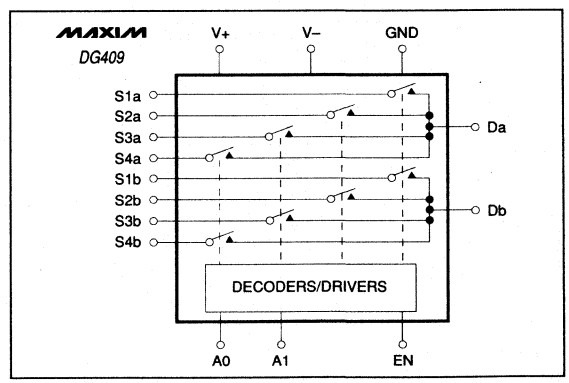


Figure 3. $t_{ON(EN)}$, $t_{OFF(EN)}$ Test Circuit

Pin Configurations (continued)



Functional Diagrams (continued)



19-4728; Rev. 0; 12/91

MAXIM

Quad SPST Precision Analog Switches

General Description

The DG411/DG412/DG413 are quad, single-pole-single-throw (SPST) precision analog switches. The DG411 is normally closed (SPST, NC), while the DG412 is normally open (SPST, NO). The DG413 has two normally open and two normally closed switches. All three parts offer low on resistance (less than 35Ω), low leakage (less than 250pA), and fast switching times – turn-on time less than 175ns and turn-off time less than 145ns.

The DG411/DG412/DG413 are fabricated with Maxim's new improved silicon gate process. And a 44V maximum breakdown voltage allows rail-to-rail switch-off blocking capability.

These devices can be used with a single positive supply (+12V to +30V) or split supplies (±4.5V to ±20V) while retaining CMOS logic input compatibility and fast switching. CMOS inputs provide reduced input loading and very low leakage currents.

Applications

Sample-and-Hold Circuits
Guidance and Control Systems
Winchester Disk Drives
Heads-Up Displays
Test Equipment
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

Features

- ◆ $r_{DS(ON)}$ < 35Ω
- ◆ Leakage < 250pA
- ◆ Single- or Bipolar-Supply Operation
- ◆ TTL/CMOS Logic Compatible
- ◆ Rail-to-Rail Switch-Off Blocking Capability
- ◆ Monolithic, Low-Power Design

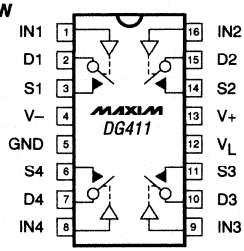
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
DG411C/D	0°C to +70°C	Dice*
DG411DJ	-40°C to +85°C	16 Plastic DIP
DG411DY	-40°C to +85°C	16 Narrow SO
DG411DK	-40°C to +85°C	16 CERDIP
DG411AK	-55°C to +125°C	16 CERDIP**
DG412C/D	0°C to +70°C	Dice*
DG412DJ	-40°C to +85°C	16 Plastic DIP
DG412DY	-40°C to +85°C	16 Narrow SO
DG412DK	-40°C to +85°C	16 CERDIP
DG412AK	-55°C to +125°C	16 CERDIP**
DG413C/D	0°C to +70°C	Dice*
DG413DJ	-40°C to +85°C	16 Plastic DIP
DG413DY	-40°C to +85°C	16 Narrow SO
DG413DK	-40°C to +85°C	16 CERDIP
DG413AK	-55°C to +125°C	16 CERDIP**

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

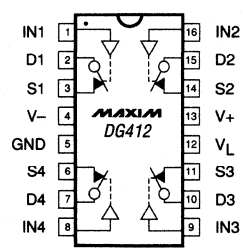
Pin Configurations/Functional Diagrams

TOP VIEW



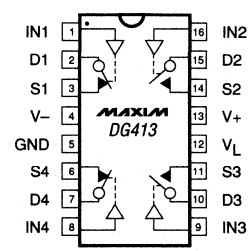
DIP/SO

LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

LOGIC	SWITCH 1, 4	SWITCH 2, 3
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC "1" INPUT

Quad SPST Precision Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
V_L ..... (GND -0.3V) to (V+ +0.3V)
Digital Inputs V_S, V_D (Note 1) ..... (V- -2V) to (V+ +2V) or 30mA (whichever occurs first)
Current (any terminal) 30mA
Peak Current, S or D
(pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C) (Note 2)
16-Pin Plastic DIP (derate 7.5mW/°C above +70°C) ... 470mW
16-Pin Narrow SO (derate 8.7mW/°C above +70°C) ... 696mW
16-Pin CERDIP (derate 10mW/°C above +70°C) 900mW
Operating Temperature Ranges:
DG41_C_ ..... 0°C to +70°C
DG41_D_ ..... -40°C to +85°C
DG41_AK ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Signals on Sx, Dx, or INx exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current rating.

Note 2: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Dual Supplies)

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 3)			–15		15	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = –10mA, V_D = 8.5V or –8.5V, V+ = 13.5V, V– = –13.5V		T_A = +25°C		25	35	Ω
				T_A = T_{MIN} to T_{MAX}			45	
$r_{DS(ON)}$ Matching Between Channels	$\Delta r_{DS(ON)}$	V_D = ±10V, (Note 4), I_S = –10mA, V+ = 13.5V, V– = –13.5V		T_A = +25°C			15	Ω
Source-Off Leakage Current	$I_{S(OFF)}$	V_D = –15.5V, V_S = 15.5V, V+ = 16.5V, V– = –16.5V		T_A = +25°C	–0.25	–0.10	0.25	nA
				T_A = T_{MIN} to T_{MAX}	–20		20	
Drain-Off Leakage Current	$I_{D(OFF)}$	V_S = –15.5V, V_D = 15.5V, V+ = 16.5V, V– = –16.5V		T_A = +25°C	–0.25	–0.10	0.25	nA
				T_A = T_{MIN} to T_{MAX}	–20		20	
Drain-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_S = ±15.5V, V_D = ∓15.5V, V+ = 16.5V, V– = –16.5V		T_A = +25°C	–0.4	–0.1	0.4	nA
				T_A = T_{MIN} to T_{MAX}	–40		40	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX (Note 2)	UNITS
INPUT								
Input Current with Input Voltage High	I_{INH}	IN_ = 2.4V, all others = 0.8V			–0.500	0.005	0.500	µA
Input Current with Input Voltage Low	I_{INL}	IN_ = 0.8V all others = 2.4V			–0.500	0.005	0.500	µA
SUPPLY								
Power-Supply Range					±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V– = –16.5V		T_A = +25°C		0.0001	1	µA
				T_A = T_{MIN} to T_{MAX}			5	
Negative Supply Current	I–	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V– = –16.5V		T_A = +25°C	–1	–0.0001		µA
				T_A = T_{MIN} to T_{MAX}	–5			
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V– = –16.5V		T_A = +25°C		0.0001	1	µA
				T_A = T_{MIN} to T_{MAX}			5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V V+ = 16.5V, V– = –16.5V		T_A = +25°C	–1	–0.0001		µA
				T_A = T_{MIN} to T_{MAX}	–5			
DYNAMIC								
Turn-On Time	t_{ON}	Figure 1, V_S = ±10V		T_A = +25°C		110	175	ns
				T_A = T_{MIN} to T_{MAX}			220	
Turn-Off Time	t_{OFF}	Figure 1, V_S = ±10V		T_A = +25°C		100	145	ns
				T_A = T_{MIN} to T_{MAX}			160	
Break-Before-Make Time Delay	t_D	DG413 Only, Figure 2, R_L = 300Ω, C_L = 35pF		T_A = +25°C		25		ns
Charge Injection	Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 3		T_A = +25°C		5		pC
Off Isolation (Note 5)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 4		T_A = +25°C		68		dB
Crosstalk (Note 6)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5		T_A = +25°C		85		dB
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 6		T_A = +25°C		9		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 6		T_A = +25°C		9		pF
Channel-On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	f = 1MHz, Figure 7		T_A = +25°C		35		pF

Quad SPST Precision Analog Switches

ELECTRICAL CHARACTERISTICS (Single Supply)

(V+ = 12V, V- = 0V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 3)			0		12	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = –10mA, V_D = 3.8V, V+ = 10.8V		T_A = +25°C		40	80	Ω
				T_A = T_{MIN} to T_{MAX}			100	
SUPPLY								
Positive Supply Current	I+	V+ = 13.2V, All channels on or off, V_{IN} = 0V or 5V,		T_A = +25°C		0.0001	1	µA
				T_A = T_{MAX}			5	
Negative Supply Current	I–	V+ = 13.2V, All channels on or off, V_{IN} = 0V or 5V		T_A = +25°C	–1	0.0001		µA
				T_A = T_{MAX}	–5			
Logic Supply Current	I_L	V_L = 5.25V, All channels on or off, V_{IN} = 0V or 5V		T_A = +25°C		0.0001	1	µA
				T_A = T_{MAX}			5	
Ground Current	I_{GND}	V_L = 5.25V, All channels on or off, V_{IN} = 0V or 5V		T_A = +25°C	–1	–0.0001		µA
				T_A = T_{MAX}	–5			
DYNAMIC								
Turn-On Time	t_{ON}	Figure 1, V_S = 8V		T_A = +25°C		175	250	ns
				T_A = T_{MIN} to T_{MAX}			315	
Turn-Off Time	t_{OFF}	Figure 1, V_S = 8V		T_A = +25°C		95	125	ns
				T_A = T_{MIN} to T_{MAX}			140	
Break-Before-Make Time Delay	t_D	DG413 Only, Figure 2, R_L = 300Ω, C_L = 35pF		T_A = +25°C		25		ns
Charge Injection	Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 7		T_A = +25°C		25		pC

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta r_{DS(ON)} = \Delta r_{DS(ON)}$ MAX – $\Delta r_{DS(ON)}$ MIN.

Note 5: See Figure 4. Off Isolation = $20\log_{10} V_D/V_S$, V_D = output, V_S = input to off switch.

Note 6: Between any two switches. See Figure 5.

Pin Description

PIN	NAME	FUNCTION
1,8,9,16	IN1-IN4	Inputs
2,7,10,15	D1-D4	Drain Outputs
3,6,11,14	S1-S4	Source Outputs
4	V-	Negative Supply Voltage Input
5	GND	Ground
12	V_L	Logic Supply Voltage
13	V+	Positive Supply Voltage Input – connected to substrate.

Test Circuits/Timing Diagrams

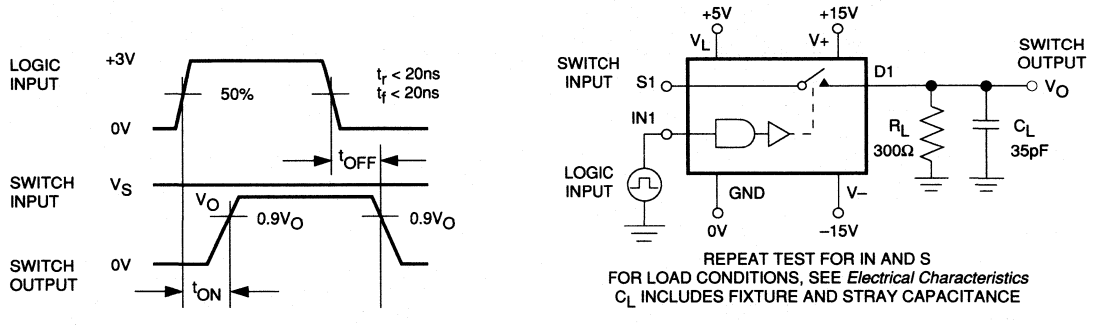


Figure 1. Switching-Time Test Circuit

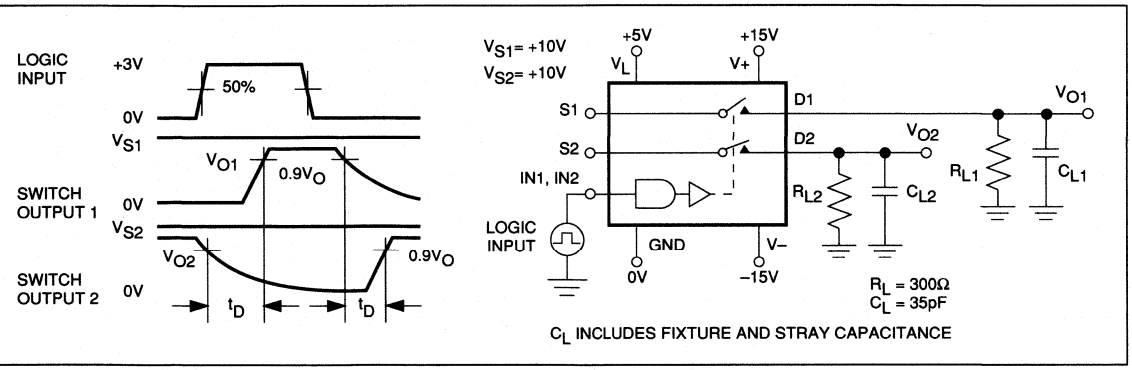


Figure 2. Break-Before-Make Test Circuit

QUAD SPST Precision Analog Switches

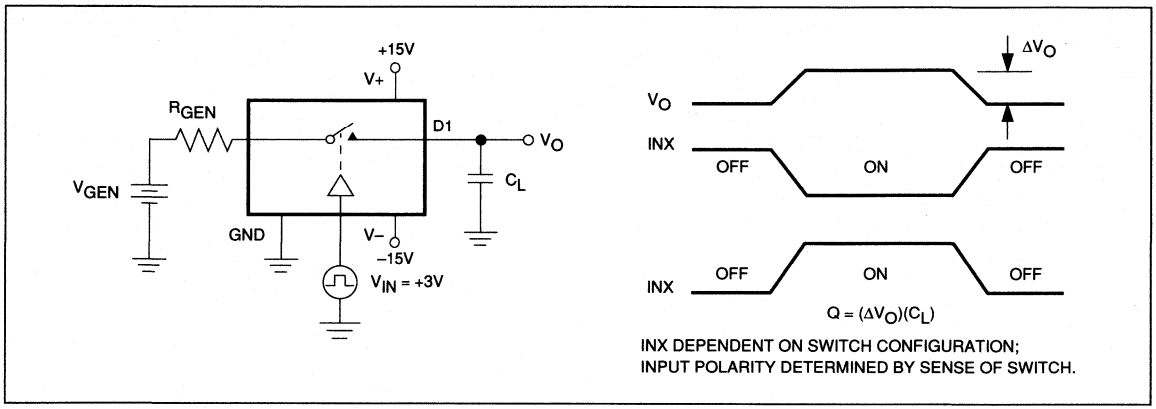


Figure 3. Charge-Injection Test Circuit

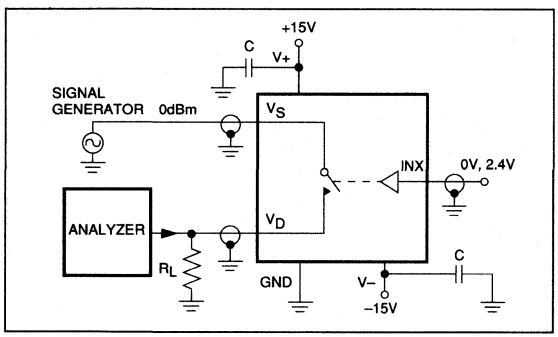


Figure 4. Off-Isolation Test Circuit

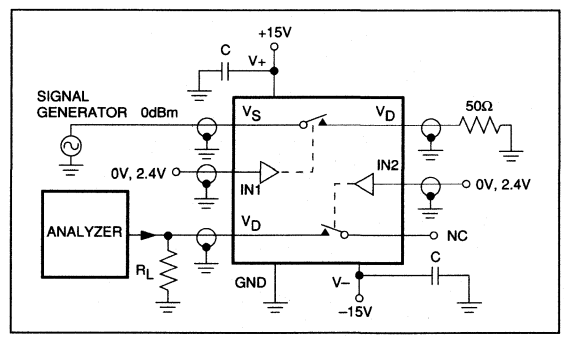


Figure 5. Crosstalk Test Circuit

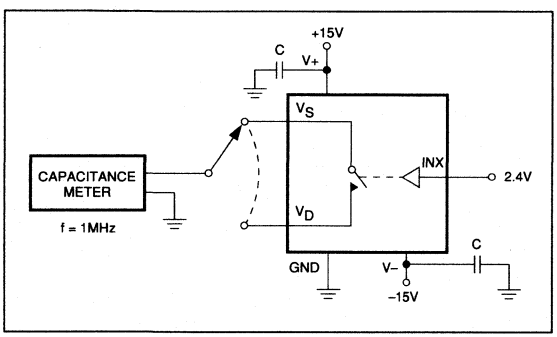


Figure 6. Channel-Off Capacitance Test Circuit

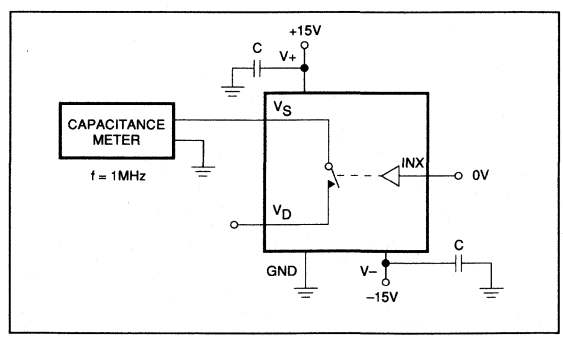


Figure 7. Channel-On Capacitance Test Circuit

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

Precision MiniDIP CMOS Analog Switches

General Description

The DG417/DG418/DG419 are precision CMOS analog switches. The DG417 is normally closed (SPST, NC), while the DG418 is normally open (SPST, NO). The DG419 has one normally open and one normally closed switch (SPDT). All three parts offer low on resistance (less than 35W), low leakage (less than 250pA), and fast switching times – turn-on time less than 175ns and turn-off time less than 145ns.

The DG417/DG418/DG419 are fabricated with Maxim's new improved silicon gate process. And a 44V maximum breakdown voltage allows rail-to-rail switch-off blocking capability.

Features

- ♦ **$r_{DS(ON)}$ < 35W**
- ♦ **Leakage < 250pA**
- ♦ **TTL-/CMOS-Logic Compatible**
- ♦ **Rail-to-Rail Switch-Off Blocking Capability**
- ♦ **Monolithic, Low-Power Design**

Applications

Sample-and-Hold Circuits

Guidance and Control Systems

Winchester Disk Drives

Heads-Up Displays

Test Equipment

Military Radios

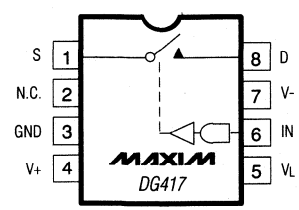
Communications Systems

Battery-Powered Systems

PBX, PABX

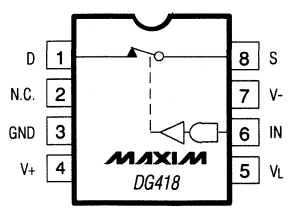
Pin Configurations/Functional Diagrams

TOP VIEW



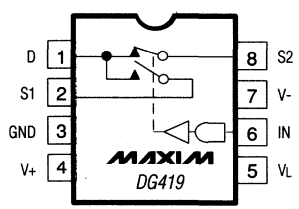
DIP

LOGIC	SWITCH
0	ON
1	OFF



DIP

LOGIC	SWITCH
0	OFF
1	ON



DIP

LOGIC	SWITCH 1	SWITCH 2
0	ON	OFF
1	OFF	ON

SWITCHES SHOWN FOR LOGIC "1" INPUT; LOGIC "0" ≤ 0.8V, LOGIC "1" ≥ 2.4V

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

Low-Power, High-Speed, Latchable CMOS Analog Switches

General Description

The DG421/DG423/DG425 are latchable CMOS analog switches. The DG421 has two normally open switches (SPST, NO). The DG423 (SPDT) has one normally open and one normally closed switch per pair, as does the DG425 (DPST). All three parts offer low on resistance (less than 35Ω), low leakage (less than 250pA), and fast switching times – turn-on time less than 250ns and turn-off time less than 200ns.

The DG421/DG423/DG425 are fabricated with Maxim's new improved silicon gate process. And a 44V maximum breakdown voltage allows rail-to-rail switch-off blocking capability.

The latch is transparent when $\overline{WR}$ is low. When $\overline{WR}$ is high, the latches store the logic control data. A low on $\overline{RS}$ resets all switches to their default state.

Applications

Sample-and-Hold Circuits

Guidance and Control Systems

Winchester Disk Drives

Heads-Up Displays

Test Equipment

Military Radios

Communications Systems

Battery-Powered Systems

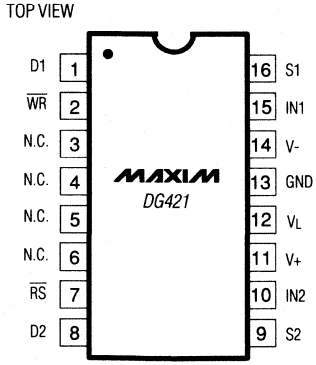
PBX, PABX

Features

- ♦ $r_{DS(ON)}$ < 35Ω
- ♦ Leakage < 250pA
- ♦ TTL-/CMOS-Logic Compatible
- ♦ Rail-to-Rail Switch-Off Blocking Capability
- ♦ Monolithic, Low-Power Design

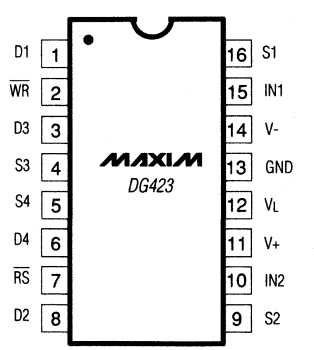
Pin Configurations

TOP VIEW



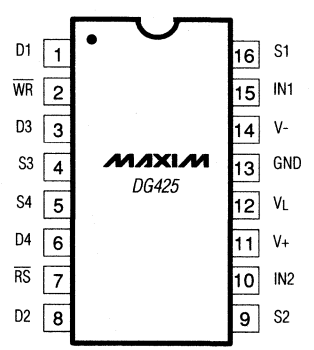
DIP

WR	RS	INx	SWITCH
0	1	0	OFF
		1	ON



DIP

WR	RS	INx	SWITCH 1, 2	SWITCH 3, 4
0	1	0	OFF	ON
		1	ON	OFF



DIP

WR	RS	INx	SWITCH
0	1	0	OFF
		1	ON

LOGIC "0" ≤ 0.8V, LOGIC "1" ≥ 2.4V

19-4611; Rev 0; 12/91

MAXIM

QUAD SPST Analog Switches

General Description

The DG441/DG442 are quad single-pole-single-throw (SPST) analog switches. The DG441 is normally closed (SPST, NC), while the DG442 is normally open (SPST, NO). Both parts offer low channel on resistance (less than 85Ω), low leakage (less than 500pA), and fast switching – turn-on time less than 250ns, and turn-off time less than 170ns.

The DG441/DG442 are fabricated with Maxim's new improved 44V CMOS process. Design improvements yield reduced charge injection and low power consumption. The 44V maximum breakdown voltage allows rail-to-rail switch-off blocking capability.

The DG441/DG442 operate with a single positive supply (+12V to +30V) or split supplies (±4.5V to ±20V) while retaining CMOS logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits
Guidance and Control Systems
Winchester Disk Drives
Heads-Up Displays
Test Equipment
Communications Systems
Battery-Operated Systems
PBX, PABX

Features

- **$r_{DS(ON)}$ < 85Ω**
- **Leakage < 500pA**
- **Single-Supply Operation (+12V to +30V)**
  Bipolar-Supply Operation (±4.5V to ±20V)
- **TTL/CMOS Logic Compatible**
- **Rail-to-Rail Switch-Off Blocking Capability**

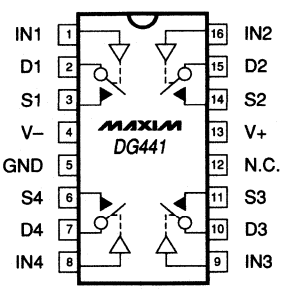
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
DG441C/D	0°C to +70°C	Dice*
DG441DJ	-40°C to +85°C	16 Plastic DIP
DG441DY	-40°C to +85°C	16 Narrow SO
DG441DK	-40°C to +85°C	16 CERDIP
DG441AK	-55°C to +125°C	16 CERDIP**
DG442C/D	0°C to +70°C	Dice*
DG442DJ	-40°C to +85°C	16 Plastic DIP
DG442DY	-40°C to +85°C	16 Narrow SO
DG442DK	-40°C to +85°C	16 CERDIP
DG442AK	-55°C to +125°C	16 CERDIP**

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

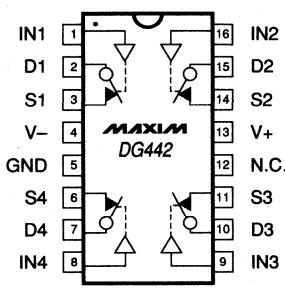
Pin Configurations/Functional Diagrams

TOP VIEW



DIP/SO

LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

LOGIC	SWITCH
0	OFF
1	ON

SWITCHES SHOWN FOR LOGIC "1" INPUT

QUAD SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
Digital Inputs V_S, V_D ..... V- -2V to V+ +2V or 30mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Peak Current, S or D
(pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C) (Note 1)
16-Pin Plastic DIP (derate 7.5mW/°C above +70°C) ..593mW
16-Pin Narrow SO (derate 8.7mW/°C above +70°C) ..696mW
16-Pin CERDIP (derate 10mW/°C above +70°C) 800mW
Operating Temperature Ranges:
DG441C/DG442C ..... 0°C to +70°C
DG441D/DG442D ..... -40°C to +85°C
DG441AK/DG442AK ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Dual Supplies)

(V+ = 15V, V- = -15V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog-Signal Range	V_{ANALOG}	(Note 3)		–15		15	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = –10mA V_D = 8.5V or –8.5V, V+ = 13.5V, V– = –13.5V	T_A = +25°C		50	85	Ω
			T_A = T_{MIN} to T_{MAX}			100	
Source-Off Leakage Current	$I_{S(OFF)}$	V_D = ±15.5V V_S = ∓15.5V V+ = 16.5V, V– = –16.5V	T_A = +25°C	–0.50	0.01	0.50	nA
			T_A = T_{MAX}	–20		20	
Drain-Off Leakage Current	$I_{D(OFF)}$	V_S = ±15.5V V_D = ∓15.5V V+ = 16.5V, V– = –16.5V	T_A = +25°C	–0.50	0.01	0.50	nA
			T_A = T_{MAX}	–20		20	
Drain-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = ±15.5V V_S = ±15.5V V+ = 16.5V, V– = –16.5V	T_A = +25°C	–0.50	0.08	0.50	nA
			T_A = T_{MAX}	–40		40	
INPUT							
Input Current with Input Voltage High	I_{INH}	$V_{IN\_}$ = 2.4V, all others = 0.8V		–500	0.01	500	nA
Input Current with Input Voltage Low	I_{INL}	$V_{IN\_}$ = 0.8V, all others 2.4V		–500	0.01	500	nA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SUPPLY							
Power-Supply Range				±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V– = –16.5V	T_A = T_{MIN} to T_{MAX}		15	100	µA
Negative Supply Current	I–	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C	–1	–0.0001		µA
			T_A = T_{MIN} to T_{MAX}	–5			
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V– = –16.5V	T_A = T_{MIN} to T_{MAX}	–100	–15		µA
DYNAMIC							
Turn-On Time	t_{ON}	Figure 1, V_S = ±10V, R_L = 1kΩ	T_A = +25°C		150	250	ns
Turn-Off Time	t_{OFF}	DG441, Figure 1, V_S = ±10V	T_A = +25°C		90	120	ns
		DG442, Figure 1, V_S = ±10V	T_A = +25°C		110	170	ns
Charge Injection	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 2	T_A = +25°C		–1		pC
Off Isolation (Note 4)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 3	T_A = +25°C		60		dB
Crosstalk (Note 5)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 4	T_A = +25°C		–100		dB
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 5	T_A = +25°C		4		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 5	T_A = +25°C		4		pF
Channel-On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	f = 1MHz, Figure 5	T_A = +25°C		16		pF

QUAD SPST Analog Switches

ELECTRICAL CHARACTERISTICS (Single Supply)

(V+ = 12V, V- = 0V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog-Signal Range	V_{ANALOG}	(Note 3)		0		12	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = –10mA, V_D = 3V, 8V, V+ = 10.8V	T_A = +25°C		100	160	Ω
			$T_A = T_{MIN}$ to T_{MAX}			200	
SUPPLY							
Power-Supply Range				0		12	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V			15	100	µA
Negative Supply Current	I–		T_A = +25°C	–1	–0.0001		
			$T_A = T_{MIN}$ to T_{MAX}	–5			
Ground Current	I_{GND}		$T_A = T_{MIN}$ to T_{MAX}	–100	–15		
DYNAMIC							
Turn-On Time	t_{ON}	Figure 1, V_S = 8V	T_A = +25°C		300	400	ns
Turn-Off Time	t_{OFF}	Figure 1, V_S = 8V	T_A = +25°C		60	200	ns
Charge Injection	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 2	T_A = +25°C		2		pC

Note 2. The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 3. Guaranteed by design.
Note 4. See Figure 3. Off Isolation = 20 $\log_{10} V_D/V_S$, V_D = output, V_S = input to off switch.
Note 5. Between any two switches. See Figure 4.

Pin Description

PIN	NAME	FUNCTION
1,16,9,8	IN1-IN4	Input
2,15,10,7	D1-D4	Drain Output
3,14,11,6	S1-S4	Source Output
4	V-	Negative Supply Voltage Input
5	GND	Ground
12	N.C.	No Connect
13	V+	Positive Supply Voltage Input – connected to substrate.

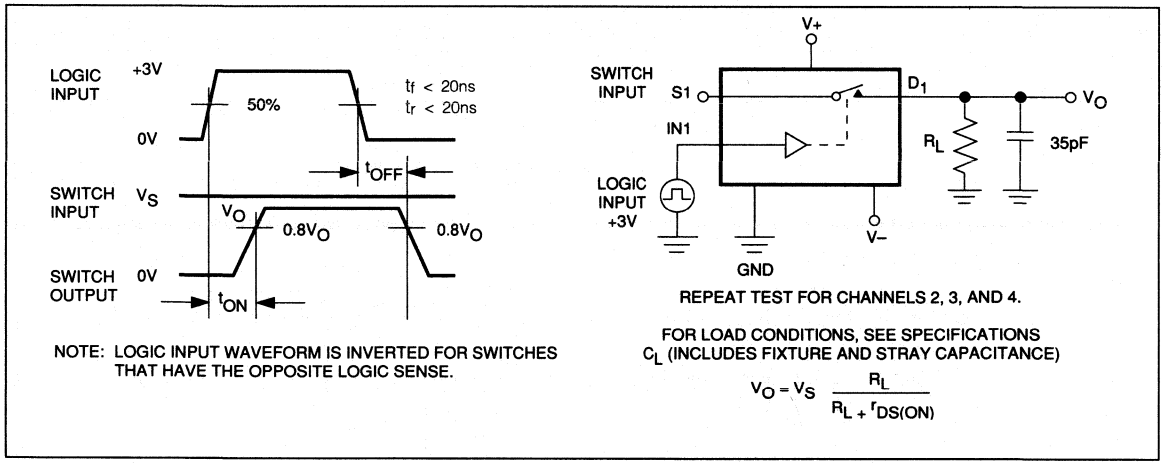


Figure 1. Switching-Time Test Circuit

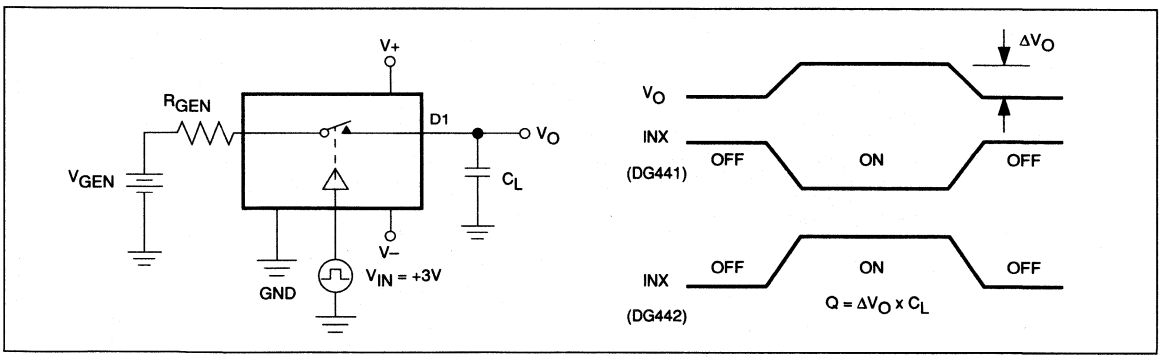


Figure 2. Charge-Injection Test Circuit

FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100Hz TO 13MHz	HP3330B AUTOMATIC SYNTHESIZER	HP3571A TRACKING SPECTRUM ANALYZER

$$\text{OFF ISOLATION} = 20\log\frac{V_S}{V_D}$$

C = 1µF TANTALUM IN PARALLEL WITH 0.01µF CERAMIC

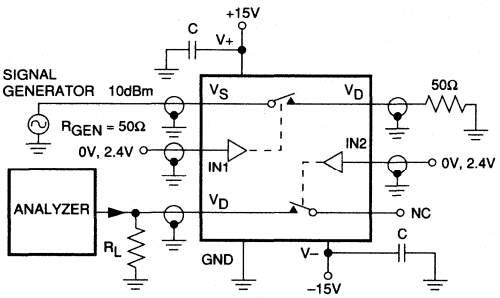


Figure 3. Crosstalk Test Circuit

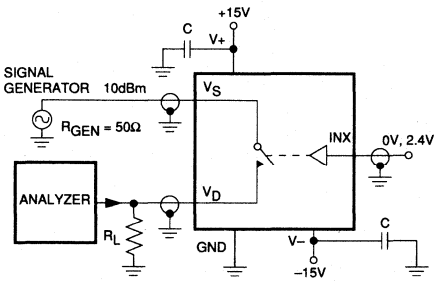


Figure 4. Off-Isolation Test Circuit

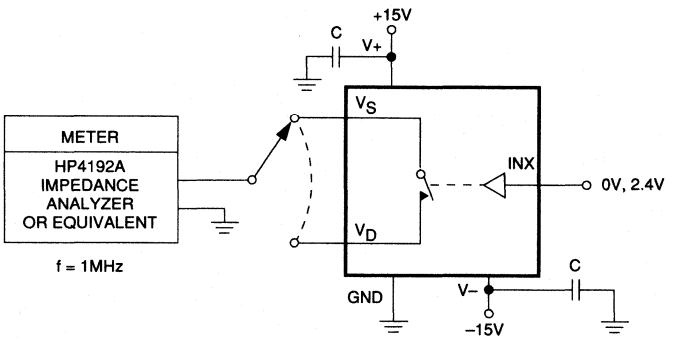


Figure 5. Channel Capacitance Test Circuit

19-4705; Rev 0; 12/91

MAXIM

QUAD SPST Analog Switches

General Description

The DG444/DG445 are quad single-pole-single-throw (SPST) analog switches. The DG444 is normally closed (SPST, NC), while the DG445 is normally open (SPST, NO). Both parts offer low resistance (less than 85Ω), low leakage (less than 500pA), and fast switching over the analog range – turn-on time less than 250ns, and turn-off time less than 170ns.

The DG444/DG445 are fabricated with Maxim's new improved 44V process. Design improvements yield reduced output spiking and low power consumption. The 44V maximum breakdown voltage allows rail-to-rail switch-off blocking capability.

These switches can be used with a single positive supply (+12V to +30V) or split supplies (±4.5V to ±20V) while retaining CMOS logic input compatibility and fast switching. CMOS inputs provide reduced input loading.

Applications

Sample-and-Hold Circuits
Guidance and Control Systems
Winchester Disk Drives
Heads-Up Displays
Test Equipment
Military Radios
Communications Systems
Battery-Operated Systems
PBX, PABX

Truth Table

FOUR SPST SWITCHES PER PACKAGE

LOGIC	SWITCH	
	DG444	DG445
0	ON	OFF
1	OFF	ON

LOGIC "0" ≤ 0.8 V
LOGIC "1" ≥ 2.4V

Features

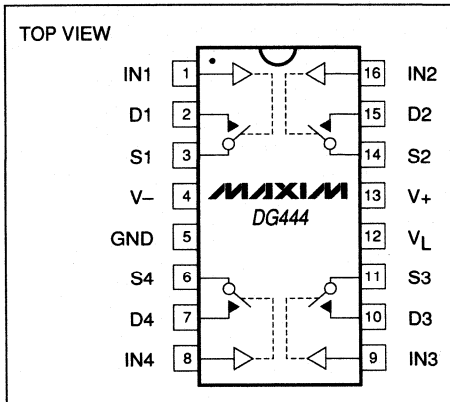
- ◆ $r_{DS(ON)}$ < 85Ω
- ◆ Leakage < 500pA
- ◆ Single-Supply Operation (+12V to +30V)
  Bipolar-Supply Operation (±4.5V to ±20V)
- ◆ CMOS/TTL Logic Compatible
- ◆ Rail-to-Rail Switch-Off Blocking Capability

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
DG444C/D	0°C to +70°C	Dice*
DG444DJ	-40°C to +85°C	16 Plastic DIP
DG444DY	-40°C to +85°C	16 Narrow SO
DG445C/D	0°C to +70°C	Dice*
DG445DJ	-40°C to +85°C	16 Plastic DIP
DG445DY	-40°C to +85°C	16 Narrow SO

* *Contact factory for dice specifications.*

Pin Configuration/ Functional Diagram



DIP/SO
SWITCHES SHOWN FOR LOGIC "1" INPUT

QUAD SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-

V+ 44V
GND 25V
V_L ..... GND -0.3V to V+ +0.3V
Digital Inputs V_S, V_D ..... V- -2V to V+ +2V or 30mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Peak Current, S or D
(pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C) (Note 1)
16-Pin Plastic DIP (derate 7.5mW/°C above +70°C) ..593mW
16-Pin Narrow SO (derate 8.7mW/°C above +70°C) ..696mW
Operating Temperature Ranges:
DG444C/DG445C ..... 0°C to +70°C
DG444D/DG445D ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: All leads are soldered or welded to PC board.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Dual Supplies)

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		–15		15	V
Drain-Source On Resistance	$r_{DS(ON)}$	I_S = –10mA, V_D = 8.5V or –8.5V, V+ = 13.5V, V– = –13.5V	T_A = +25°C		50	85	Ω
			T_A = T_{MIN} to T_{MAX}			100	
Source-Off Leakage Current	$I_{S(OFF)}$	V_D = ±15.5V, V_S = ∓15.5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C	–0.50	0.01	0.50	nA
			T_A = T_{MIN} to T_{MAX}	–20		20	
Drain-Off Leakage Current	$I_{D(OFF)}$	V_S = ±15.5V, V_D = ∓15.5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C	–0.50	0.01	0.50	nA
			T_A = T_{MIN} to T_{MAX}	–20		20	
Drain-On Leakage Current	$I_{D(ON)}$ + $I_{S(ON)}$	V_D = ±15.5V, V_S = ±15.5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C	–0.50	0.08	0.50	nA
			T_A = T_{MIN} to T_{MAX}	–40		40	
INPUT							
Input Current with Input Voltage High	I_{INH}	$V_{IN\_}$ = 2.4V, all others = 0.8V		–0.5	–0.00001	0.5	µA
Input Current with Input Voltage Low	I_{INL}	$V_{IN\_}$ = 0.8V, all others 2.4V		–0.5	0.00001	0.5	µA

ELECTRICAL CHARACTERISTICS (Dual Supplies) (continued)

V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX (Note 2)	UNITS
SUPPLY							
Power-Supply Range				±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C		0.001	1	µA
			T_A = T_{MIN} to T_{MAX}			5	
Negative Supply Current	I–	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C	–1	–0.0001		µA
			T_A = T_{MIN} to T_{MAX}	–5			
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C		0.001	1	µA
			T_A = T_{MIN} to T_{MAX}			5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V, V+ = 16.5V, V– = –16.5V	T_A = +25°C	–1	–0.0001		µA
			T_A = T_{MIN} to T_{MAX}	–5			
DYNAMIC							
Turn-On Time	t_{ON}	V_S = ±10V, Figure 1	T_A = +25°C		150	250	ns
Turn-Off Time	t_{OFF}	DG444, V_S = ±10V, Figure 1	T_A = +25°C		90	120	ns
		DG445, V_S = ±10V, Figure 1	T_A = +25°C		110	170	ns
Charge Injection	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 2	T_A = +25°C		–1		pC
Off Isolation (Note 4)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 3	T_A = +25°C		60		dB
Crosstalk (Note 5)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 4	T_A = +25°C		100		dB
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 5	T_A = +25°C		4		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 5	T_A = +25°C		4		pF
Channel-On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	f = 1MHz, Figure 5	T_A = +25°C		16		pF

QUAD SPST Analog Switches

ELECTRICAL CHARACTERISTICS (Single Supply)

(V+ = 12V, V- = 0V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		0		12	V
Drain-Source on Resistance	$r_{DS(ON)}$	I_S = –10mA, V_L = 5.25V, V_D = 3V, 8V, V+ = 10.8V	T_A = +25°C		100	160	Ω
			T_A = T_{MIN} to T_{MAX}			200	
SUPPLY							
Power-Supply Range				0		12	V
Positive Supply Current	I+	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C		0.001	1	µA
			T_A = T_{MIN} to T_{MAX}			5	
Negative Supply Current	I–	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	–1	–0.0001		µA
			T_A = T_{MIN} to T_{MAX}	–5			
Logic Supply Current	I_L	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C		0.001	1	µA
			T_A = T_{MIN} to T_{MAX}			5	
Ground Current	I_{GND}	All channels on or off, V_{IN} = 0V or 5V	T_A = +25°C	–1	–0.0001		µA
			T_A = T_{MIN} to T_{MAX}	–5			
DYNAMIC							
Turn-On Time	t_{ON}	V_S = 8V, Figure 1	T_A = +25°C		300	400	ns
Turn-Off Time	t_{OFF}	V_S = 8V, Figure 1	T_A = +25°C		60	200	ns
Charge Injection	Q	C_L = 1nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 2	T_A = +25°C		2		pC

Note 2. The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 3. Guaranteed by design.
Note 4. See Figure 3. Off Isolation = $20\log_{10} V_D/V_S$, V_D = output, V_S = input to off switch.
Note 5. Between any two switches. See Figure 4.

Pin Description

PIN	NAME	FUNCTION
1,16,9,8	IN1-IN4	Logic Control Inputs
2,15,10,7	D1-D4	Drain Outputs
3,14,11,6	S1-S4	Source Outputs
4	V-	Negative Supply Voltage Input
5	GND	Ground
12	V_L	Logic Supply Voltage Input
13	V+	Positive Supply Voltage Input – connected to substrate.

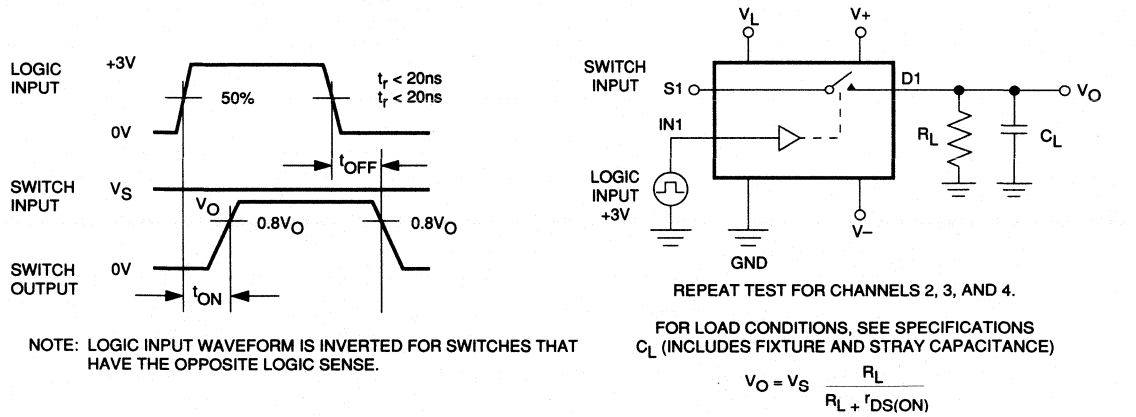


Figure 1. Switching-Time Test Circuit

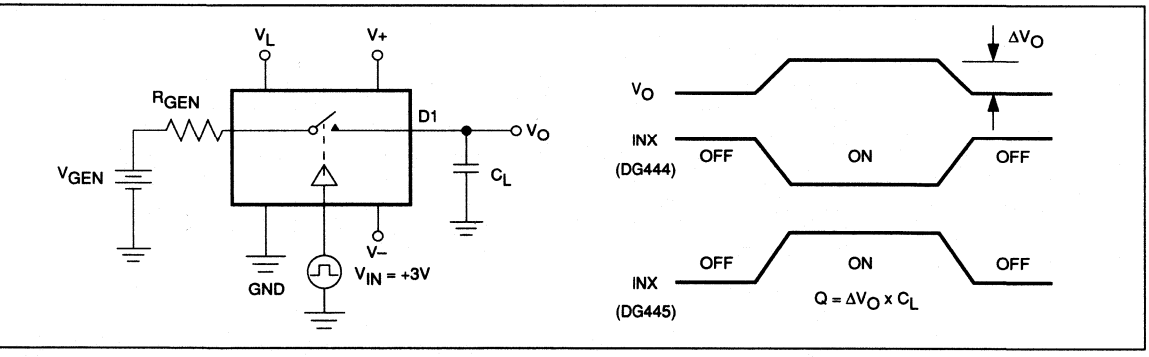


Figure 2. Charge-Injection Test Circuit

QUAD SPST Analog Switches

FREQUENCY TESTED	SIGNAL GENERATOR	ANALYZER
100Hz TO 13MHz	HP3330B AUTOMATIC SYNTHESIZER	HP3571A TRACKING SPECTRUM ANALYZER

C = 1µF TANTALUM IN PARALLEL WITH 0.01µF CERAMIC

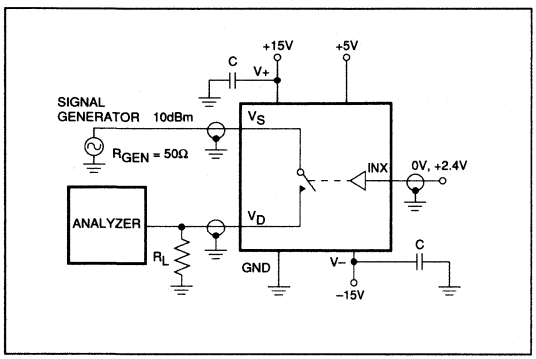


Figure 3. Off-Isolation Test Circuit

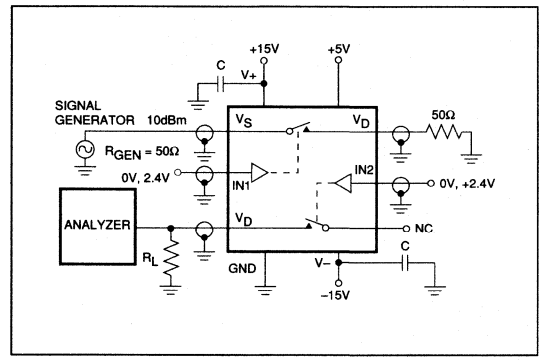


Figure 4. Crosstalk Test Circuit

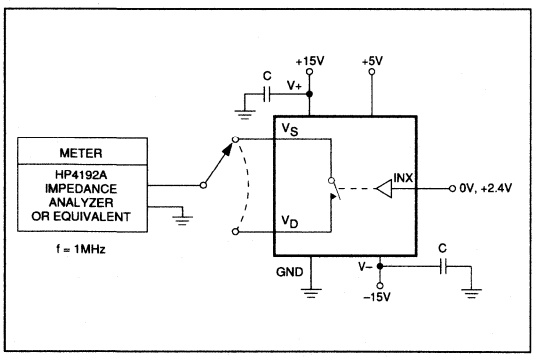


Figure 5. Source-/Drain-Off Capacitance

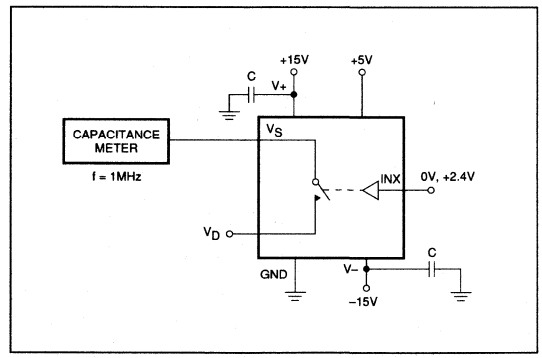


Figure 6. Source-/Drain-On Capacitance

MAXIM

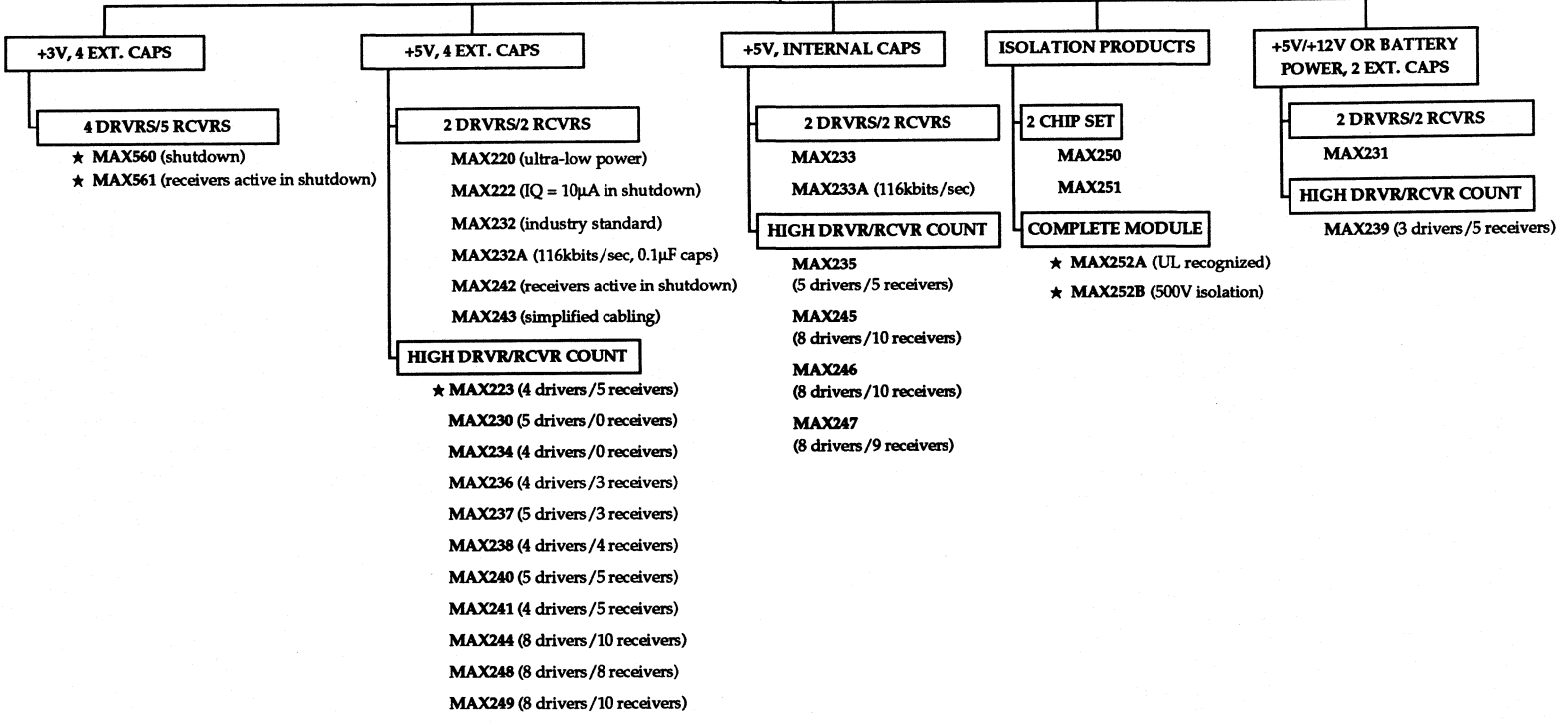
Interface Products

* Advance Information – first page of data sheet in preparation.

Part Number	Power Supply (V)	# of RS-232 Drivers	# of RS-232 Receivers	# of Ext. Caps	Nominal Cap. Value (µF)	Shutdown & 3-State	Supply Current (mA max)	Guaranteed Data Rate (kbits/sec max)	Features	Price† 1000-up ($)
MAX220	+5	2	2	4	4.7/10	No	2	20	Ultra low-power, industry-standard pinout	2.20
MAX222	+5	2	2	4	0.1	Yes	10	116	MAX232A with shutdown	2.20
MAX223	+5	4	5	4	1.0	Yes	15	20	+5V IBM PC serial port w/ receivers active in shutdown	3.29
MAX230 (MAX200)	+5	5	0	4	1.0	Yes	15 (20)	20	5 drivers with shutdown	3.29
MAX231	+5 and +7.5 to +13.2	2	2	2	1.0	No	1/5	20	Standard +5/+12V or battery supplies; same functions as MAX232	1.91
MAX232 (MAX202)	+5	2	2	4	1.0	No	10 (15)	20	Industry standard	1.91
MAX232A	+5	2	2	4	0.1	No	10	116	Higher slew rate, small caps	2.20
MAX233 (MAX203)	+5	2	2	0	-	No	10 (15)	20	No external caps	3.61
MAX233A	+5	2	2	0	-	No	10	116	No external caps, high slew rate	4.21
MAX234 (MAX204)	+5	4	0	4	1.0 (0.1)	No	15 (20)	20	Replaces 1488	3.10
MAX235 (MAX205)	+5	5	5	0	-	Yes	15 (20)	20	No external caps	6.34
MAX236 (MAX206)	+5	4	3	4	1.0 (0.1)	Yes	15 (20)	20	Shutdown, three-state	3.29
MAX237 (MAX207)	+5	5	3	4	1.0 (0.1)	No	15 (20)	20	Complements IBM PC serial port	3.29
MAX238 (MAX208)	+5	4	4	4	1.0 (0.1)	No	15 (20)	20	Replaces 1488 and 1489	3.29
MAX239 (MAX209)	+5 and +7.5 to +13.2	3	5	2	1.0 (0.1)	No	1/15 (20)	20	Standard +5/+12V or battery supplies; single package solution for IBM PC serial port	3.29
MAX240	+5	5	5	4	1.0	Yes	15	20	DIP or flatpak package	5.16
MAX241 (MAX211)	+5	4	5	4	1.0 (0.1)	Yes	15 (20)	20	Complete IBM PC serial port	3.29
MAX242	+5	2	2	4	0.1	Yes	10	116	Separate shutdown and enable	2.20
MAX243	+5	2	2	4	0.1	No	10	116	Open-line detection simplifies cabling	2.20
MAX244	+5	8	10	4	1.0	No	25	64	High slew rate	7.65
MAX245	+5	8	10	0	-	Yes	25	64	High slew rate, int. caps, two shutdown modes	12.15
MAX246	+5	8	10	0	-	Yes	25	64	High slew rate, int. caps, three shutdown modes	12.15
MAX247	+5	8	9	0	-	Yes	25	64	High slew rate, int. caps, nine operating modes	12.15
MAX248	+5	8	8	4	1.0	Yes	25	64	High slew rate, selective half-chip enables	7.65
MAX249	+5	6	10	4	1.0	Yes	25	64	MAX248 with 2 complete IBM PC serial ports	7.65
MAX560	+3	4	5	4	1.0	Yes	8	20	+3V MAX561 + receivers active in shutdown	3.29
MAX561	+3	4	5	4	1.0	Yes	8	20	+3V Complete IBM PC serial port	3.29
RS-232 ISOLATION PRODUCTS										
MAX250	+5	2	2	-	-	Yes	-	20	Isolated RS-232 chipset	3.20
MAX251	+5	2	2	-	-	Yes	-	20	Isolated RS-232 chipset	3.20
MAX252A	+5	2	2	0	-	Yes	90	9.6	UL recognized, 1500V isolation	45.91
MAX252B	+5	2	2	0	-	Yes	90	9.6	Economical 500V isolation	27.14

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

RS-232 LINE DRIVERS/RECEIVERS



★ New product since the publication of the 1990 Short Form Product Guide.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

+5V RS-232 Transceivers with 0.1µF External Capacitors

General Description

The MAX200-MAX211 transceivers are designed for RS-232 and V.28 communication interfaces where ±12V supplies are not available. On-board charge pumps convert the +5V input to the ±10V needed for RS-232 output levels. The MAX200-MAX211 drivers and receivers meet all EIA/TIA-232E and CCITT V.28 specifications at a data rate of 20kbits/sec. The drivers maintain the ±5V EIA/TIA-232E output signal levels at data rates in excess of 120kbits/sec when loaded in accordance with the EIA/TIA-232E specification.

The low-power shutdown mode of the MAX200, MAX206, and MAX211 is useful in battery-powered systems since power dissipation is reduced to less than 5µW. The MAX203 and MAX205 use no external components and are recommended for applications where printed circuit board space is critical.

The MAX211 is available in a 28-pin wide small outline (SO) package and a 28-pin shrink small-outline package (SSOP), which uses 60% less area than the SO.

Applications

Computers
Laptops, Palmtops, Notebooks

Battery-Powered Equipment

Hand-Held Equipment

Features

Superior to Bipolar:

- ♦ **0.1µF External Capacitors**
- ♦ **116kbits/sec Data Rate**
- ♦ **Single +5V Supply Operation**
- ♦ **Small 28-Pin SSOP Package - Uses 60% Less Area than SO**
- ♦ **Low-Power Shutdown Current, <1µA**
- ♦ **Designed for RS-232 and V.28 Applications**
- ♦ **Three-State TTL/CMOS Receiver Outputs**

Selection Table

Part Number	Power-Supply Voltage (V)	No. of RS-232 Drivers	No. of RS-232 Receivers	External Capacitors (0.1µF)	Low-Power Shutdown/ TTL Three -State
MAX200	+5	5	0	4	Yes/No
MAX202	+5	2	2	4	No/No
MAX203	+5	2	2	None	No/No
MAX204	+5	4	0	4	No/No
MAX205	+5	5	5	None	Yes/Yes
MAX206	+5	4	3	4	Yes/Yes
MAX207	+5	5	3	4	No/No
MAX208	+5	4	4	4	No/No
MAX211	+5	4	5	4	Yes/Yes

+5V RS-232 Transceivers with 0.1µF External Capacitors

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +14V
V- ..... +0.3V to -14V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V+ + 0.3V) to (V- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration
T_{OUT} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) 842mW
16-Pin SO (derate 8.70mW/°C above +70°C) 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) .. 800mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) .. 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) .. 889mW
24-Pin Narrow Plastic DIP (derate 8.70mW/°C above +70°C) . 696mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C) .. 941mW
24-Pin CERDIP (derate 12.50mW/°C above +70°C) . 1000mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) . 1000mW
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
44-Pin Plastic FP (derate 11.11mW/°C above +70°C . 889mW
Operating Temperature Ranges:
MAX2__C__ ..... 0°C to +70°C
MAX2__E__ ..... -40°C to +85°C
MAX2__M__ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(MAX202/204/206/207/208/211 V_{CC} = 5V ±10%, MAX203/MAX205 V_{CC} = 5V ±5%, C1 = C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground	±5	±9		V
V_{CC} Power-Supply Current	MAX202, MAX203, no load, T_A = +25°C		8	15	mA
	MAX200, MAX204-MAX208, MAX211		9	20	
Shutdown Supply Current	Figure 1, T_A = +25°C		1	10	µA
Input Logic Threshold Low	T_{IN}, $\overline{EN}$, SHDN			0.8	V
Input Logic Threshold High	T_{IN}	2.0			V
	$\overline{EN}$, SHDN	2.4			
Logic Pull-Up Current	T_{IN} = 0V		15	200	µA
RS-232 Input Voltage Operating Range		-30		+30	V
RS-232 Input Threshold Low	V_{CC} = 5V, T_A = +25°C	0.8	1.2		V
RS-232 Input Threshold High	V_{CC} = 5V, T_A = +25°C		1.7	2.4	V
RS-232 Input Hysteresis	V_{CC} = 5V	0.2	0.5	1.0	V
RS-232 Input Resistance	V_{CC} = 5V, T_A = +25°C	3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 1.6mA (MAX202, MAX203), I_{OUT} = 3.2mA (all others)			0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA	3.5			V
TTL/CMOS Output Leakage Current	$\overline{EN}$ = V_{CC}, 0V ≤ R_{OUT} ≤ V_{CC}		0.05	±10	µA
Output Enable Time (Figure 2)	MAX205, MAX206, MAX211		1000		ns
Output Disable Time (Figure 2)	MAX205, MAX206, MAX211		350		ns
Propagation Delay	RS-232 to TTL		0.4		µs

ELECTRICAL CHARACTERISTICS (continued)

(MAX202/204/206/207/208/211 V_{CC} = 5V ±10%, MAX203/MAX205 V_{CC} = 5V ±5%, C1 = C4 = 0.1μF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300			Ω
Transition Region Slew Rate	MAX200, MAX204-MAX211 C_L = 50pF to 2500pF R_L = 3kΩ to 7kΩ V_{CC} = 5V, T_A = +25°C measured from +3V to -3V or -3V to +3V	3	5.5	30	V/μs
	MAX202, MAX203 C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ V_{CC} = 5V, T_A = +25°C measured from +3V to -3V or -3V to +3V		4	30	
RS-232 Output Short-Circuit Current			±10	±45	mA

19-4323; Rev 2; 7/92

MAXIM

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

General Description

The MAX220-MAX249 family of line drivers/receivers is intended for all EIA-232E and V.28/V.24 communications interfaces, and in particular, for those applications where ±12V is not available.

These parts are particulary useful in battery-powered systems since their low-power shutdown mode reduces power dissipation to less than 5µW. The MAX233, MAX235 and MAX245-MAX247 use no external components and are recommended for applications where printed circuit board space is critical.

All members of the family except the MAX231 and MAX239 need only a single +5V supply for operation. The RS-232 drivers/receivers have on-board charge-pump voltage converters which convert the +5V input power to the ±10V needed to generate the RS-232 output levels. The MAX231 and MAX239, designed to operate from +5V and +12V, contain a +12V to -12V charge-pump voltage converter.

Since nearly all RS-232 applications need both line drivers and receivers, the family includes both receivers and drivers in one package. The wide variety of RS-232 applications require differing numbers of drivers and receivers. Maxim offers a wide selection of RS-232 driver/receiver combinations in order to minimize the package count (see *Selection Guide*).

Applications

Portable Computers

Low-Power Modems

Interface Translation

Battery-Powered RS-232 Systems

Multi-Drop RS-232 Networks

Features

Superior to Bipolar

- **Operate from Single +5V Power Supply (+5V and +12V – MAX231 and MAX239)**
- **Low-Power Receive Mode in Shutdown (MAX223/MAX242)**
- **Meet All EIA-232E and V.28 Specifications**
- **Multiple Drivers and Receivers**
- **3-State Driver and Receiver Outputs**
- **Open-Line Detection (MAX243)**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX220CPE	0°C to +70°C	16 Plastic DIP
MAX220CSE	0°C to +70°C	16 Narrow SO
MAX220CWE	0°C to +70°C	16 Wide SO
MAX220C/D	0°C to +70°C	Dice*
MAX220EPE	-40°C to +85°C	16 Plastic DIP
MAX220ESE	-40°C to +85°C	16 Narrow SO
MAX220EWE	-40°C to +85°C	16 Wide SO
MAX220MJE	-55°C to +125°C	16 CERDIP
MAX222CPN	0°C to +70°C	18 Plastic DIP
MAX222CWN	0°C to +70°C	18 Wide SO
MAX222C/D	0°C to +70°C	Dice*
MAX222EPN	-40°C to +85°C	18 Plastic DIP
MAX222EWN	-40°C to +85°C	18 Wide SO
MAX222EJN	-40°C to +85°C	18 CERDIP
MAX222MJN	-55°C to +125°C	18 CERDIP

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

Interface Products

Part Number	Power Supply (V)	# of RS-232 Drivers	# of RS-232 Receivers	# of Ext. Caps	Nominal Cap. Value (µF)	Shutdown & 3-State	Supply Current (mA max)	Guaranteed Data Rate (kbits/sec max)	Features
MAX220	+5	2	2	4	4.7/10	No	2	20	Ultra low-power, industry-standard pinout
MAX222	+5	2	2	4	0.1	Yes	10	116	MAX232A with shutdown
MAX223	+5	4	5	4	1.0	Yes	15	20	+5V IBM PC serial port w/ receivers active in shutdown
MAX230 (MAX200)	+5	5	0	4	1.0	Yes	15 (20)	20	5 drivers with shutdown
MAX231	+5 and +7.5 to +13.2	2	2	2	1.0	No	1/5	20	Standard +5/+12V or battery supplies; same functions as MAX232
MAX232 (MAX202)	+5	2	2	4	1.0	No	10 (15)	20	Industry standard
MAX232A	+5	2	2	4	0.1	No	10	116	Higher slew rate, small caps
MAX233 (MAX203)	+5	2	2	0	-	No	10 (15)	20	No external caps
MAX233A	+5	2	2	0	-	No	10	116	No external caps, high slew rate
MAX234 (MAX204)	+5	4	0	4	1.0 (0.1)	No	15 (20)	20	Replaces 1488
MAX235 (MAX205)	+5	5	5	0	-	Yes	15 (20)	20	No external caps
MAX236 (MAX206)	+5	4	3	4	1.0 (0.1)	Yes	15 (20)	20	Shutdown, three-state
MAX237 (MAX207)	+5	5	3	4	1.0 (0.1)	No	15 (20)	20	Complements IBM PC serial port
MAX238 (MAX208)	+5	4	4	4	1.0 (0.1)	No	15 (20)	20	Replaces 1488 and 1489
MAX239 (MAX209)	+5 and +7.5 to +13.2	3	5	2	1.0 (0.1)	No	1/15 (20)	20	Standard +5/+12V or battery supplies; single package solution for IBM PC serial port
MAX240	+5	5	5	4	1.0	Yes	15	20	DIP or flatpak package
MAX241 (MAX211)	+5	4	5	4	1.0 (0.1)	Yes	15 (20)	20	Complete IBM PC serial port
MAX242	+5	2	2	4	0.1	Yes	10	116	Separate shutdown and enable
MAX243	+5	2	2	4	0.1	No	10	116	Open-line detection simplifies cabling
MAX244	+5	8	10	4	1.0	No	25	64	High slew rate
MAX245	+5	8	10	0	-	Yes	25	64	High slew rate, int. caps, two shutdown modes
MAX246	+5	8	10	0	-	Yes	25	64	High slew rate, int. caps, three shutdown modes
MAX247	+5	8	9	0	-	Yes	25	64	High slew rate, int. caps, nine operating modes
MAX248	+5	8	8	4	1.0	Yes	25	64	High slew rate, selective half-chip enables
MAX249	+5	6	10	4	1.0	Yes	25	64	MAX248 with 2 complete IBM PC serial ports
MAX560	+3	4	5	4	1.0	Yes	8	20	+3V MAX561 + receivers active in shutdown
MAX561	+3	4	5	4	1.0	Yes	8	20	+3V Complete IBM PC serial port
RS-232 ISOLATION PRODUCTS									
MAX250	+5	2	2	-	-	Yes	-	20	Isolated RS-232 chipset
MAX251	+5	2	2	-	-	Yes	-	20	Isolated RS-232 chipset
MAX252A	+5	2	2	0	-	Yes	90	9.6	UL recognized, 1500V isolation
MAX252B	+5	2	2	0	-	Yes	90	9.6	Economical 500V isolation

ABSOLUTE MAXIMUM RATINGS – MAX220/222/232A/233A/242/243

Supply Voltage (V_{CC}) ..... -0.3V to +6V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} - 0.3V)
R_{IN} ..... ±30V
T_{OUT} (Note 1) ..... ±15V
Output Voltages
T_{OUT} ..... ±15V
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Driver/Receiver Output Short Circuited to GND ... Continuous
Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) . 842mW
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) . 889mW
20-Pin Plastic DIP (derate 8.00mW/°C above +70°C) .. 440mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) .. 696mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C) 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) ..... ?
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C) 842mW
Operating Temperature Ranges:
MAX2 _ _ AC _ _ , MAX2 _ _ C _ _ ..... 0°C to +70°C
MAX2 _ _ AE _ _ , MAX2 _ _ E _ _ ..... -40°C to +85°C
MAX2 _ _ AM _ _ , MAX2 _ _ M _ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Input voltage measured with T_{OUT} in high-impedance state, $\overline{SHDN}$ or V_{CC} = 0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX220/222/232A/233A/242/243

(V_{CC} = +5V ±10%, C1-C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±8		V
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High			2	1.4		V
Logic Pull-Up/Input Current	$\overline{SHDN}$ = V_{CC}			5	40	µA
	$\overline{SHDN}$ = 0V			±0.01	±1	
Output Leakage Current	V_{CC} = 5.5V, $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	µA
	V_{CC} = $\overline{SHDN}$ = 0V, V_{OUT} = ±15V			±0.01	±10	
Data Rate	Except MAX220, normal operation			200	116	kbits/sec
	MAX220			22	20	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±22		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±30	V
RS-232 Input Threshold Low	V_{CC} = 5V	Except MAX243 $R2_{IN}$	0.8	1.3		V
		MAX243 $R2_{IN}$ (Note 2)	-3			
RS-232 Input Threshold High	V_{CC} = 5V	Except MAX243 $R2_{IN}$		1.8	2.4	V
		MAX243 $R2_{IN}$ (Note 2)		-0.5	-0.1	
RS-232 Input Hysteresis	Except MAX243, V_{CC} = 5V, no hyst. in shdn.		0.2	0.5	1	V
	MAX243			1		
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} -0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Sinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	$\overline{SHDN}$ = V_{CC} or $\overline{EN}$ = V_{CC}, 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

ELECTRICAL CHARACTERISTICS – MAX220/222/232A/233A/242/243 (continued)

(V_{CC} = +5V ±10%, C1-C4 = 0.1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

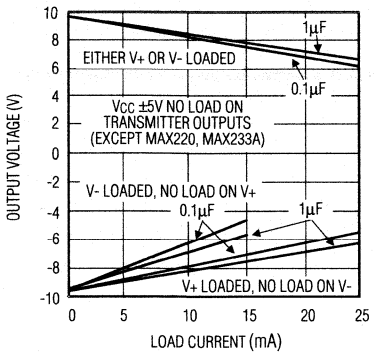
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{EN}$ Input Threshold Low				1.4	0.8	V
$\overline{EN}$ Input Threshold High			2.0	1.4		V
POWER SUPPLY						
Operating Supply Voltage			4.5		5.5	V
V_{CC} Supply Current ($\overline{SHDN}$ = V_{CC}), Figures 5, 6, 9, 18	No load	MAX220		0.5	2	mA
		MAX222/232A/233A/242/243		4	10	
	3kΩ load both outputs	MAX220		12		
		MAX222/232A/233A/242/243		15		
Shutdown Supply Current	MAX222/242	T_A = +25°C		0.1	10	µA
		T_A = 0°C to +70°C		2	50	
		T_A = -40°C to +85°C		2	50	
		T_A = -55°C to +125°C		35	100	
$\overline{SHDN}$ Input Leakage Current					±1	µA
$\overline{SHDN}$ Threshold Low				1.4	0.8	V
$\overline{SHDN}$ Threshold High			2.0	1.4		V
AC CHARACTERISTICS						
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V	MAX222/232A/233A/242/243	6	12	30	V/µs
		MAX220	1.5	3	30	
Transmitter Propagation Delay TTL to RS-232 (Normal Operation), Figure 1	t_{PHLT}	MAX222/232A/233A/242/243		1.3	3.5	µs
		MAX220		4	10	
	t_{PLHT}	MAX222/232A/233A/242/243		1.5	3.5	
		MAX220		5	10	
Receiver Propagation Delay RS-232 to TTL (Normal Operation), Figure 2	t_{PHLR}	MAX222/232A/233A/242/243		0.5	1	µs
		MAX220		0.6	3	
	t_{PLHR}	MAX222/232A/233A/242/243		0.6	1	
		MAX220		0.8	3	
Receiver Propagation Delay RS-232 to TTL (Shutdown), Figure 2	t_{PHLS}	MAX242		0.5	10	µs
	t_{PLHS}	MAX242		2.5	10	
Receiver-Output Enable Time, Figure 3	t_{ER}	MAX222/242		125	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}	MAX222/242		160	500	ns
Transmitter-Output Enable Time ($\overline{SHDN}$ goes high), Figure 4	t_{ET}	MAX222/242, 0.1µF caps (Includes charge-pump start-up)		250		µs
Transmitter-Output Disable Time ($\overline{SHDN}$ goes low), Figure 4	t_{DT}	MAX222/242, 0.1µF caps		600		ns
Transmitter + to - Propagation Delay Difference (Normal Operation)	t_{PHLT}-t_{PLHT}	MAX222/232A/233A/242/243		300		ns
		MAX220		2000		
Receiver + to - Propagation Delay Difference (Normal Operation)	t_{PHLR}-t_{PLHR}	MAX222/232A/233A/242/243		100		ns
		MAX220		225		

Note 2: MAX243 $R2_{OUT}$ is guaranteed to be low when the $R2_{IN}$ is ≥ 0V or is floating.

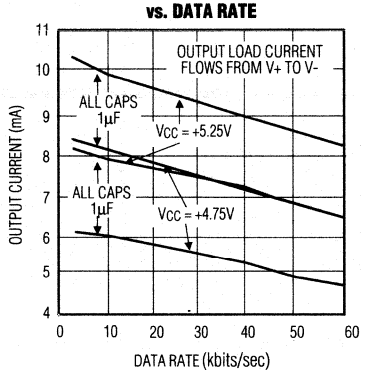
Typical Operating Characteristics

MAX220/222/232A/233A/242/243

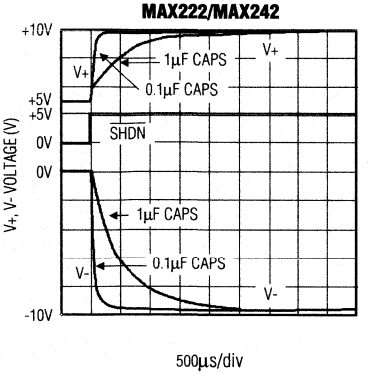
OUTPUT VOLTAGE vs. LOAD CURRENT



AVAILABLE OUTPUT CURRENT vs. DATA RATE



ON-TIME EXITING SHUTDOWN – MAX222/MAX242



2

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

ABSOLUTE MAXIMUM RATINGS – MAX223, MAX230-MAX241

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +14V
V- ..... +0.3V to -14V
Input Voltages
T_{IN} ..... -0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
Output Voltages
T_{OUT} ..... (V+ + 0.3V) to (V- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short-Circuit Duration, T_{OUT} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) . 800mW
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) . 842mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) . 889mW
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) 1067mW
24-Pin Plastic DIP (derate 9.09mW/°C above +70°C) .. 500mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) .. 800mW
24-Pin Wide SO (derate 11.76mW/°C above +70°C) ... 941mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) . 1000mW
44-Pin Plastic FP (derate 11.11mW/°C above +70°C) 611mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) .. 727mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) . 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) . 889mW
24-Pin Narrow CERDIP (derate 12.50mW/°C above +70°C) 1000mW
24-Pin Sidebraze (derate 20.0mW/°C above +70°C) 1600mW
28-Pin SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges:
MAX2 _ _ C _ _ ..... 0°C to +70°C
MAX2 _ _ E _ _ ..... -40°C to +85°C
MAX2 _ _ M _ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX223, MAX230-MAX241

(MAX223/230/232/234/236/237/238/240/241 V_{CC} = +5V ±10%, MAX233/MAX235 V_{CC} = 5V ±5%, C1-C4 = 1.0µF, MAX231/MAX239 V_{CC} = 5V ±10%, V+ = 7.5V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±7.3		V
V_{CC} Power-Supply Current	No load, T_A = +25°C	MAX232, 233		5	10	mA
		MAX223, 230, 234-238, 240, 241		7	15	
		MAX231, 239		.4	1	
V+ Power Supply Current		MAX231		1.8	5	mA
		MAX239		5	15	
Shutdown Supply Current	T_A = +25°C	MAX223		15	50	µA
		MAX241		1	10	
Input Logic Threshold Low	T_{IN}; EN, $\overline{SHDN}$ (MAX223), $\overline{EN}$, SHDN (MAX230, MAX235-MAX241)				0.8	V
Input Logic Threshold High	T_{IN}		2.0			
	EN, $\overline{SHDN}$ (MAX223), $\overline{EN}$, SHDN (MAX230, MAX235-MAX241)		2.4			V
Logic Pull-Up Current	T_{IN} = 0V			15	200	µA
Receiver Input Voltage Operating Range			-30		+30	V

ELECTRICAL CHARACTERISTICS – MAX223, MAX230-MAX241 (continued)

(MAX223/230/232/234/236/237/238/240/241 V_{CC} = +5V ±10%, MAX233/MAX235 V_{CC} = 5V ±5%, C1-C4 = 1.0µF, MAX231/MAX239 V_{CC} = 5V ±10%, V+ = 7.5V to 13.2V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

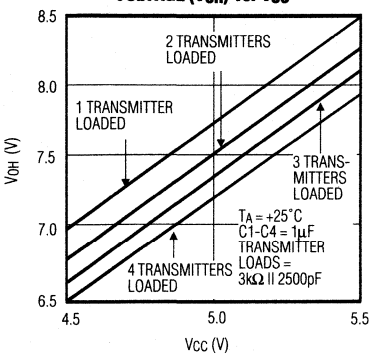
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 Input Threshold Low	T_A = +25°C, V_{CC} = 5V	Normal Operation $\overline{SHDN}$ = 5V (MAX223), SHDN = 0V (MAX235-MAX241)	0.8	1.2		V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V (R4, R5)	0.6	1.5		
RS-232 Input Threshold High	T_A = +25°C, V_{CC} = 5V	Normal Operation $\overline{SHDN}$ = 5V (MAX223), SHDN = 0V (MAX235-MAX241)		1.7	2.4	V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V (R4, R5)		1.5	2.4	
RS-232 Input Hysteresis	V_{CC} = 5V; no hysteresis in shutdown		0.2	0.5	1.0	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 1.6mA (MAX231-233 I_{OUT} = 3.2mA)				0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.4		V
TTL/CMOS Output Leakage Current	0V ≤ R_{OUT} ≤ V_{CC}; EN = 0V (MAX223); $\overline{EN}$ = V_{CC} (MAX235-241)			0.05	±10	µA
Receiver Output Enable Time	Normal operation	MAX223		600		ns
		MAX235-MAX241		400		
Receiver Output Disable Time	Normal operation	MAX223		900		ns
		MAX235-MAX241		250		
Propagation Delay	RS-232 IN to TTL/CMOS OUT, C_L = 150pF			0.5	10	µs
		t_{PHLS}		4	40	
		t_{PLHS}		6	40	
Transition Region Slew Rate	MAX223, MAX230, MAX234-MAX241 T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V		3	5.1	30	V/µs
	MAX231, MAX232, MAX233 T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V			4	30	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V		300			Ω
Receiver Out Short-Circuit Current				±10		mA

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

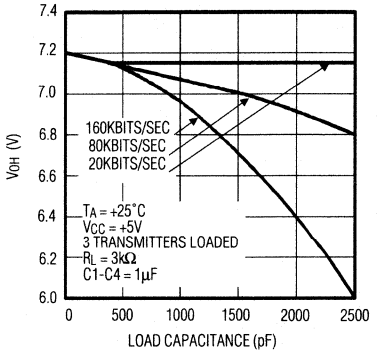
Typical Operating Characteristics

MAX223, MAX230, MAX234-MAX241

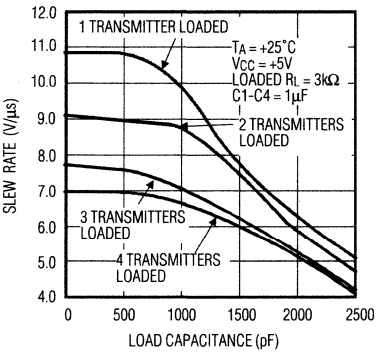
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. V_{CC}



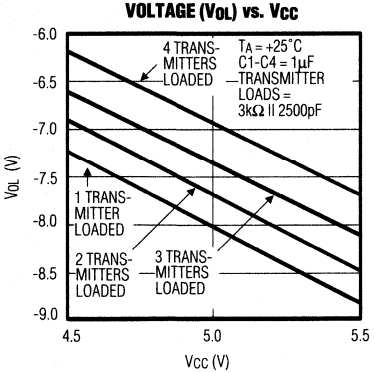
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



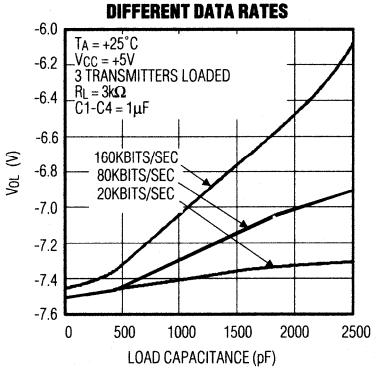
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



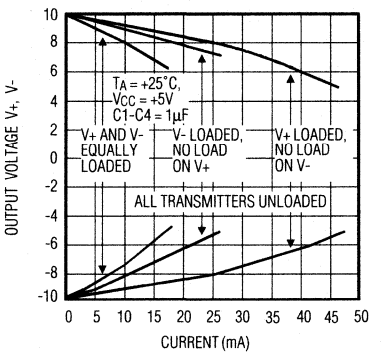
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. V_{CC}



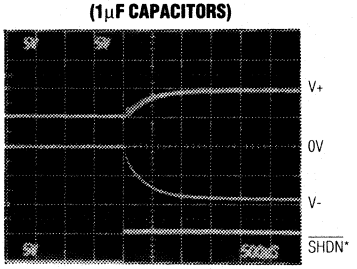
TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



TRANSMITTER OUTPUT VOLTAGE V+, V- vs. LOAD CURRENT



V+, V- WHEN EXITING SHUTDOWN (1µF CAPACITORS)



*SHUTDOWN POLARITY IS REVERSED FOR THE MAX241

ABSOLUTE MAXIMUM RATINGS – MAX244-MAX249

Supply Voltage (V_{CC}) ..... -0.3V to +6V
Input Voltages
  T_{IN}, ENA, ENB, ENR, ENT, ENRA,
  ENRB, ENTA, ENTB ..... -0.3V to (V_{CC} + 0.3V)
  R_{IN} ..... ±25V
  T_{OUT} (Note 4) ..... ±15V
  R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)
Short Circuit (1 output at a time)
  T_{OUT} to GND ..... Continuous
  R_{OUT} to GND ..... Continuous

Continuous Power Dissipation (T_A = +70°C)
  40-Pin Plastic DIP (derate 11.11mW/°C above +70°C) . . 611mW
  44-Pin PLCC (derate 13.33mW/°C above +70°C) 1067mW
Operating Temperature Ranges:
  MAX24_C_ _ ..... 0°C to +70°C
  MAX24_E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 4: Input voltage measured with transmitter output in a high-impedance state, shutdown, or V_{CC} = 0V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX244-MAX249

(V_{CC} = +5.0V ±10%, external capacitors C1-C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RS-232 TRANSMITTERS						
Input Logic Threshold Low				1.4	0.8	V
Input Logic Threshold High			2	1.4		V
Logic Pull-Up/Input Current	Tables 1A-1C	Normal operation		10	50	µA
		Shutdown		±0.01	±1	
Data Rate	Tables 1A-1C, normal operation				64	kbits/sec
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to GND		±5	±7.5		V
Output Leakage Current (Shutdown)	Tables 1A-1C			±0.01	±25	µA
				±0.01	±25	
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V (Note 5)		300	10M		Ω
Output Short-Circuit Current	V_{OUT} = 0V		±7	±30		mA
RS-232 RECEIVERS						
RS-232 Input Voltage Operating Range					±25	V
RS-232 Input Threshold Low	V_{CC} = 5V		0.8	1.3		V
RS-232 Input Threshold High	V_{CC} = 5V			1.8	2.4	V
RS-232 Input Hysteresis	V_{CC} = 5V		0.2	0.5	1.0	V
RS-232 Input Resistance			3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 3.2mA			0.2	0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC}-0.2		V
TTL/CMOS Output Short-Circuit Current	Sourcing V_{OUT} = GND		-2	-10		mA
	Sinking V_{OUT} = V_{CC}		10	30		
TTL/CMOS Output Leakage Current	Normal operation, outputs disabled, Tables 1A-1C, 0V ≤ V_{OUT} ≤ V_{CC}			±0.05	±10	µA

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

ELECTRICAL CHARACTERISTICS – MAX244-MAX249 (continued)

(V_{CC} = +5V ±10%, external capacitors C1-C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

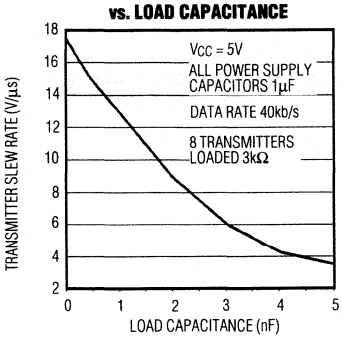
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY AND CONTROL LOGIC						
Operating Supply Voltage			4.5		5.5	V
V_{CC} Supply Current (Normal Operation)	No load			11	30	mA
	3kΩ loads on all outputs			57		
Shutdown Supply Current	T_A = +25°C			8	25	µA
	T_A = T_{MIN} to T_{MAX}				50	
Control Input	Leakage Current				±1	µA
	Threshold Low			1.4	0.8	V
	Threshold High		2.4	1.4		
AC CHARACTERISTICS						
Transition Slew Rate	C_L = 50pF to 2500pF, R_L = 3kΩ to 7kΩ, V_{CC} = 5V, T_A = +25°C, measured from +3V to -3V or -3V to +3V		5	10	30	V/µs
Transmitter Propagation Delay TTL to RS-232 (Normal Operation), Figure 1	t_{PHLT}			1.3	3.5	µs
	t_{PLHT}			1.5	3.5	
Receiver Propagation Delay RS-232 to TTL (Normal Operation), Figure 2	t_{PHLR}			0.6	1.5	µs
	t_{PLHR}			0.6	1.5	
Receiver Propagation Delay RS-232 to TTL (Low Power Mode), Figure 2	t_{PHLS}			0.6	10	µs
	t_{PLHS}			3.0	10	
Transmitter + to - Propagation Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}			350		ns
Receiver + to - Propagation Delay Difference (Normal Operation)	t_{PHLT} - t_{PLHT}			350		ns
Receiver-Output Enable Time, Figure 3	t_{ER}			100	500	ns
Receiver-Output Disable Time, Figure 3	t_{DR}			100	500	ns
Transmitter Enable Time, Figure 4	t_{ET}	MAX246-249 (excludes charge-pump startup)		5		µs
		MAX245, MAX247 (includes charge-pump startup)		10		ms
Transmitter Disable Time, Figure 3	t_{DT}			100		ns

Note 5: The 300Ω minimum specification complies with EIA-232E, but the actual resistance when in shutdown mode or V_{CC} = 0 is 10MΩ as is implied by the leakage specification.

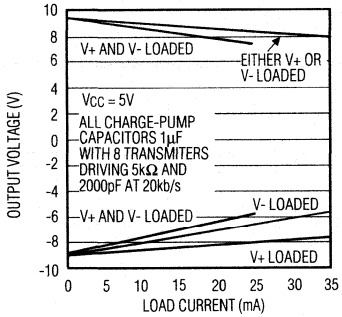
Typical Operating Characteristics

MAX244-MAX249

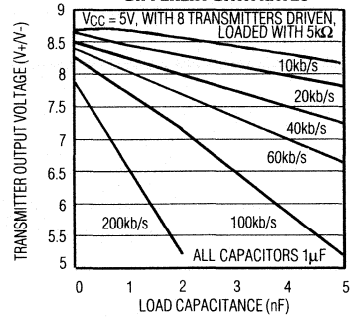
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



OUTPUT VOLTAGE vs. LOAD CURRENT FOR V+ AND V-



TRANSMITTER OUTPUT VOLTAGE vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



+5V-Powered Multi-Channel RS-232 Drivers/Receivers

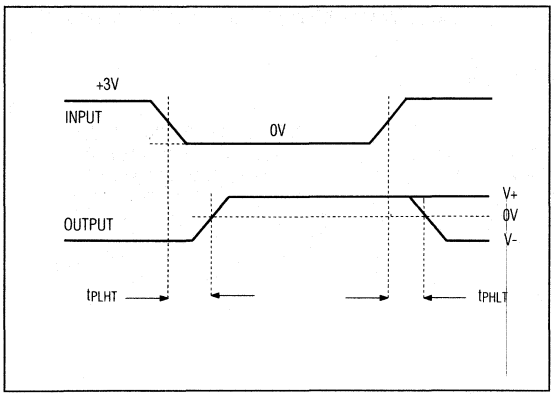


Figure 1. Transmitter Propagation Delay Timing

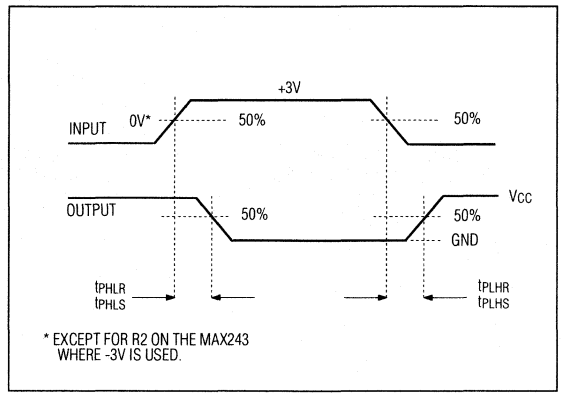


Figure 2. Receiver Propagation Delay Timing

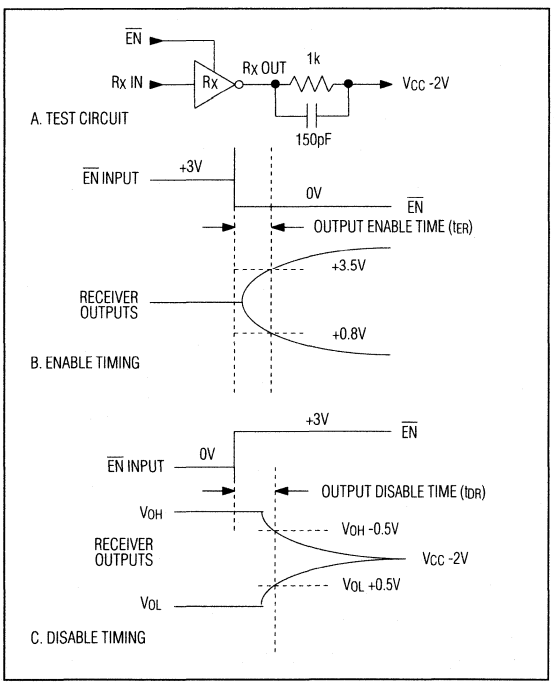


Figure 3. Receiver-Output Enable and Disable Timing

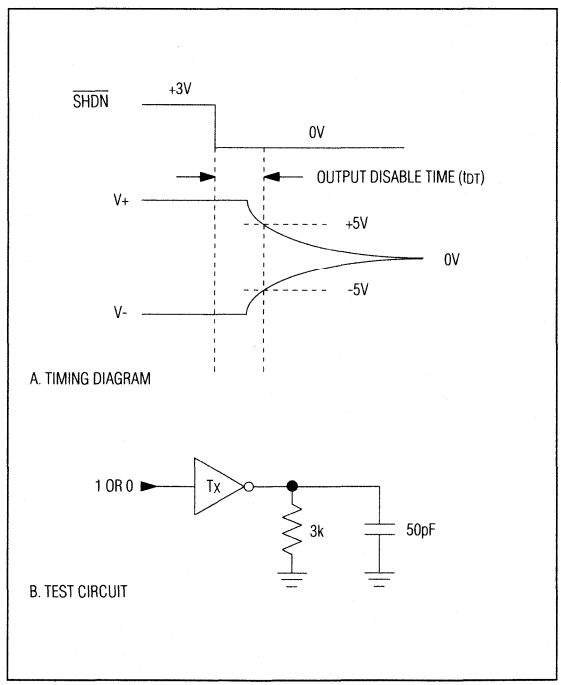


Figure 4. Transmitter-Output Disable Timing

Table 1A. MAX245 Control Pin Configurations

$\overline{ENT}$	$\overline{ENR}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All Active	RA1-RA4 3-State, RA5 Active	RB1-RB4 3-State, RB5 Active
1	0	Shutdown	All 3-State	All 3-State	All Low-Power Receive Mode	All Low-Power Receive Mode
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State, RA5 Low-Power Receive Mode	RB1-RB4 3-State, RB5 Low-Power Receive Mode

Table 1B. MAX246 Control Pin Configurations

$\overline{ENA}$	$\overline{ENB}$	OPERATION STATUS	TRANSMITTERS		RECEIVERS	
			TA1-TA4	TB1-TB4	RA1-RA5	RB1-RB5
0	0	Normal Operation	All Active	All Active	All Active	All Active
0	1	Normal Operation	All Active	All 3-State	All Active	RB1-RB4 3-State RB5 Active
1	0	Shutdown	All 3-State	All Active	RA1-RA4 3-State RA5 Active	All Active
1	1	Shutdown	All 3-State	All 3-State	RA1-RA4 3-State RA5 Low-Power Receive Mode	RB1-RB4 3-State RB5 Low-Power Receive Mode

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

Table 1C. MAX247/248/249 Control Pin Configurations

$\overline{ENTA}$	$\overline{ENTB}$	$\overline{ENRA}$	$\overline{ENRB}$	OPERATION STATUS		TRANSMITTERS		RECEIVERS	
					MAX247	TA1-TA4	TB1-TB4	RA1-RA4	RB1-RB5
					MAX248	TA1-TA4	TB1-TB4	RA1-RA4	RB1-RB4
					MAX249	TA1-TA3	TB1-TB3	RA1-RA5	RB1-RB5
0	0	0	0	Normal Operation		All Active	All Active	All Active	All Active
0	0	0	1	Normal Operation		All Active	All Active	All Active	All 3-State, except RB5 stays Active on MAX247
0	0	1	0	Normal Operation		All Active	All Active	All 3-State	All Active
0	0	1	1	Normal Operation		All Active	All Active	All 3-State	All 3-State, except RB5 stays Active on MAX247
0	1	0	0	Normal Operation		All Active	All 3-State	All Active	All Active
0	1	0	1	Normal Operation		All Active	All 3-State	All Active	All 3-State, except RB5 stays Active on MAX247
0	1	1	0	Normal Operation		All Active	All 3-State	All 3-State	All Active
0	1	1	1	Normal Operation		All Active	All 3-State	All 3-State	All 3-State, except RB5 stays Active on MAX247
1	0	0	0	Normal Operation		All 3-State	All Active	All Active	All Active
1	0	0	1	Normal Operation		All 3-State	All Active	All Active	All 3-State, except RB5 stays Active on MAX247
1	0	1	0	Normal Operation		All 3-State	All Active	All 3-State	All Active
1	0	1	1	Normal Operation		All 3-State	All Active	All 3-State	All 3-State, except RB5 stays Active on MAX247
1	1	0	0	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	Low-Power Receive Mode
1	1	0	1	Shutdown		All 3-State	All 3-State	Low-Power Receive Mode	All 3-State, except RB5 Low-Power Receive Mode on MAX247
1	1	1	0	Shutdown		All 3-State	All 3-State	All 3-State	Low-Power Receive Mode
1	1	1	1	Shutdown		All 3-State	All 3-State	All 3-State	All 3-State, except RB5 stays Active on MAX247

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

Detailed Description

The MAX220-MAX249 contain four sections: dual charge-pump DC-DC voltage converters, RS-232 drivers, RS-232 receivers, and receiver and transmitter enable control inputs.

Dual Charge-Pump Voltage Converter

The MAX220-MAX249 have two internal charge-pumps that convert +5V to ±10V (unloaded) for RS-232 driver operation. The first converter uses capacitor C1 to double the +5V input to +10V on C3 at the V+ output. The second converter uses capacitor C2 to invert +10V to -10V on C4 at the V- output.

A small amount of power may be drawn from the +10V (V+) and -10V (V-) outputs to power external circuitry (see Typical Operating Characteristics), except on the MAX245-MAX247, where these pins are not available. V+ and V- are not regulated, so the output voltage drops with increasing load current. Do not load V+ and V- to a point that violates the minimum ±5V EIA-232E driver output voltage when sourcing current from V+ and V- to external circuitry.

When using the shutdown feature (MAX222, MAX230, MAX235, MAX236, MAX240, MAX241 and MAX245-MAX249) avoid using V+ and V- to power external circuitry. When these parts are shut down, V- falls to 0V, and V+ falls to +5V. For applications where a +10V external supply is applied to the V+ pin (instead of using the internal charge pump to generate +10V), the C1 capacitor must not be installed and the $\overline{SHDN}$ pin must be tied to V_{CC}. This is because V+ is internally connected to V_{CC} in shutdown mode.

RS-232 Drivers

The typical driver output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver and V_{CC} = +5V. Output swing is guaranteed to meet the EIA-232E and V.28 specification, that calls for ±5V minimum driver output levels under worst-case conditions. These include a minimum 3kΩ load, V_{CC} = +4.5V, and maximum operating temperature. Unloaded driver output voltage ranges from (V+ -1.3V) to (V- +0.5V).

Input thresholds are both TTL and CMOS compatible. The inputs of unused drivers can be left unconnected since 400kΩ input pull-up resistors to V_{CC} are built-in. The pull-up resistors force the outputs of unused drivers low because all drivers invert. The internal input pull-up resistors typically source 12µA, except in shutdown mode where the pull-ups are disabled. Driver outputs turn off and enter a high-impedance state—where leakage current is typically microamperes (maximum 25µA)—when in shutdown mode, in three-state mode, or when device power is removed. Outputs can be driven to ±15V. The power-supply current typically drops to 8µA in shutdown mode.

The MAX239 has a receiver 3-state control line, and the MAX223, MAX235, MAX236, MAX240 and MAX241 have both a receiver 3-state control line and a low-power shutdown control. The receiver TTL/CMOS outputs are in a high-impedance 3-state mode whenever the 3-state $\overline{EN}$able line is high, and are also high-impedance whenever the shutdown control line is high.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA with the driver output pulled to ground. The driver output leakage remains less then 1µA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V the transmitter is diode clamped to ground with 1kΩ series impedance. The transmitter is also zener clamped to approximately V_{CC} + 6V, with a series impedance of 1kΩ.

The driver output slew rate is limited to less than 30V/µs as required by the EIA-232E and V.28 specifications.

RS-232 Receivers

EIA-232E and V.28 specifications define a voltage level greater than 3V as a logic 0, so all receivers invert. Input thresholds are set at 0.8V and 2.4V, so receivers respond to TTL level inputs as well as EIA-232E and V.28 levels.

The receiver inputs withstand an input overvoltage up to ±25V and provide input terminating resistors with nominal 5kΩ values. The receivers implement Type 1 interpretation of the fault conditions of V.28 and EIA-232E.

The receiver input hysteresis is typically 0.5V with a guaranteed minimum of 0.2V. This produces clear output transitions with slow-moving input signals, even with moderate amounts of noise and ringing. The receiver propagation delay is typically 600ns and is independent of input swing direction.

Low-Power Receive Mode

The low-power receive-mode feature of the MAX223, MAX242, and MAX245-MAX249 puts the IC into shutdown mode, but still allows it to receive information. This is important for applications where systems are periodically awakened to look for activity. Using low-power receive mode, the system can still receive a signal that will activate it on command and prepare it for communication at faster data rates. This operation conserves system power.

MAX243 – Negative Threshold

The MAX243 is pin compatible with the MAX232A, differing only in that RS-232 cable fault protection is removed on one of the two receiver inputs. This means that control lines such as CTS and RTS can either be driven or left floating without interrupting communication. Different cables are not needed to interface with different pieces of equipment.

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

The input threshold of the receiver without cable fault protection is -0.8V rather than +1.4V. Its output goes positive only if the input is connected to a control line that is actively driven negative. If not driven, it defaults to the 0 or "OK to send" state. Normally, the MAX243's other receiver (+1.4V threshold) is used for the data line (TD or RD), while the negative threshold receiver is connected to the control line (DTR, DTS, CTS, RTS, etc.).

Other members of the RS-232 family implement the optional cable fault protection as specified by EIA-232E specifications. This means a receiver output goes high whenever its input is driven negative, left floating, or shorted to ground. The high output tells the serial communications IC to stop sending data. To avoid this, the control lines must either be driven or connected with jumpers to an appropriate positive voltage level.

Shutdown – MAX222-MAX242

On the MAX222, MAX235, MAX236, MAX240, and MAX241, all receivers are disabled during shutdown. On the MAX223 and MAX242, two receivers continue to operate in a reduced power mode when the chip is in shutdown. Under these conditions, the propagation delay increases to about 2.5µs for a high-to-low input transition. When in shutdown, the receiver acts as a CMOS inverter with no hysteresis. The MAX223 and MAX242 also have a receiver output enable input ($\overline{EN}$) that allows receiver output control independent of $\overline{SHDN}$. With all other devices, $\overline{SHDN}$ also disables the receiver outputs.

Receiver and Transmitter Enable Control Inputs – MAX245-MAX249

The MAX245-MAX249 feature transmitter and receiver enable controls.

The receivers have three modes of operation: full-speed receive (normal active), three-state (disabled), and low-power receive (enabled receivers continue to function at lower data rates). The receiver enable inputs control the full-speed receive and three-state modes. The transmitters have two modes of operation: full-speed transmit (normal active) and three-state (disabled). The transmitter enable inputs also control the shutdown mode. The device enters shutdown mode when all transmitters are disabled. Enabled receivers function in the low-power receive mode when in shutdown.

Tables 1A-1C define the control states. The MAX244 has no control pins and is not included in these tables.

The MAX245 provides ten receivers and eight drivers with separate receiver and transmitter enable controls. The charge pumps turn off and the device shuts down when a logic high is applied to the $\overline{ENT}$ input. In this state, the supply current drops to less than 25µA and the receivers continue to operate in a low-power receive mode. Driver outputs enter a high-impedance state (three-state mode). Eight of the receiver outputs are controlled by the $\overline{ENR}$ input, while the remaining two receivers (RA5 and RB5) are always active. RA1-RA4 and RB1-RB4 are put in a three-state mode when $\overline{ENR}$ is a logic high.

The MAX246 has ten receivers and eight drivers with two control pins, each controlling one side of the device. A logic high at the A-side control input ($\overline{ENA}$) causes the four A-side receivers and drivers to go into a three-state mode. Similarly, the B-side control input ($\overline{ENB}$) causes the four B-side drivers and receivers to go into a three-state mode. As in the MAX245, one A-side and one B-side receiver (RA5 and RB5) remain active at all times. The entire device is put into shutdown mode when both the A and B sides are disabled, ($\overline{ENA}$ = $\overline{ENB}$ = +5V).

The MAX247 provides nine receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs each control four drivers. The ninth receiver (RB5) is always active. The device enters shutdown mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

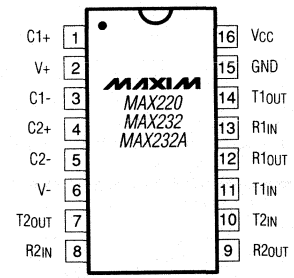
The MAX248 provides eight receivers and eight drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control four receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control four drivers each. This part does not have an always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$.

The MAX249 provides ten receivers and six drivers with four control pins. The $\overline{ENRA}$ and $\overline{ENRB}$ receiver enable inputs each control five receiver outputs. The $\overline{ENTA}$ and $\overline{ENTB}$ transmitter enable inputs control three drivers each. There is no always-active receiver. The device enters shutdown mode and transmitters go into a three-state mode with a logic high on both $\overline{ENTA}$ and $\overline{ENTB}$. In shutdown mode, active receivers operate in a low-power receive mode at data rates less than 20kb/s.

Applications Information

Figures 5 through 24 show pin configurations and typical operating circuits. In applications that are sensitive to power-supply noise, V_{CC} should be decoupled to ground with a capacitor of the same value as C1 and C2 connected as close as possible to the device. RS-232 receivers and drivers invert on all devices.

TOP VIEW



DIP/SO

CAPACITANCE (µF)					
DEVICE	C1	C2	C3	C4	C5
MAX220	4.7	4.7	10	10	4.7
MAX232	1.0	1.0	1.0	1.0	1.0
MAX232A	0.1	0.1	0.1	0.1	0.1

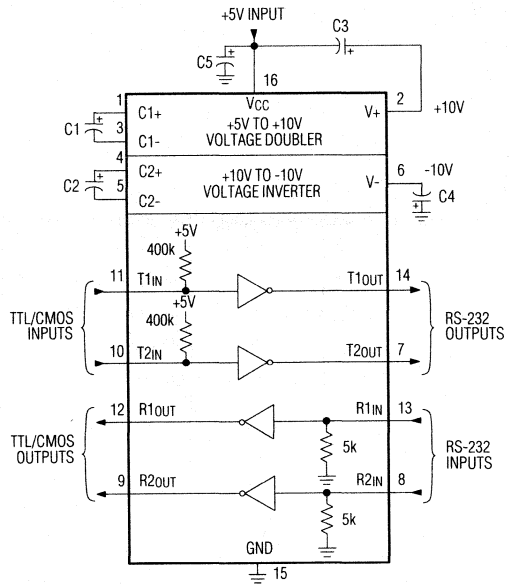
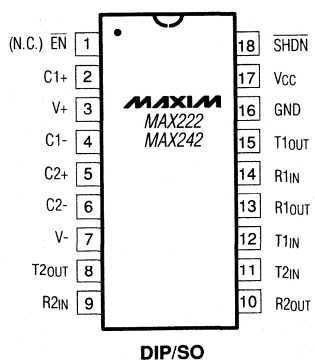


Figure 5. MAX220/232/232A Pin Configuration and Typical Operating Circuit

TOP VIEW



DIP/SO

( ) ARE FOR MAX222 ONLY.

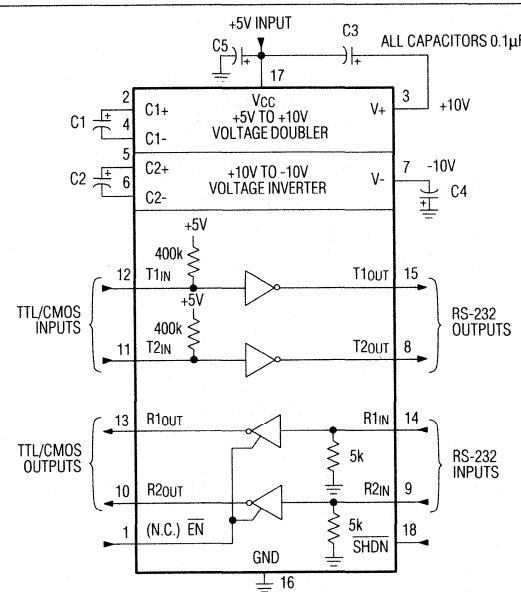


Figure 6. MAX222/MAX242 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

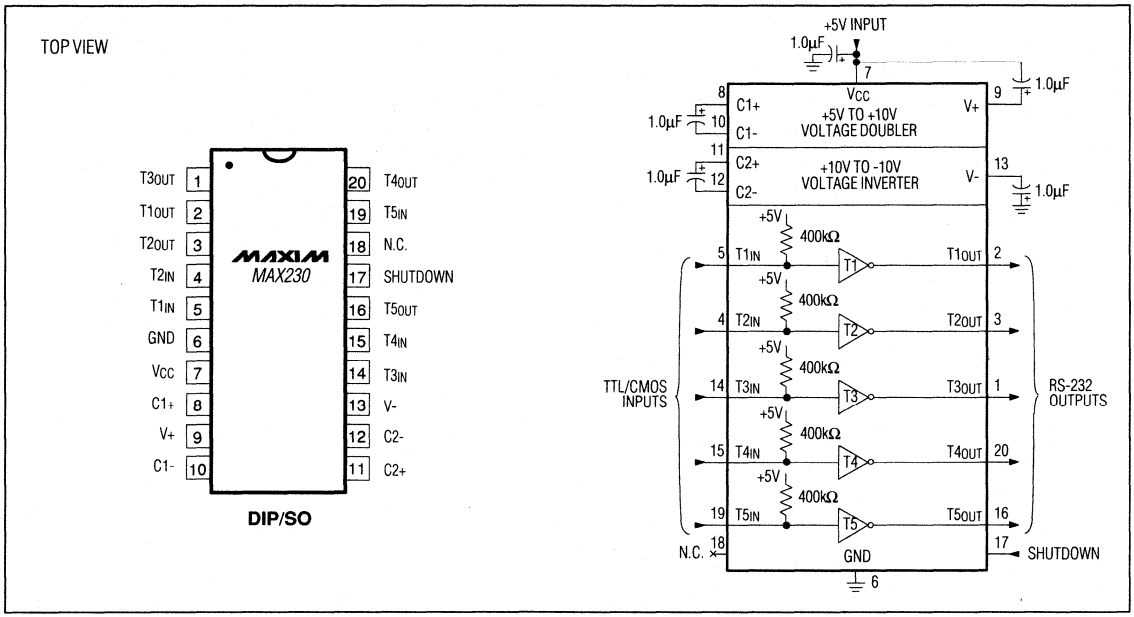


Figure 7. MAX230 Pin Configuration and Typical Operating Circuit

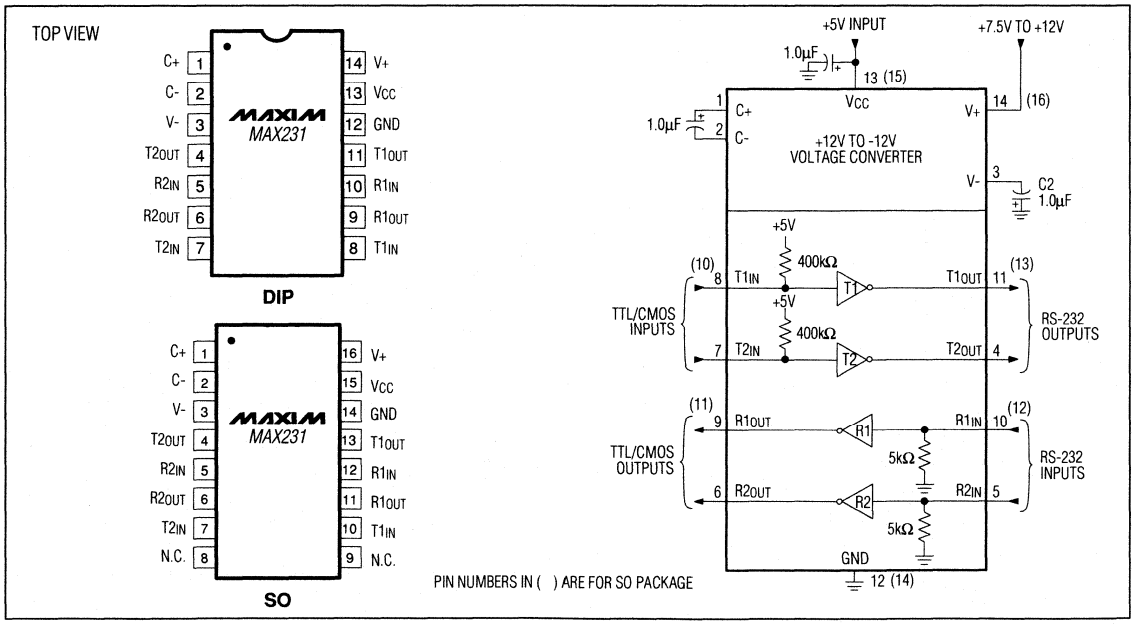


Figure 8. MAX230 Pin Configurations and Typical Operating Circuit

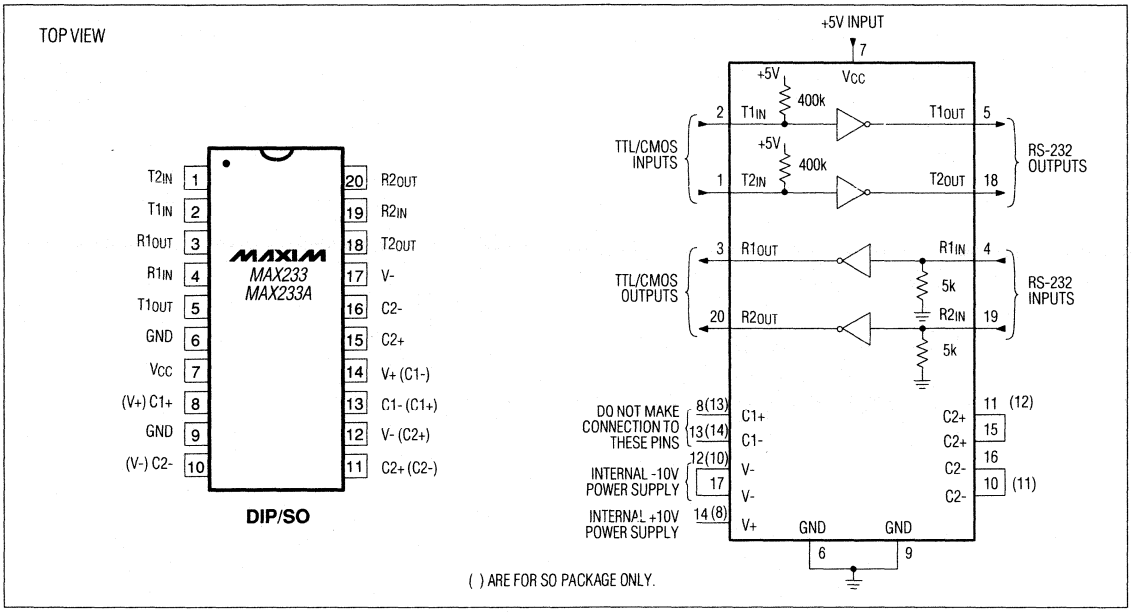


Figure 9. MAX233/MAX233A Pin Configuration and Typical Operating Circuit

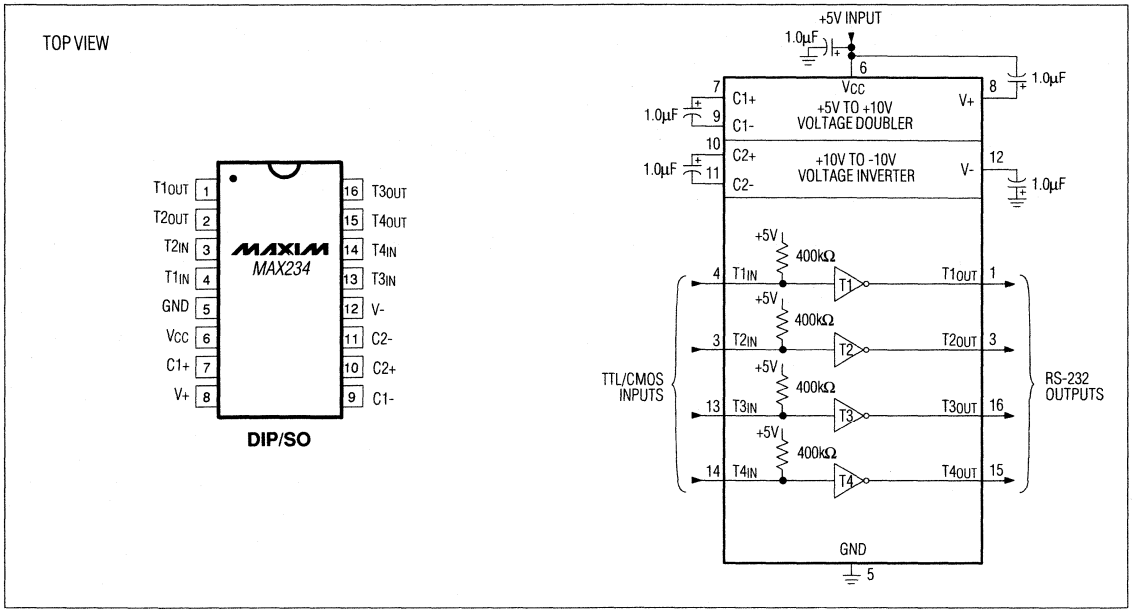


Figure 10. MAX234 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

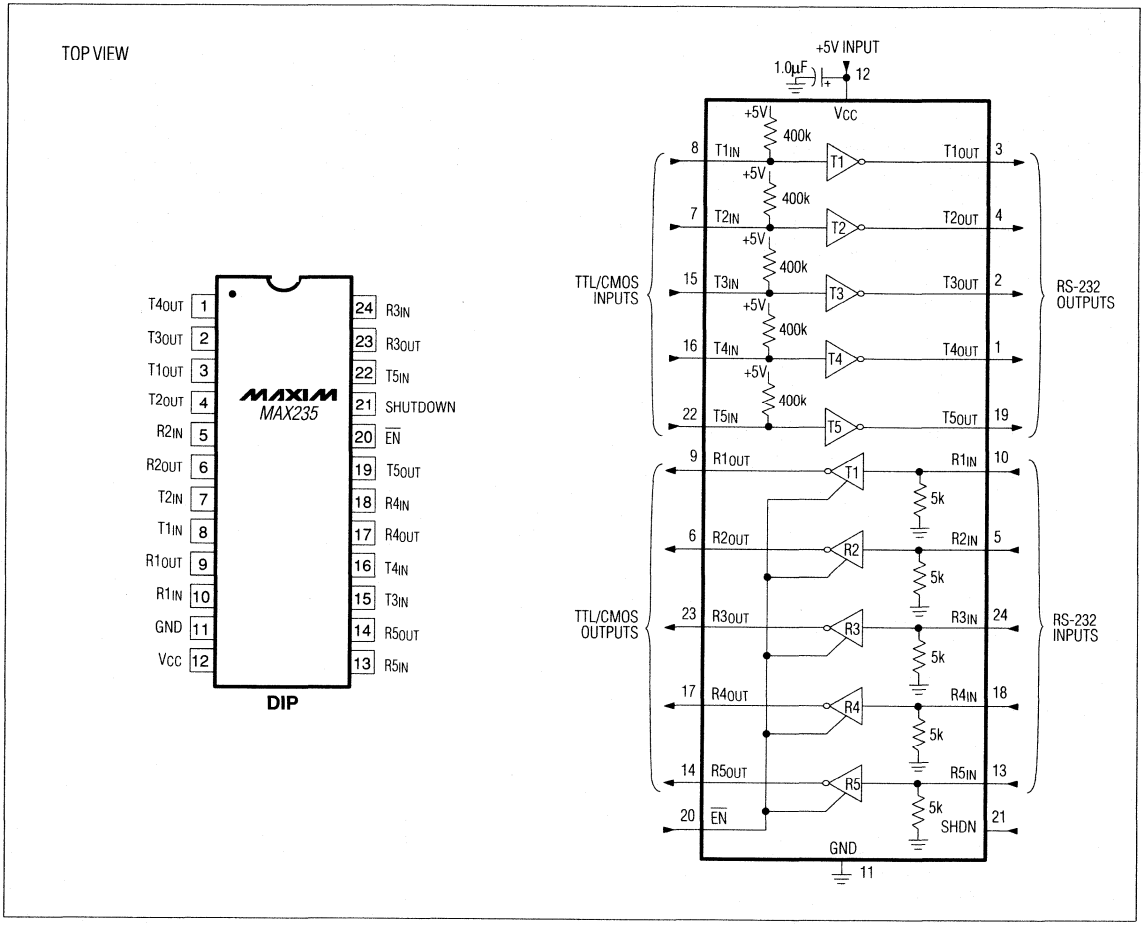


Figure 11. MAX235 Pin Configuration and Typical Operating Circuit

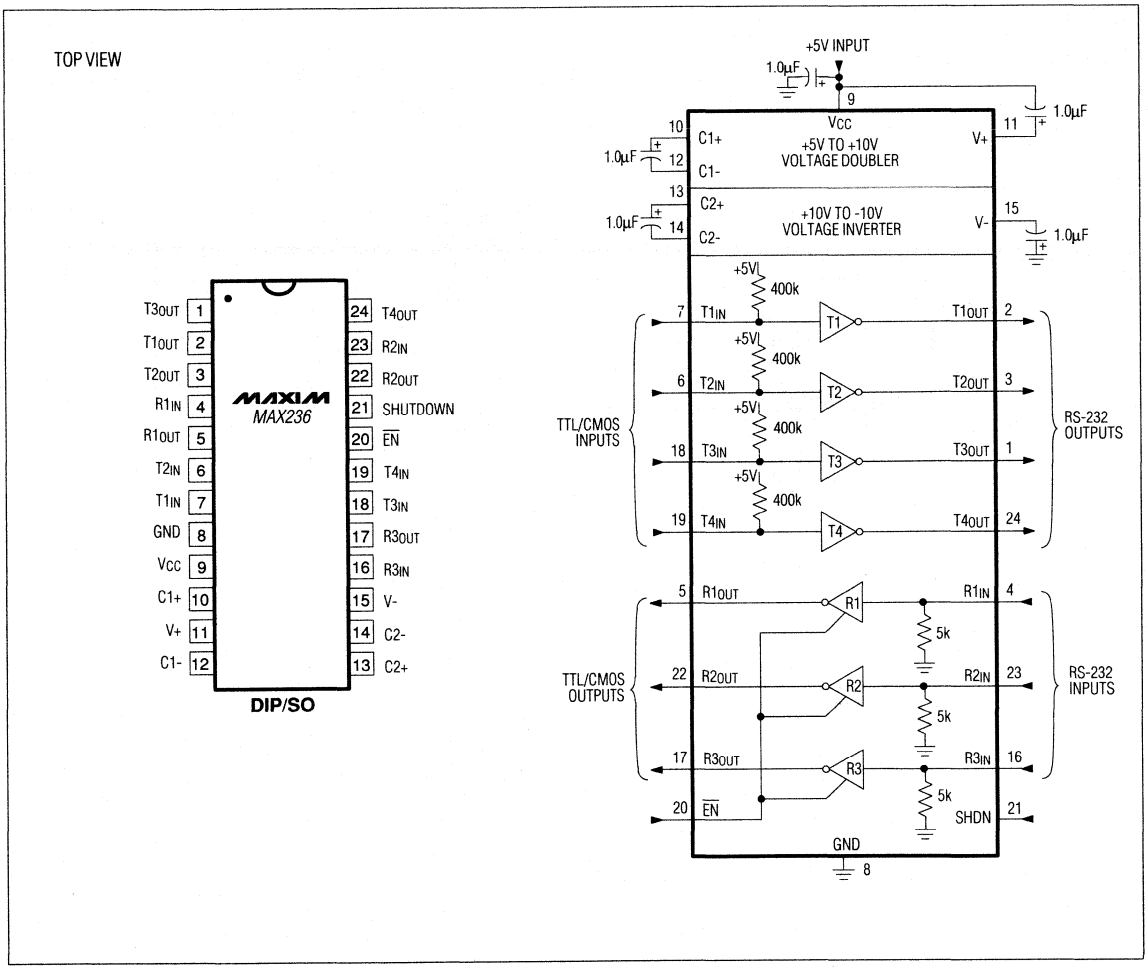


Figure 12. MAX236 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

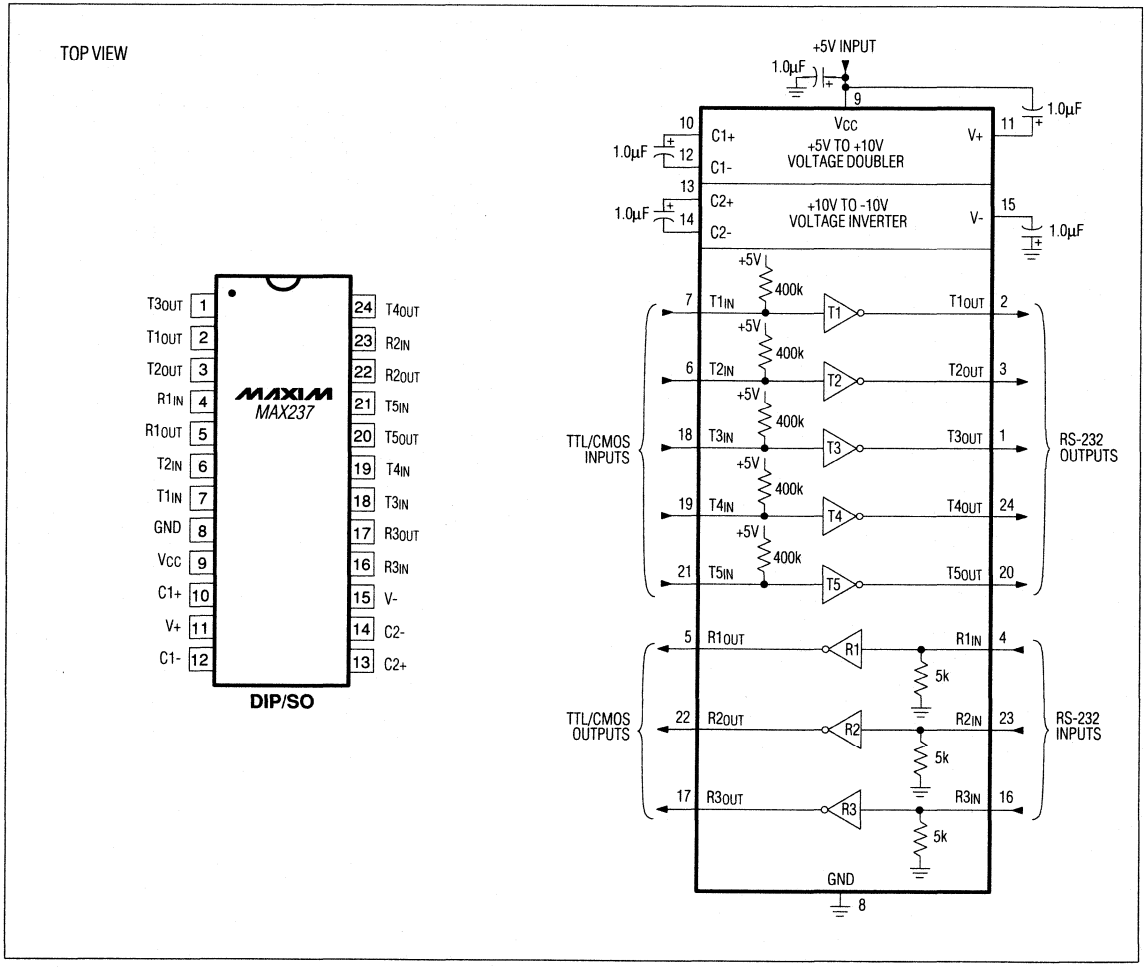


Figure 13. MAX237 Pin Configuration and Typical Operating Circuit

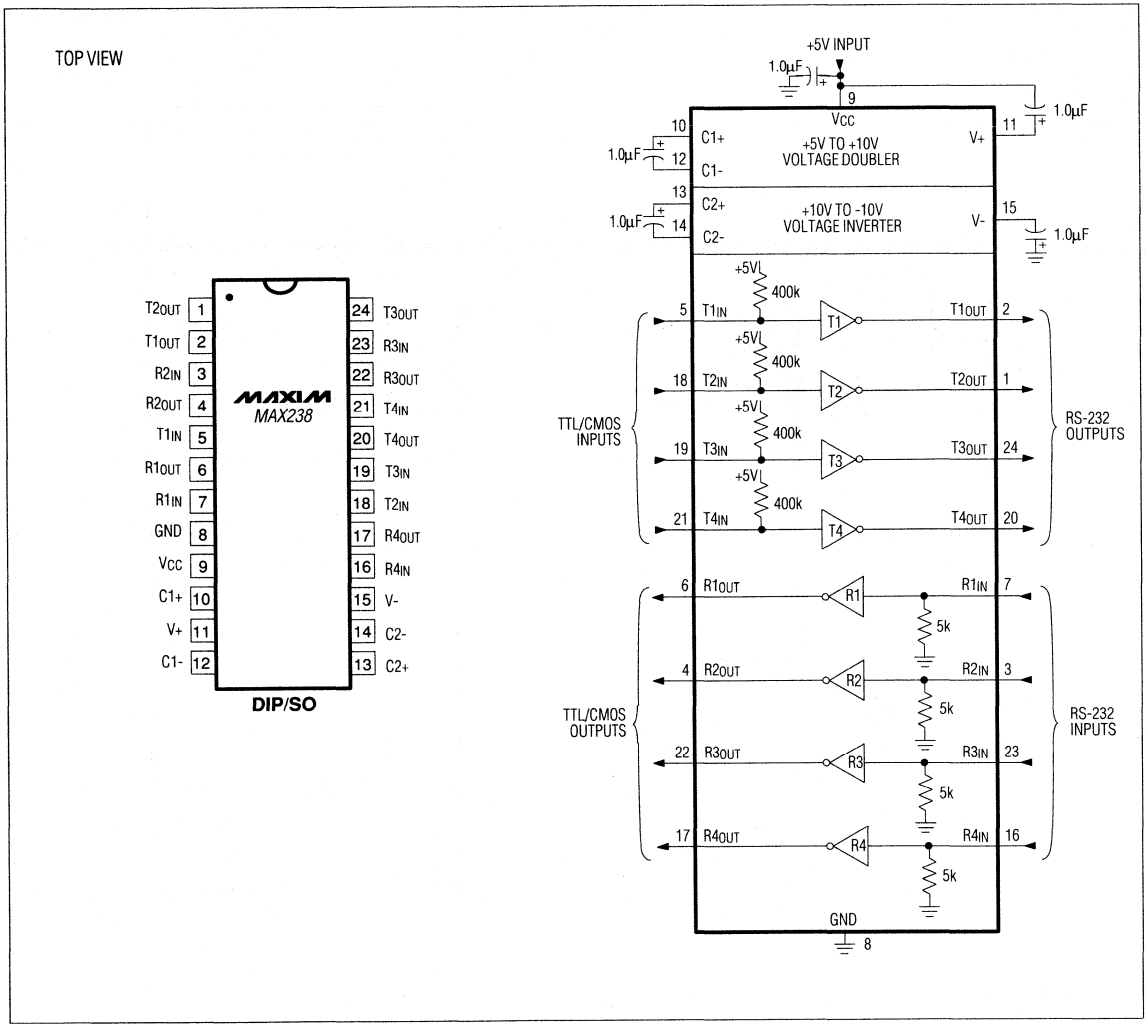


Figure 14. MAX238 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

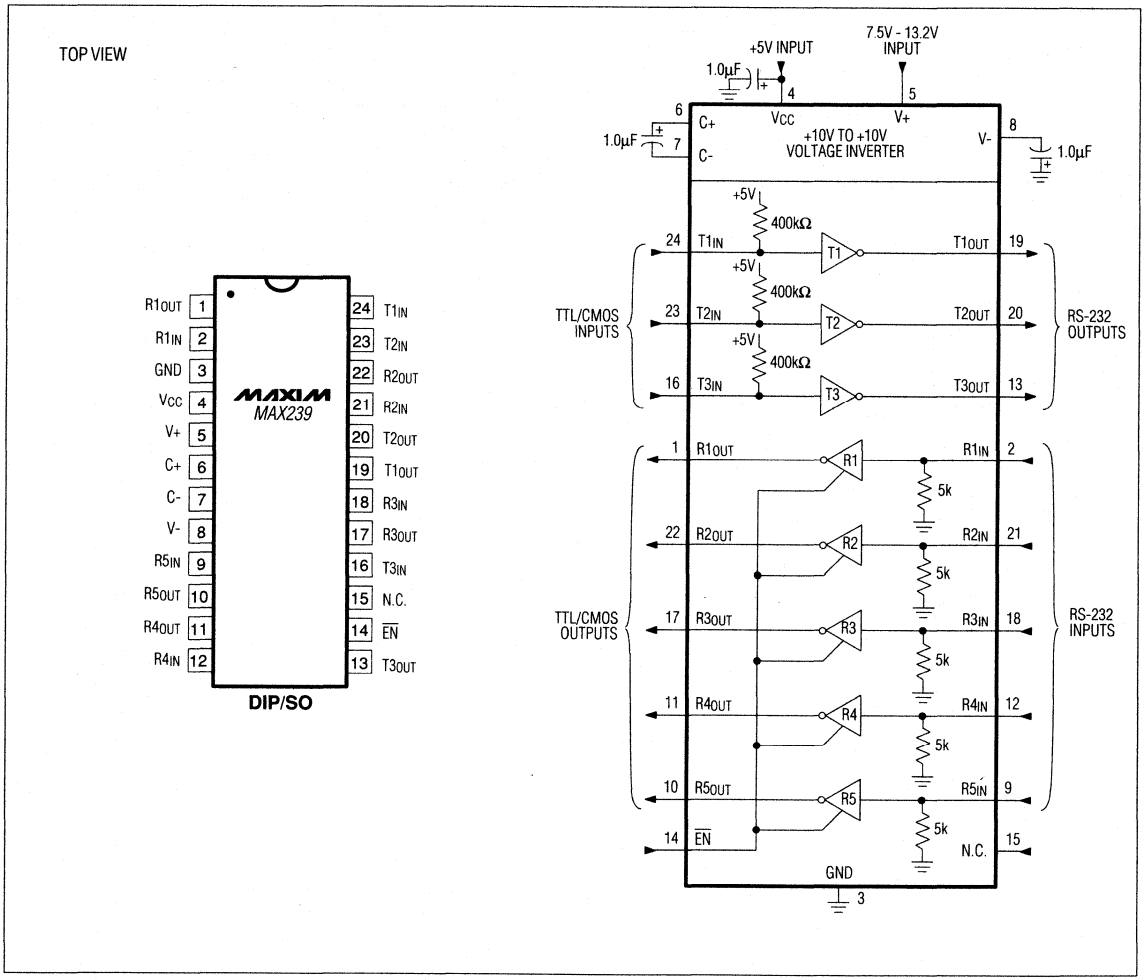


Figure 15. MAX239 Pin Configuration and Typical Operating Circuit

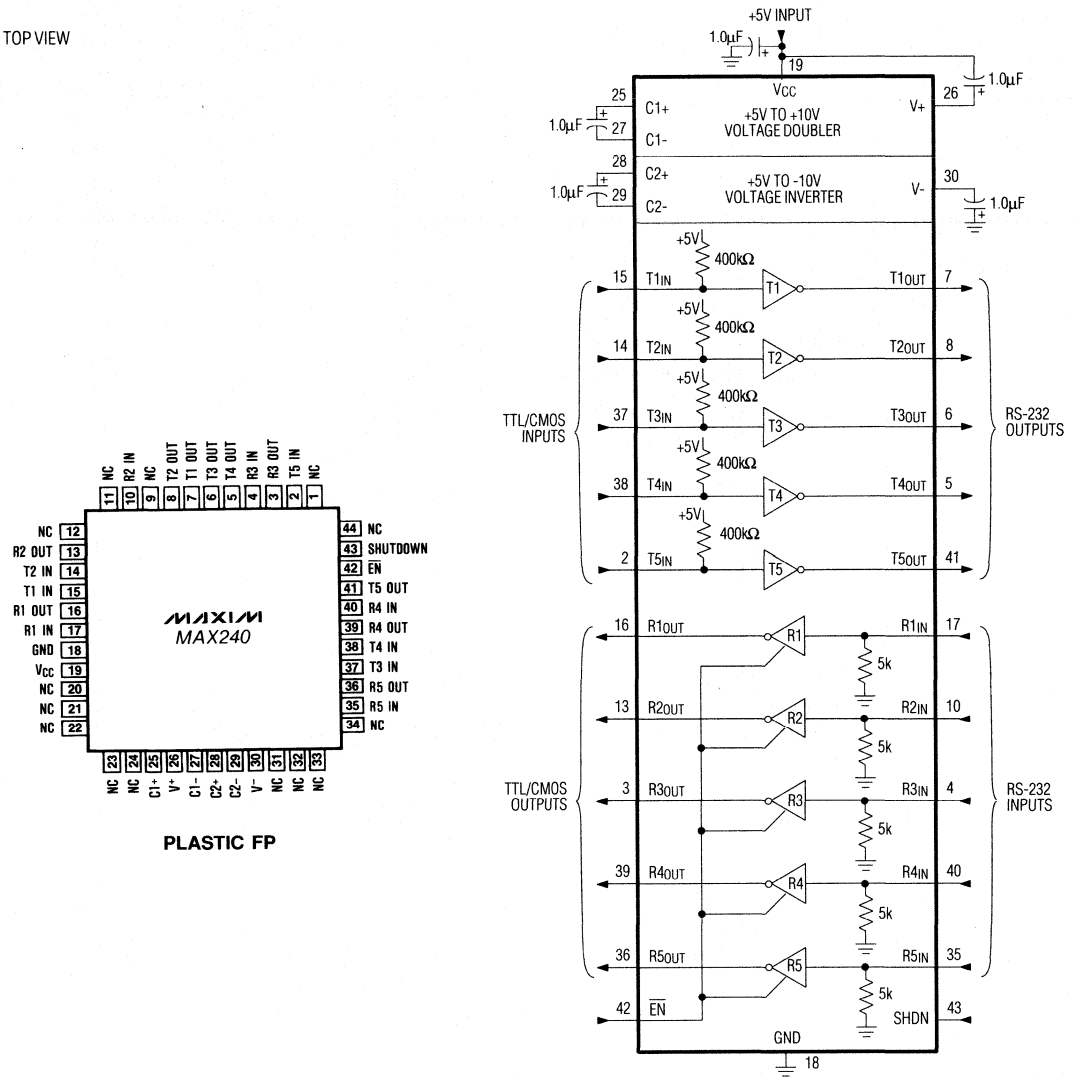


Figure 16. MAX240 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

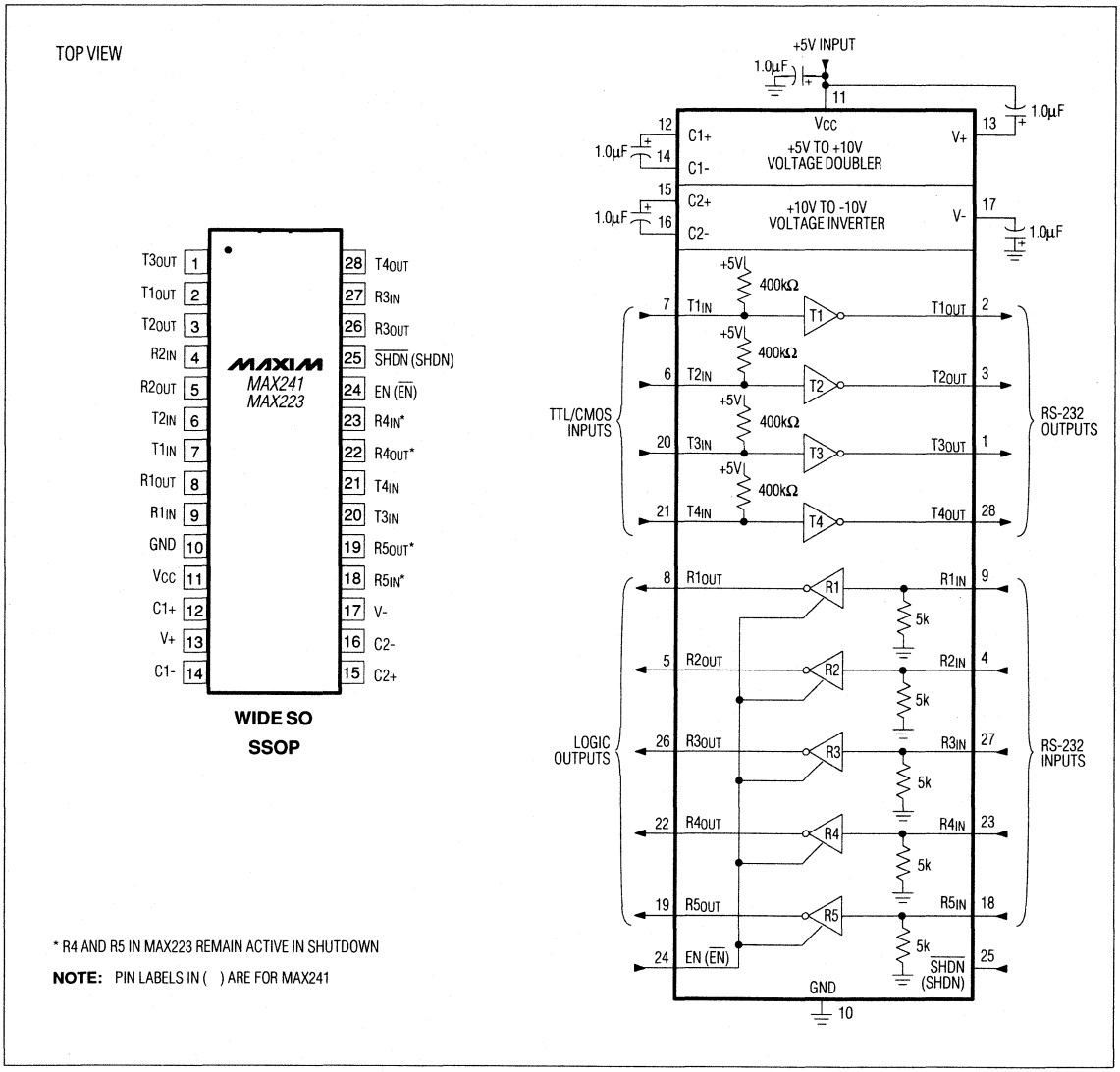
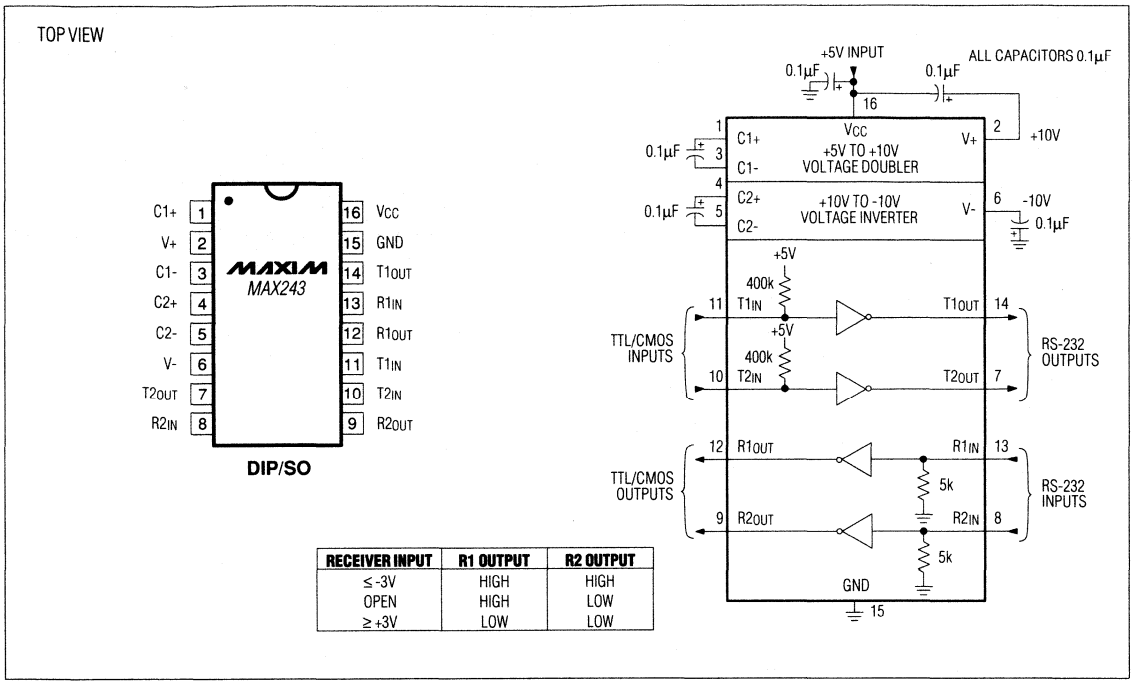


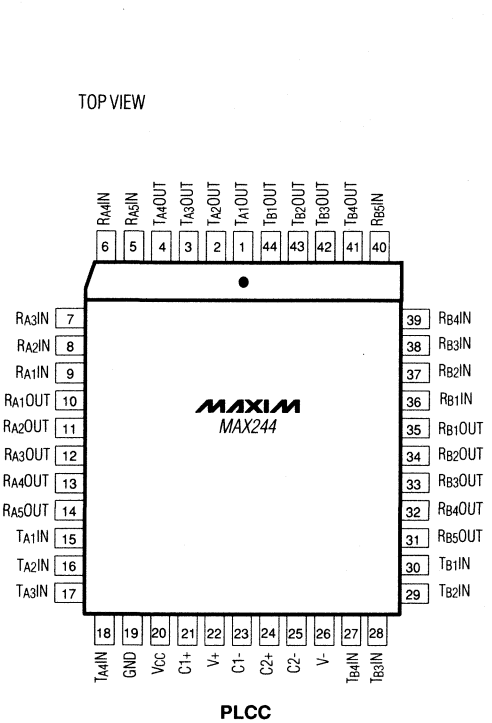
Figure 17. MAX241, MAX223 Pin Configuration and Typical Operating Circuit



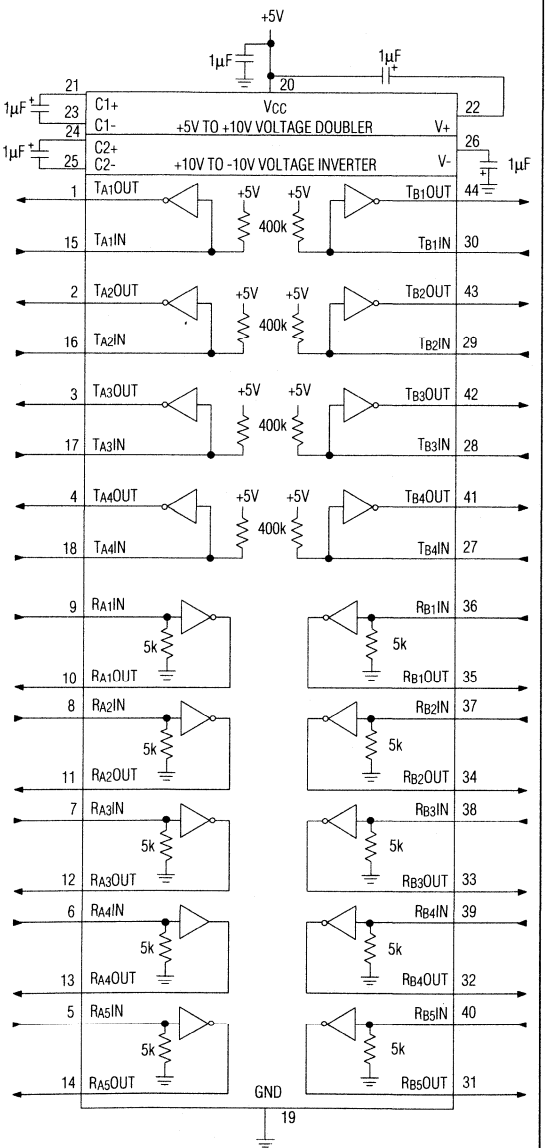
RECEIVER INPUT	R1 OUTPUT	R2 OUTPUT
≤ -3V	HIGH	HIGH
OPEN	HIGH	LOW
≥ +3V	LOW	LOW

Figure 18. MAX243 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers



PLCC



MAX244 Functional Description

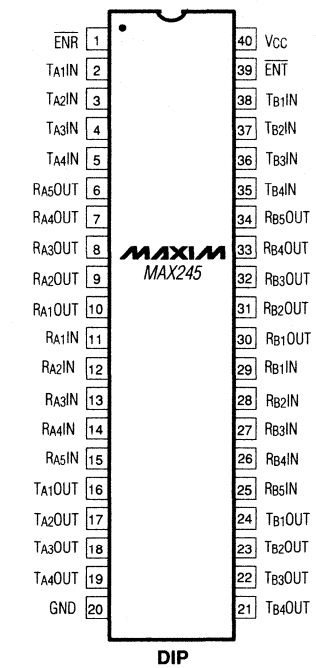
10 Receivers Always Active
- 5 A-Side Receivers
- 5 B-Side Receivers

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

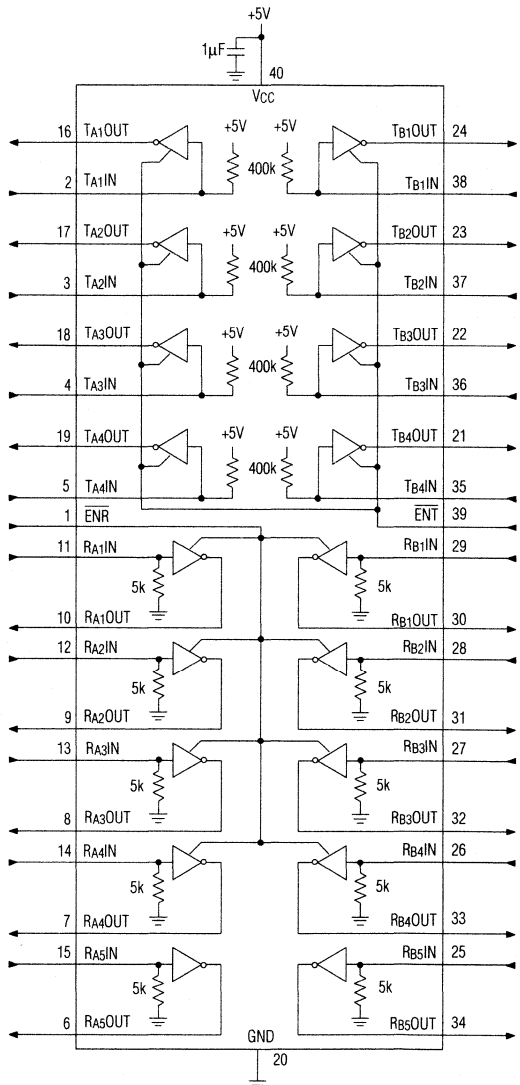
No Control Pins

Figure 19. MAX244 Pin Configuration and Typical Operating Circuit

TOP VIEW



DIP



MAX245 Functional Description

10 Receivers
- 5 A-Side Receivers (R_{A5} always active)
- 5 B-Side Receivers (R_{B5} always active)

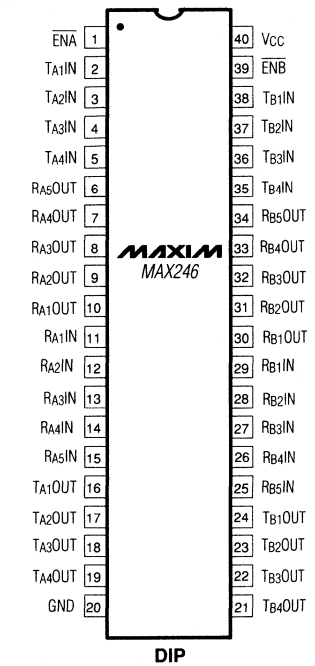
8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

2 Control Pins
- 1 Receiver Enable ($\overline{ENR}$)
- 1 Transmitter Enable ($\overline{ENT}$)

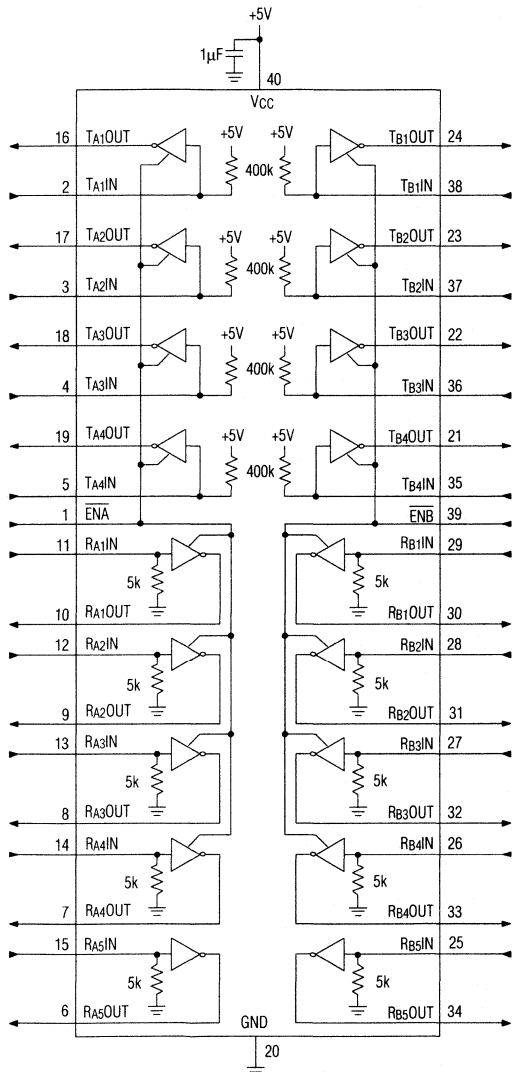
Figure 20. MAX245 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

TOP VIEW



DIP



MAX246 Functional Description

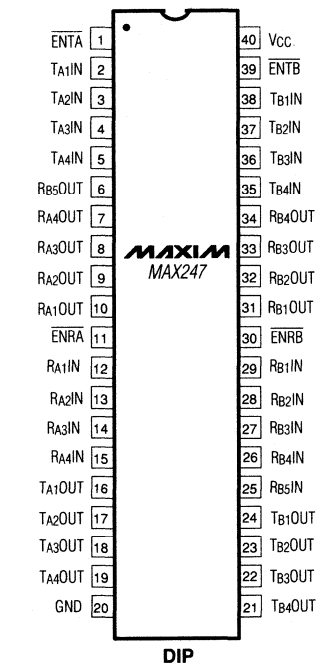
10 Receivers
- 5 A-Side Receivers (R_{A5} always active)
- 5 B-Side Receivers (R_{B5} always active)

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

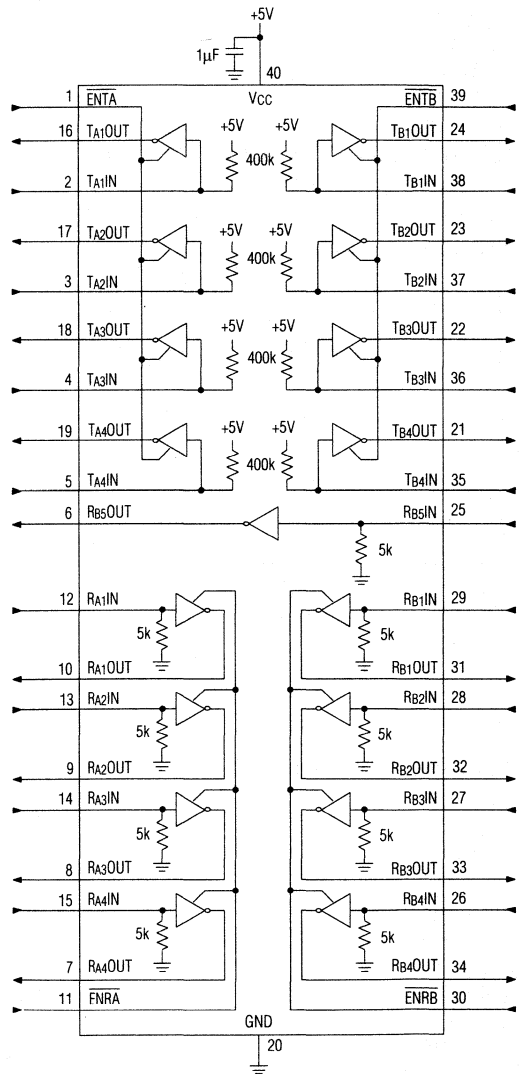
2 Control Pins
- Enable A-Side ($\overline{ENA}$)
- Enable B-Side ($\overline{ENB}$)

Figure 21. MAX246 Pin Configuration and Typical Operating Circuit

TOP VIEW



DIP



MAX247 Functional Description

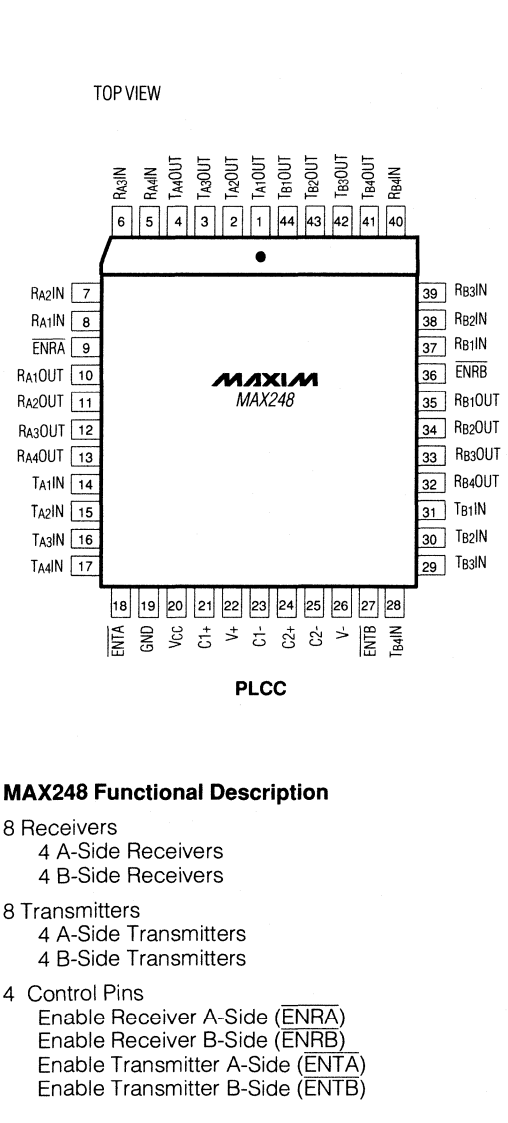
9 Receivers
- 4 A-Side Receivers
- 5 B-Side Receivers (R_{B5} always active)

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 22. MAX247 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers



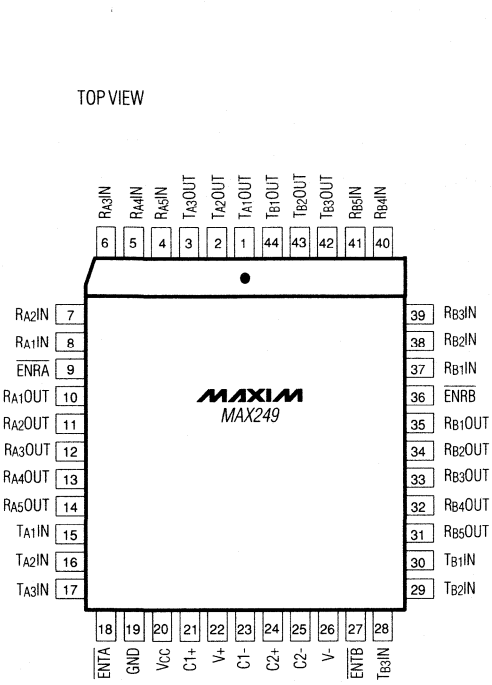
MAX248 Functional Description

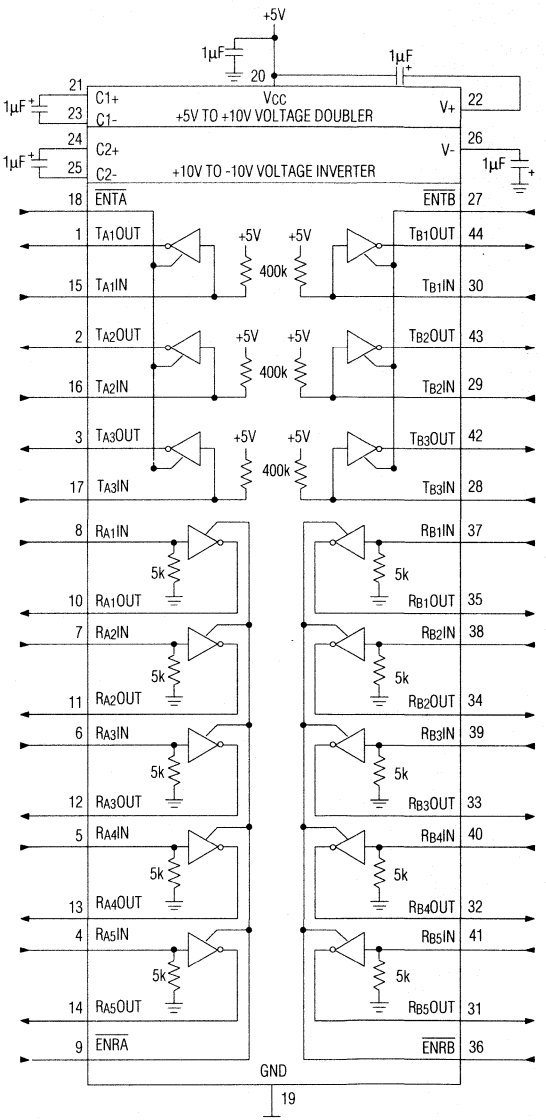
8 Receivers
- 4 A-Side Receivers
- 4 B-Side Receivers

8 Transmitters
- 4 A-Side Transmitters
- 4 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 23. MAX248 Pin Configuration and Typical Operating Circuit





MAX249 Functional Description

10 Receivers
- 5 A-Side Receivers
- 5 B-Side Receivers

6 Transmitters
- 3 A-Side Transmitters
- 3 B-Side Transmitters

4 Control Pins
- Enable Receiver A-Side ($\overline{ENRA}$)
- Enable Receiver B-Side ($\overline{ENRB}$)
- Enable Transmitter A-Side ($\overline{ENTA}$)
- Enable Transmitter B-Side ($\overline{ENTB}$)

Figure 24. MAX249 Pin Configuration and Typical Operating Circuit

+5V-Powered Multi-Channel RS-232 Drivers/Receivers

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX223CAI	0°C to +70°C	28 SSOP
MAX223CWI	0°C to +70°C	28 Wide SO
MAX223EAI	-40°C to +85°C	28 SSOP
MAX223EWI	-40°C to +85°C	28 Wide SO
MAX230CPP	0°C to +70°C	20 Plastic DIP
MAX230CWP	0°C to +70°C	20 Wide SO
MAX230C/D	0°C to +70°C	Dice*
MAX230EPP	-40°C to +85°C	20 Plastic DIP
MAX230EWP	-40°C to +85°C	20 Wide SO
MAX230MJP	-55°C to +125°C	20 CERDIP
MAX231CPD	0°C to +70°C	14 Plastic DIP
MAX231CWE	0°C to +70°C	16 Wide SO
MAX231C/D	0°C to +70°C	Dice*
MAX231EPD	-40°C to +85°C	14 Plastic DIP
MAX231EWE	-40°C to +85°C	16 Wide SO
MAX231MJD	-55°C to +125°C	14 CERDIP
MAX232CPE	0°C to +70°C	16 Plastic DIP
MAX232CWE	0°C to +70°C	16 Wide SO
MAX232C/D	0°C to +70°C	Dice*
MAX232EPE	-40°C to +85°C	16 Plastic DIP
MAX232EWE	-40°C to +85°C	16 Wide SO
MAX232MJE	-55°C to +125°C	16 CERDIP
MAX232ACPE	0°C to +70°C	16 Plastic DIP
MAX232ACSE	0°C to +70°C	16 Narrow SO
MAX232ACWE	0°C to +70°C	16 Wide SO
MAX232AC/D	0°C to +70°C	Dice*
MAX232AEPE	-40°C to +85°C	16 Plastic DIP
MAX232AESE	-40°C to +85°C	16 Narrow SO
MAX232AEWE	-40°C to +85°C	16 Wide SO
MAX232AMJE	-55°C to +125°C	16 CERDIP
MAX233CPP	0°C to +70°C	20 Plastic DIP
MAX233EPP	-40°C to +85°C	20 Plastic DIP
MAX233ACPP	0°C to +70°C	20 Plastic DIP
MAX233ACWP	0°C to +70°C	20 Wide SO
MAX233AEPP	-40°C to +85°C	20 Plastic DIP
MAX233AEWP	-40°C to +85°C	20 Wide SO
MAX234CPE	0°C to +70°C	16 Plastic DIP
MAX234CWE	0°C to +70°C	16 Wide SO
MAX234C/D	0°C to +70°C	Dice*
MAX234EPE	-40°C to +85°C	16 Plastic DIP
MAX234EWE	-40°C to +85°C	16 Wide SO
MAX234MJE	-55°C to +125°C	16 CERDIP
MAX235CPG	0°C to +70°C	24 Wide Plastic DIP
MAX235EPG	-40°C to +85°C	24 Wide Plastic DIP
MAX235EDG	-40°C to +85°C	24 Ceramic SB
MAX235MDG	-55°C to +125°C	24 Ceramic SB
MAX236CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX236CWG	0°C to +70°C	24 Wide SO
MAX236C/D	0°C to +70°C	Dice*
MAX236ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX236EWG	-40°C to +85°C	24 Wide SO
MAX236MRG	-55°C to +125°C	24 CERDIP
MAX237CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX237CWG	0°C to +70°C	24 Wide SO
MAX237C/D	0°C to +70°C	Dice*
MAX237ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX237EWG	-40°C to +85°C	24 Wide SO
MAX237MRG	-55°C to +125°C	24 CERDIP
MAX238CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX238CWG	0°C to +70°C	24 Wide SO
MAX238C/D	0°C to +70°C	Dice*
MAX238ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX238EWG	-40°C to +85°C	24 Wide SO
MAX238MRG	-55°C to +125°C	24 CERDIP
MAX239CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX239CWG	0°C to +70°C	24 Wide SO
MAX239C/D	0°C to +70°C	Dice*
MAX239ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX239EWG	-40°C to +85°C	24 Wide SO
MAX239MRG	-55°C to +125°C	24 CERDIP
MAX240CMH	0°C to +85°C	44 Plastic FP
MAX241CAI	0°C to +70°C	28 SSOP
MAX241EAI	-40°C to +85°C	28 SSOP
MAX241CWI	0°C to +70°C	28 Wide SO
MAX241EWI	-40°C to +85°C	28 Wide SO
MAX242CPN	0°C to +70°C	18 Plastic DIP
MAX242CWN	0°C to +70°C	18 Wide SO
MAX242C/D	0°C to +70°C	Dice*
MAX242EPN	-40°C to +85°C	18 Plastic DIP
MAX242EWN	-40°C to +85°C	18 Wide SO

** Contact factory for dice specifications.*

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX242MJN	-55°C to +125°C	18 CERDIP
MAX243CPE	0°C to +70°C	16 Plastic DIP
MAX243CSE	0°C to +70°C	16 Narrow SO
MAX232CWE	0°C to +70°C	16 Wide SO
MAX243C/D	0°C to +70°C	Dice*
MAX243EPE	-40°C to +85°C	16 Plastic DIP
MAX243ESE	-40°C to +85°C	16 Narrow SO
MAX232EWE	-40°C to +85°C	16 Wide SO
MAX243MJE	-55°C to +125°C	16 CERDIP
MAX244CQH	0°C to +70°C	44 PLCC
MAX244C/D	0°C to +70°C	Dice*
MAX244EQH	-40°C to +85°C	44 PLCC
MAX245CPL	0°C to +70°C	40 Plastic DIP
MAX245C/D	0°C to +70°C	Dice*
MAX245EPL	-40°C to +85°C	40 Plastic DIP
MAX246CPL	0°C to +70°C	40 Plastic DIP
MAX246C/D	0°C to +70°C	Dice*
MAX246EPL	-40°C to +85°C	40 Plastic DIP
MAX247CPL	0°C to +70°C	40 Plastic DIP
MAX247C/D	0°C to +70°C	Dice*
MAX247EPL	-40°C to +85°C	40 Plastic DIP
MAX248CQH	0°C to +70°C	44 PLCC
MAX248C/D	0°C to +70°C	Dice*
MAX248EQH	-40°C to +85°C	44 PLCC
MAX249CQH	0°C to +70°C	44 PLCC
MAX249EQH	-40°C to +85°C	44 PLCC

** Contact factory for dice specifications.*

19-0022; Rev 0; 5/92

MAXIM

+5V RS-232 Transceiver with Two Receivers Active in Shutdown

General Description

The MAX223/MAX241 are line drivers/receivers designed for RS-232 and V.28 communication interfaces, and in particular, for applications where ±12V supplies are not available. The MAX223/MAX241 include four line drivers, five receivers, a shutdown mode and a receiver enable input. On-board charge pumps convert the +5V input to the ±10V needed for RS-232 output levels. The MAX223/MAX241 drivers and receivers meet all EIA/TIA-232E and CCITT V.28 specifications at a data rate of 20kbits/sec. The drivers maintain the ±5V EIA/TIA-232 output signal levels at data rates in excess of 120kbits/sec when loaded in accordance with the EIA/TIA-232E specification.

The MAX223 has an active-low shutdown and an active-high receiver enable. In shutdown mode, two receivers are active, allowing ring indicator (RI) to be easily monitored. The MAX241 has an active-high shutdown and an active-low receiver enable. In shutdown mode, all receivers are in a high-impedance three-state mode.

The MAX223/MAX241 are available in a 28-pin wide small-outline (SO) package and a 28-pin shrink small-outline package (SSOP), which requires 40% the board space of the SO package. Each operates with four 1µF capacitors, further reducing board space.

Applications

Computers – Laptops, Palmtops, Notebooks
Battery-Powered Equipment
Hand-Held Equipment

Features

- ♦ **2 Receivers Active in Shutdown Mode (MAX223)**
- ♦ **Small 28-Pin SSOP Package – 40% the Area of SO Package**
- ♦ **Low-Power Shutdown Current: 15µA MAX223 1µA MAX241**
- ♦ **120kbits/sec Data Rate - Lap-Link Compatible**
- ♦ **Guaranteed 3V/µs Min Slew Rate**
- ♦ **4 Drivers/5 Receivers**
- ♦ **Operate from Single +5V Power Supply**
- ♦ **Designed for RS-232 and V.28 Applications**
- ♦ **Three-State TTL/CMOS Receiver Outputs**

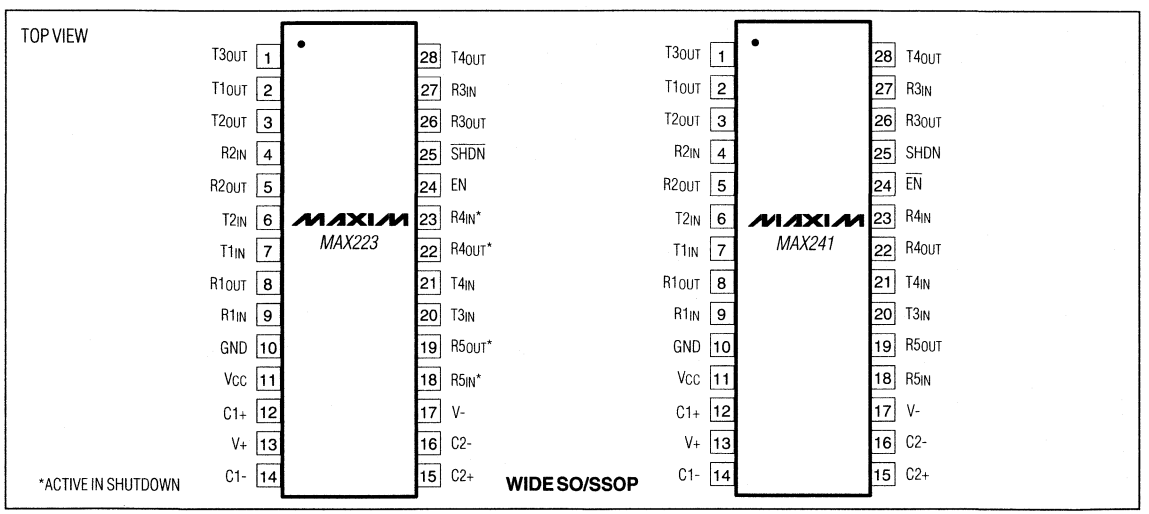
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX223CWI	0°C to +70°C	28 Wide SO
MAX223CAI	0°C to +70°C	28 SSOP
MAX223C/D	0°C to +70°C	Dice*
MAX223EWI	-40°C to +85°C	28 Wide SO
MAX223EAI	-40°C to +85°C	28 SSOP

Ordering Information continued on page 10.

**Dice are specified at T_A = +25°C.*

Pin Configurations



Typical Operating Circuit on Page 9.

+5V RS-232 Transceiver with Two Receivers Active in Shutdown

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +14V
V- ..... +0.3V to -14V
Input Voltages:
T_{IN} ..... -0.3 to (V_{CC} + 0.3V)
R_{IN} ..... ±30V
Output Voltages:
T_{OUT} ..... (V+ + 0.3V) to (V- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration
T_{OUT} ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Wide SO (derate 12.50mW/°C above +70°C) 1000mW
SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Ranges:
MAX223/241C_ _ ..... 0°C to +70°C
MAX223/241E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.5V to 5.5V, C1 - C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	All transmitter outputs loaded with 3kΩ to ground		±5.0	±7.3		V
V_{CC} Power-Supply Current	No load, T_A = +25°C			7	15	mA
Shutdown Supply Current	T_A = +25°C, Figure 1	MAX223		15	50	µA
		MAX241		1	10	
Input Logic Threshold Low	T_{IN}; EN, $\overline{SHDN}$ (MAX223), $\overline{EN}$, SHDN (MAX241)				0.8	V
Input Logic Threshold High	T_{IN}		2.0			
	EN, $\overline{SHDN}$ (MAX223), $\overline{EN}$, SHDN (MAX241)		2.4			V
Logic Pull-Up Current	T_{IN} = 0V			15	200	µA
Receiver Input Voltage Operating Range			-30		+30	V
RS-232 Input Threshold Low	T_A = +25°C, V_{CC} = 5V	Normal Operation $\overline{SHDN}$ = 5V (MAX223), SHDN = 0V (MAX241)	0.8	1.2		V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V (R4, R5)	0.6	1.5		
RS-232 Input Threshold High	T_A = +25°C, V_{CC} = 5V	Normal Operation $\overline{SHDN}$ = 5V (MAX223), SHDN = 0V (MAX241)		1.7	2.4	V
		Shutdown (MAX223) $\overline{SHDN}$ = 0V, EN = 5V (R4, R5)		1.5	2.4	
RS-232 Input Hysteresis	V_{CC} = 5V; no hysteresis in shutdown		0.2	0.5	1.0	V
RS-232 Input Resistance	T_A = +25°C, V_{CC} = 5V		3	5	7	kΩ
TTL/CMOS Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
TTL/CMOS Output Voltage High	I_{OUT} = -1.0mA		3.5	V_{CC} - 0.4		V
TTL/CMOS Output Leakage Current	0V ≤ R_{OUT} ≤ V_{CC}; EN = 0V (MAX223); $\overline{EN}$ = V_{CC} (MAX241)			0.05	±10	µA
Receiver Output Enable Time	Normal operation, Figure 2	MAX223		600		ns
		MAX241		400		
Receiver Output Disable Time	Normal operation, Figure 2	MAX223		900		ns
		MAX241		250		

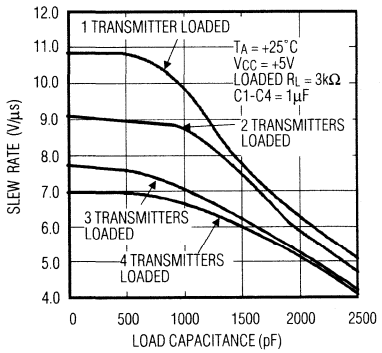
ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.5V to 5.5V, C1 - C4 = 1µF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

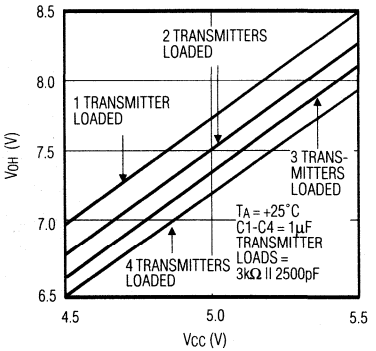
PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Propagation Delay	RS-232 IN to TTL/CMOS OUT, C_L = 150pF	Normal operation			0.5	10	µs
		$\overline{SHDN}$ = 0V (MAX223)	t_{PHLS}		4	40	
			t_{PLHS}		6	40	
Transition Region Slew Rate	T_A = +25°C, V_{CC} = 5V, R_L = 3kΩ to 7kΩ, C_L = 50pF to 2500pF, measured from +3V to -3V or -3V to +3V, Figure 3			3	5.1	30	V/µs
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V			300			Ω
Receiver Out Short-Circuit Current					±10		mA

Typical Operating Characteristics

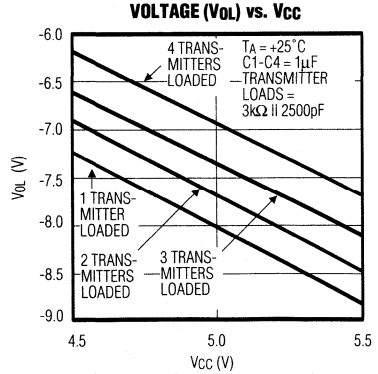
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



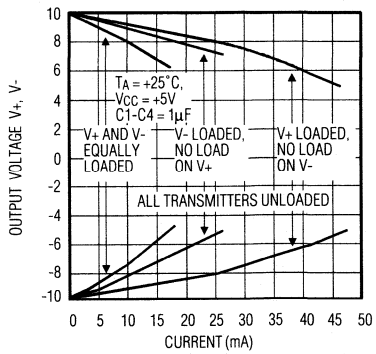
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. V_{CC}



TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. V_{CC}



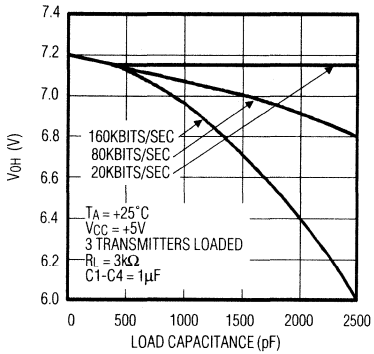
TRANSMITTER OUTPUT VOLTAGE V+, V- vs. LOAD CURRENT



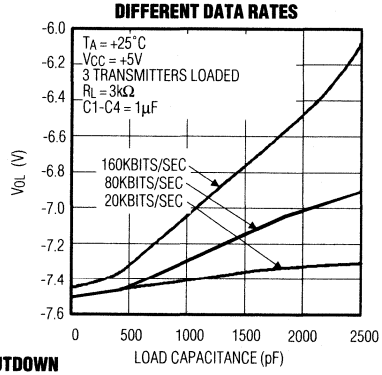
+5V RS-232 Transceiver with Two Receivers Active in Shutdown

Typical Operating Characteristics (continued)

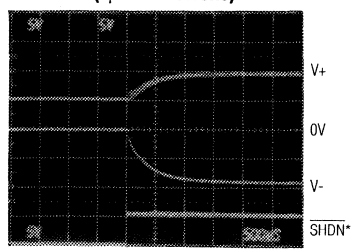
TRANSMITTER OUTPUT VOLTAGE (V_{OH}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



TRANSMITTER OUTPUT VOLTAGE (V_{OL}) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



V+, V- WHEN EXITING SHUTDOWN (1µF CAPACITORS)



*SHUTDOWN POLARITY IS REVERSED FOR THE MAX241

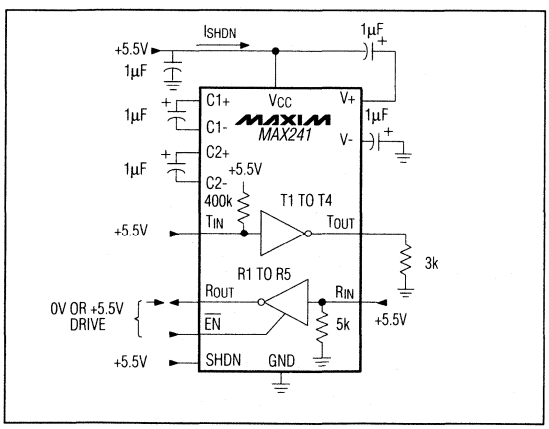


Figure 1. MAX241 Shutdown-Current Test Circuit

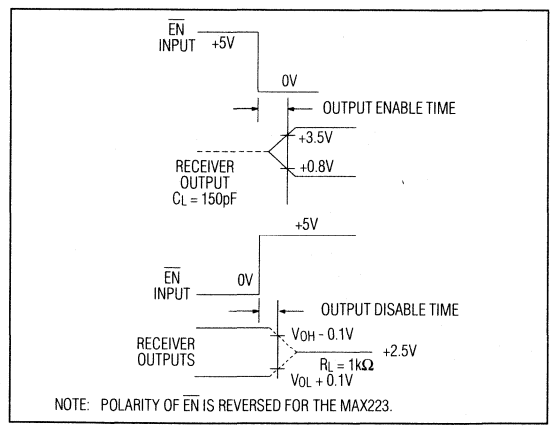


Figure 2. MAX241 Receiver Output Enable and Disable Timing

+5V RS-232 Transceiver with Two Receivers Active in Shutdown

Pin Description

PIN	NAME	FUNCTION		
1, 2, 3, 28	T_OUT	RS-232 Driver Outputs		
4, 9, 18, 23, 27	R_IN	RS-232 Receiver Inputs		
5, 8, 19, 22, 26	R_OUT	TTL/CMOS Receiver Outputs. For the MAX223, receivers R4 and R5 are active in shutdown mode when EN = 1. For the MAX241, all receivers are inactive in shutdown.		
6, 7, 20, 21	T_IN	TTL/CMOS Driver Inputs		
10	GND	Ground		
11	V_{CC}	+4.5V to +5.5V Supply Voltage		
12, 14	C1+, C1-	Terminals for positive charge-pump capacitor		
13	V+	$+2V_{CC}$ voltage generated by the charge pump		
15, 16	C2+, C2-	Terminals for negative charge-pump capacitor		
17	V-	$-2V_{CC}$ voltage generated by the charge pump		
24	EN (MAX223)	Receiver Enable	Active high	See *Shutdown and Enable Control* section.
	$\overline{EN}$ (MAX241)		Active low	
25	$\overline{SHDN}$ (MAX223)	Shutdown Control	Active low	See *Shutdown and Enable Control* section.
	SHDN (MAX241)		Active high	

Detailed Description

The MAX223 and MAX241 consist of three sections: charge-pump voltage converters, drivers (transmitters), and receivers. Each section is described in detail below.

+5V to ±10V Dual Charge-Pump Voltage Converter

The +5V to ±10V conversion is performed by two charge-pump voltage converters (Figure 4). The first uses capacitor C1 to double the +5V to +10V, storing the +10V on the V+ output filter capacitor, C3. The second charge-pump voltage converter uses capacitor C2 to invert the +10V to -10V, storing the -10V on the V- output filter capacitor, C4.

In shutdown mode, V+ is internally connected to V_{CC} by a 1kΩ pull-down resistor and V- is internally connected to ground by a 1kΩ pull-up resistor.

RS-232 Drivers

With V_{CC} = 5V, the typical driver-output voltage swing is ±8V when loaded with a nominal 5kΩ RS-232 receiver. The output swing is guaranteed to meet the EIA-232E/V.28 specification which calls for ±5V minimum output levels under worst-case conditions. These include a minimum 3kΩ load, V_{CC} = 4.5V, and maximum operating temperature. The open-circuit output voltage swing ranges from (V+ - 0.6V) to V-.

Input thresholds are both CMOS and TTL compatible. The inputs of unused drivers can be left unconnected, since 400kΩ pull-up resistors to V_{CC} are included on chip. Since all drivers invert, the pull-up resistors force the outputs of unused drivers low. The input pull-up resistors typically source 15µA, therefore the driver inputs should be driven high or open circuited to minimize power-supply current in shutdown mode.

When in low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V, the transmitter input is diode clamped to ground with a 1kΩ series impedance. The transmitter input is also zener clamped to approximately (V_{CC} + 6V), with a series impedance of 1kΩ.

RS-232 Receivers

The receivers convert the RS-232 signals to CMOS logic output levels. The receiver outputs are inverting, maintaining compatibility with the driver outputs. The guaranteed receiver input thresholds of 0.8V (0.6V in shutdown for the MAX223) and 2.4V are significantly tighter than the ±3.0V thresholds required by the EIA/TIA-232E specification. This allows the receiver inputs to respond to TTL/CMOS logic levels, as well as RS-232 levels.

The MAX223/MAX241's guaranteed 0.8V threshold ensures that receivers shorted to ground will have a logic 1 output. Also, the 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

The receiver inputs have approximately 0.5V hysteresis. This provides clean output transitions, even with slow rise and fall time input signals with moderate amounts of noise and ringing. In shutdown, the MAX223 receivers R4 and R5 have no hysteresis.

+5V RS-232 Transceiver with Two Receivers Active in Shutdown

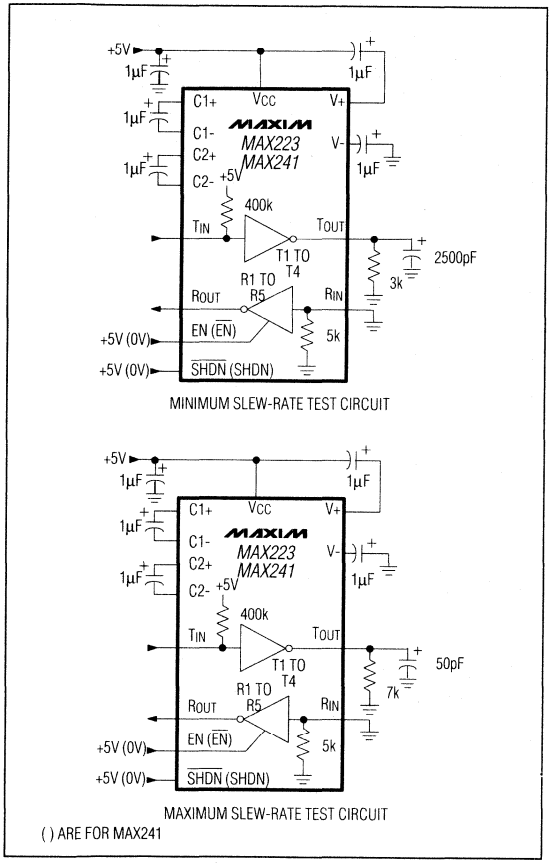


Figure 3. Transition Slew-Rate Test Circuit

Shutdown and Enable Control

The polarity of the receiver enable and shutdown logic levels for the MAX223 are the inverse of those for the MAX241.

Tables 1a and 1b show the polarity of the shutdown and enable controls for the MAX223/MAX241.

Table 1a. MAX223 Control Pin Configurations

$\overline{SHDN}$	EN	OPERATION STATUS	TRANSMITTERS	RECEIVERS	
			T1-T4	R1-R3	R4, R5
0	0	Shutdown	All 3-State	3-State	3-State
0	1	Shutdown	All 3-State	3-State	Active
1	0	Normal Operation	All Active	3-State	3-State
1	1	Normal Operation	All Active	Active	Active

Table 1b. MAX241 Control Pin Configurations

SHDN	$\overline{EN}$	OPERATION STATUS	TRANSMITTERS	RECEIVERS
			T1-T4	R1-R5
0	0	Normal Operation	All Active	All Active
0	1	Normal Operation	All Active	All 3-State
1	0	Shutdown	All 3-State	All 3-State
1	1	Shutdown	All 3-State	All 3-State

In shutdown mode, the MAX233/MAX241 charge pumps are turned off, V+ is pulled down to VCC, V- is pulled to ground, the receiver outputs are put into a high-impedance state (R4 and R5 status depends on the EN pin if using the MAX223), and the transmitter outputs are disabled. This reduces the supply current to under 15µA for the MAX223 and under 1µA for the MAX241. The time required to exit shutdown is 1ms and is shown in the *Typical Operating Characteristics*.

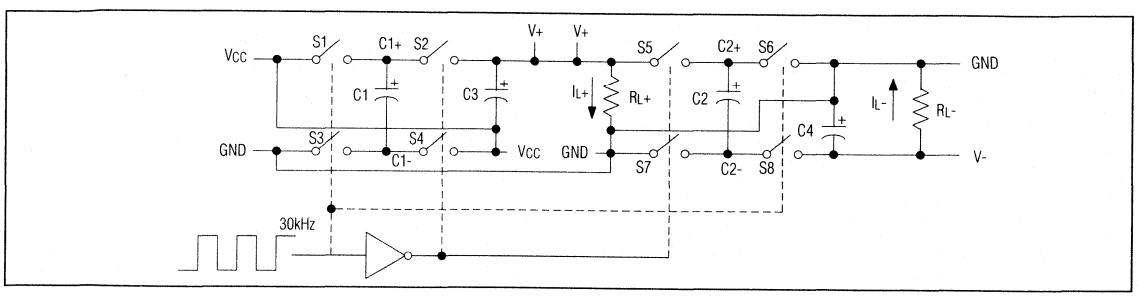


Figure 4. Charge-Pump Diagram

+5V RS-232 Transceiver with Two Receivers Active in Shutdown

Applications Information

Capacitor Selection

The type of capacitor used is not critical for proper operation of the MAX223/MAX241. Aluminum electrolytic, ceramic or tantalum capacitors are suggested. To ensure proper RS-232 signal levels over temperature when using 1µF capacitors, make sure the capacitance value does not degrade excessively as the temperature varies. If in doubt, use capacitors with a larger nominal value. Also observe the ESR (effective series resistance) value of the capacitors over temperature, since it will influence the amount of ripple on V+ and V-. To reduce the output impedance at V+ and V-, use larger capacitors (up to 10µF).

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple receivers.

Driver Outputs when Exiting Shutdown

Figure 5 shows the MAX223/MAX241 driver outputs when exiting shutdown mode. As they become active, the two driver outputs are shown going to opposite RS-232 levels (one driver input is high, the other is low). Each driver is loaded with 3kΩ in parallel with 2500pF. The driver outputs display no ringing or undesirable transients as they come out of shutdown.

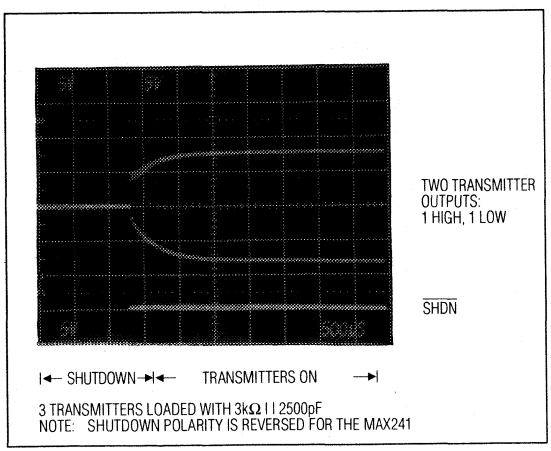


Figure 5. Transmitter Outputs When Exiting Shutdown

MAX223 Receiver Operation in Shutdown

During normal operation, the MAX223's receiver propagation delay is 0.5µs. When entering shutdown with receivers active, R4 and R5 are not valid until 80µs after $\overline{SHDN}$ is driven low. In shutdown mode, propagation delays increase to about 5µs for a high-to-low or low-to-high transition (V_{CC} = +5V) as shown in Figure 6.

Regardless of the status of the EN pin, receiver outputs R1, R2 and R3 are inactive.

When exiting shutdown, all receiver outputs are invalid until the charge pumps reach nominal values (<2ms) when using 1µF capacitors.

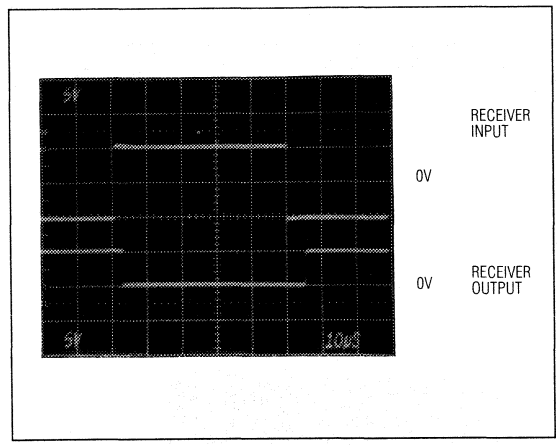


Figure 6. MAX223 Receiver R4, R5 Propagation Delay in Shutdown

Power-Supply Decoupling

In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitors.

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce noise margins. See the Output Voltage vs. Load Current graph in the *Typical Operating Characteristics*.

High Data Rates

The MAX223/MAX241 maintain the RS-232 ±5.0V minimum driver output voltage even at high data rates. Figure 6 shows one of three transmitter outputs driving 3kΩ II 2500pF loads at 120kbits/sec.

+5V RS-232 Transceiver with Two Receivers Active in Shutdown

Table 2. Summary of EIA/TIA-232E, V.28 Specifications

PARAMETER	CONDITION	EIA/TIA-232E, V.28 SPECIFICATION
Driver Output Voltage 0 Level 1 Level Output Level, Max	 3kΩ to 7kΩ load 3kΩ to 7kΩ load No load	 +5.0V to +15V -5.0V to -15V ±25V
Data Rate	3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	Up to 20kbits/sec
Receiver Input Voltage 0 Level 1 Level Input Level, Max		 +3.0V to +15V -3.0V to -15V ±25V
Instantaneous Slew Rate, Max	3kΩ ≤ R_L ≤ 7kΩ, C_L ≤ 2500pF	30V/µs
Driver Output Short-Circuit Current, Max		100mA
Transition Rate on Driver Output	V.28	1ms or 3% of the period
	EIA/TIA-232E	4% of the period
Driver Output Resistance	-2V < V_{OUT} < +2V	300Ω

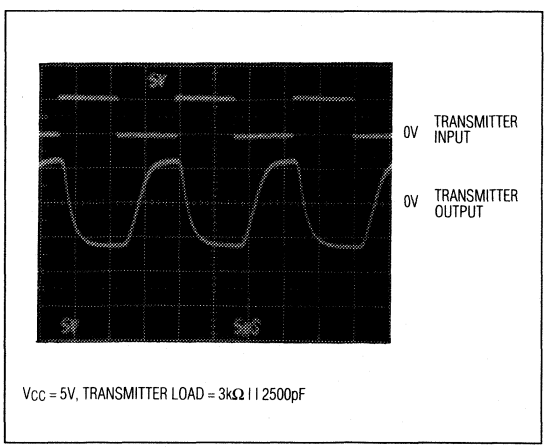


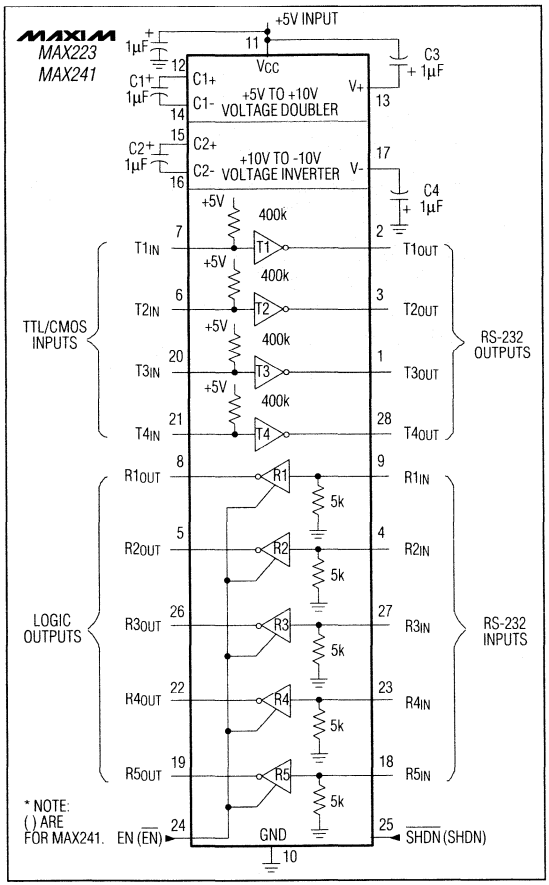
Figure 7. Transmitter Output at 120kbits/sec Driving 3 Transmitters

Table 3. DB9 Cable Connections Commonly Used for EIA/TIA-232E and V.24 Asynchronous Interfaces

PIN	CONNECTION	
1	Received Line Signal Detector (sometimes called Carrier Detect, DCD)	Handshake from DCE
2	Receive Data (RD)	Data from DCE
3	Transmit Data (TD)	Data from DTE
4	Data Terminal Ready	Handshake from DTE
5	Signal Ground	Reference point for signals
6	Data Set Ready (DSR)	Handshake from DCE
7	Request to Send (RTS)	Handshake from DTE
8	Clear to Send (CTS)	Handshake from DCE
9	Ring Indicator	Handshake from DCE

+5V RS-232 Transceiver with Two Receivers Active in Shutdown

Typical Operating Circuit



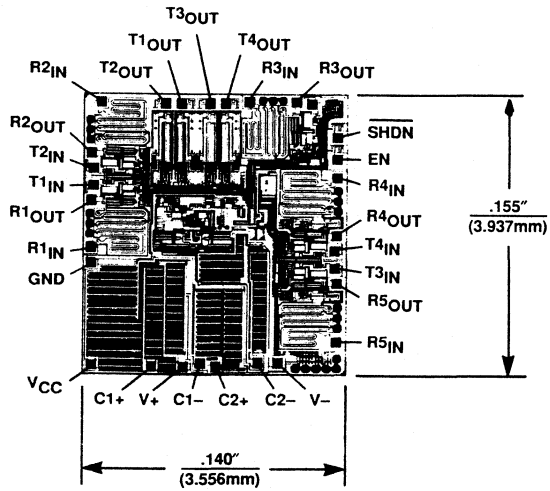
+5V RS-232 Transceiver with Two Receivers Active in Shutdown

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX241CWI	0°C to +70°C	28 Wide SO
MAX241CAI	0°C to +70°C	28 SSOP
MAX241C/D	0°C to +70°C	Dice*
MAX241EWI	-40°C to +85°C	28 Wide SO
MAX241EAI	-40°C to +85°C	28 SSOP

*Dice are specified at T_A = +25°C.

Chip Topography



19-0015; Rev 0; 5/92

MAXIM

+3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown

General Description

The MAX560/MAX561 are the first +3.3V-powered devices to implement the EIA/TIA-562 standard, which guarantees interoperability with RS-232 interfaces. The MAX560/MAX561 are guaranteed to operate with a +3.0V power supply at a 20kbits/sec data rate while maintaining ±3.7V EIA/TIA-562 signal levels.

The MAX560/MAX561 include four line drivers, five receivers, a shutdown mode, and a receiver-enable input. An on-board charge-pump voltage converter converts the +3.3V input to the ±6.6V needed to comply with the EIA/TIA-562 output levels. The MAX560 has an active-low shutdown and an active-high receiver enable. In shutdown mode, two receivers are active, allowing unidirectional communication for peripheral monitoring. The MAX561 has an active-high shutdown and an active-low receiver enable. In shutdown mode, all receivers are in a high-impedance, three-state mode.

The MAX560/MAX561 are available in a standard 28-pin wide small outline (SO) package and a 28-pin shrink small outline package (SSOP), which requires 40% of the board space of the SO package. Each operates with four 1µF capacitors, further reducing board space.

Applications

Laptop Computers
Palmtop Computers
Notebook Computers
Battery-Powered Equipment

Features

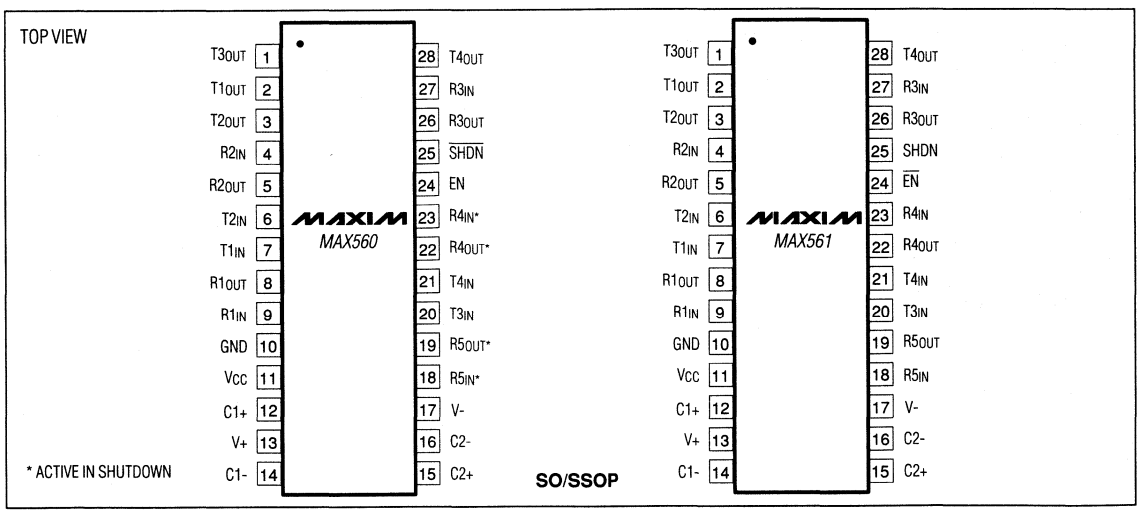
- ♦ **2 Receivers Active in Shutdown Mode (MAX560)**
- ♦ **Small 28-pin SSOP Package – 40% the Area of SO Package**
- ♦ **Guaranteed Interoperability with RS-232**
- ♦ **Operate from a Single +3.0V to +3.6V Supply**
- ♦ **Designed for EIA/TIA-562 Applications**
- ♦ **4 Drivers/5 Receivers**
- ♦ **Low-Power Shutdown:**
  <8µA MAX560
  <1µA MAX561
- ♦ **Three-State TTL/CMOS Receiver Outputs**
- ♦ **116kbits/sec Data Rate**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX560CWI	0°C to +70°C	28 Wide SO
MAX560CAI	0°C to +70°C	28 SSOP
MAX560C/D	0°C to +70°C	Dice*
MAX561CWI	0°C to +70°C	28 Wide SO
MAX561CAI	0°C to +70°C	28 SSOP
MAX561C/D	0°C to +70°C	Dice*

*Dice are specified at T_A = +25°C.

Pin Configurations



Typical operating circuit on last page

+3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown

ABSOLUTE MAXIMUM RATINGS

V_{CC} ..... -0.3V to +6V
V+ ..... (V_{CC} - 0.3V) to +14V
V- ..... +0.3V to -14V
Input Voltages
T_{IN} ..... 0.3V to (V_{CC} + 0.3V)
R_{IN} ..... ±25V
Output Voltages
T_{OUT} ..... (V+ + 0.3V) to (V- - 0.3V)
R_{OUT} ..... -0.3V to (V_{CC} + 0.3V)

Short-Circuit Duration
T_{OUT} ..... Continuous
Continuous Power Dissipation
Wide SO (derate 12.50mW/°C above +70°C) 1000mW
SSOP (derate 9.52mW/°C above +70°C) 762mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +3.0V to +3.6V, C1 - C4 = 1µF, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Swing	3 transmitter outputs loaded with 3kΩ to ground (T1, T2, and T3)		±3.7	±4.2		V
	V_{CC} = 3.3V, 4 transmitter outputs loaded with 3kΩ to ground		±3.7	±4.5		
V_{CC} Power-Supply Current	No load, T_A = +25°C			5	8	mA
Shutdown Supply Current	Figure 1, T_A = +25°C	MAX560		8	50	µA
		MAX561		1	10	
Input Logic Threshold Low	T_{IN}, EN, $\overline{SHDN}$ (MAX560), SHDN (MAX561)				0.4	V
Input Logic Threshold High	T_{IN}, EN, $\overline{SHDN}$ (MAX560), SHDN (MAX561)		2.4			V
Logic Pull-Up Current	T_{IN} = 0V			6	135	µA
Receiver Input Voltage Operating Range			-25		25	V
EIA/TIA-562 Input Threshold Low	Normal operation		0.4	0.8		V
	$\overline{SHDN}$ = 0V, ($R4_{IN}$, $R5_{IN}$)	MAX560	0.4	1.4		
EIA/TIA-562 Input Threshold High	Normal operation			1.1	2.4	V
	$\overline{SHDN}$ = 0V, ($R4_{IN}$, $R5_{IN}$)	MAX560		1.4	2.4	
EIA/TIA-562 Input Hysteresis	No hysteresis when $\overline{SHDN}$ = 0V	MAX560		0.3		V
EIA/TIA-562 Input Resistance	T_A = +25°C, V_{CC} = 3.3V		3	5	7	kΩ
CMOS Output Voltage Low	I_{OUT} = 1.6mA				0.4	V
CMOS Output Voltage High	I_{OUT} = -40µA		2.8	V_{CC} - 0.1		V
CMOS Output Leakage Current	EN = V_{CC}, 0V ≤ R_{OUT} ≤ V_{CC}			0.05	±10	µA
Output Enable Time	Figure 2, T_A = +25°C			800		ns
Output Disable Time		MAX560		1500		ns
		MAX561		500		

+3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown

ELECTRICAL CHARACTERISTICS (continued)

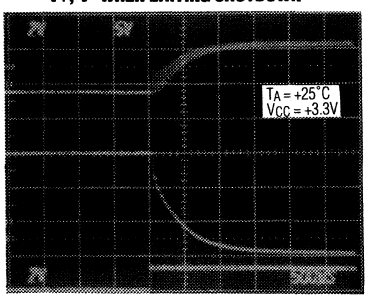
(V_{CC} = 3.0V to 3.6V, C1 - C4 = 1µF, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Propagation Delay	Receiver IN to Receiver OUT, C_L = 150pF	Normal operation			1.0	10	µs
		MAX560 SHDN = 0V	t_{PHLS}		4	40	
			t_{PLHS}		6	40	
Instantaneous Slew Rate	C_L = 50pF, R_L = 3kΩ to 7kΩ, T_A = +25°C (Note 1)					30	V/µs
Transition Region Slew Rate	R_L = 3kΩ, C_L = 2500pF, Measured from +3V to -3V or -3V to +3V				2.5		V/µs
Transmitter Output Resistance	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V			300			Ω
Receiver Out Short-Circuit Current					±10		mA

Note 1: Guaranteed by design

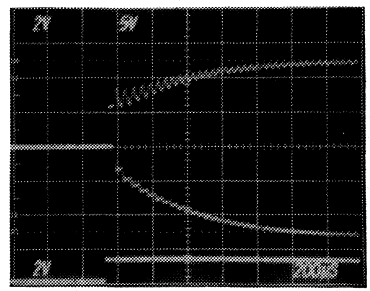
Typical Operating Characteristics

MAX560
V+, V- WHEN EXITING SHUTDOWN



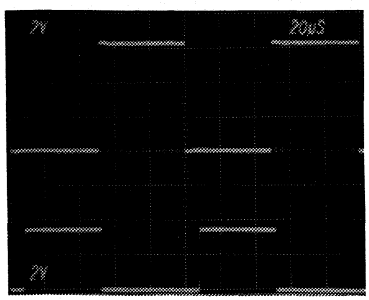
3 TRANSMITTERS LOADED WITH 3kΩ II 2500pF

MAX560
TRANSMITTER OUTPUTS WHEN EXITING SHUTDOWN

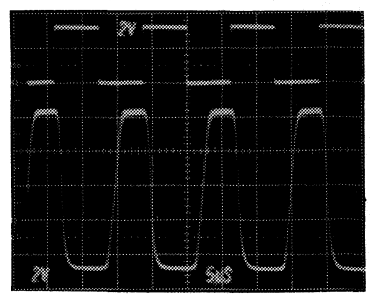


3 TRANSMITTERS LOADED WITH 3kΩ II 2500pF

MAX560
RECEIVER PROPAGATION DELAY IN SHUTDOWN



TRANSMITTER OUTPUT AT 160KBITS/SEC DRIVING 3 TRANSMITTERS

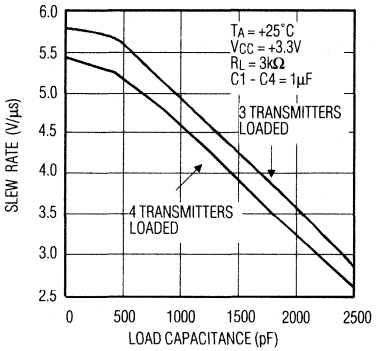


3 TRANSMITTERS LOADED WITH 3kΩ II 1000pF

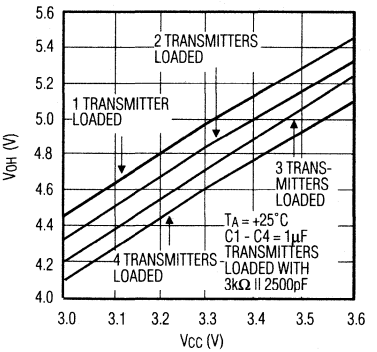
+3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown

Typical Operating Characteristics (continued)

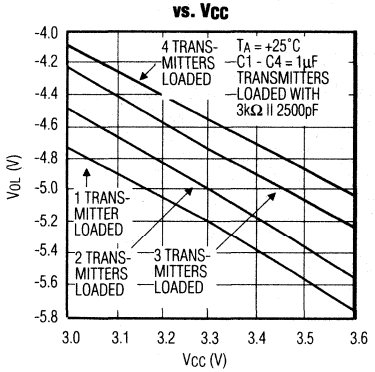
TRANSMITTER SLEW RATE vs. LOAD CAPACITANCE



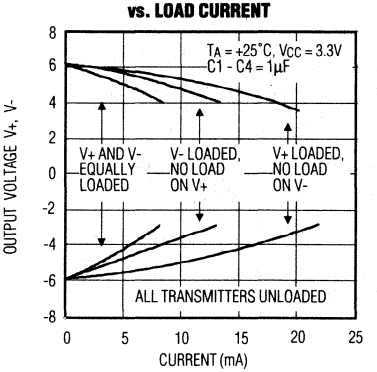
TRANSMITTER OUTPUT VOLTAGE (VOH) vs. VCC



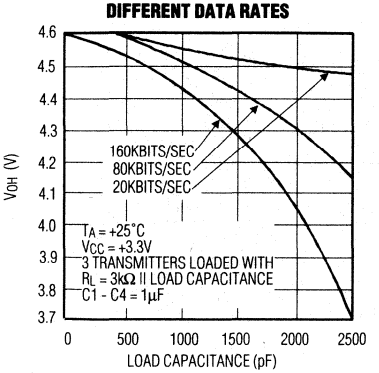
TRANSMITTER OUTPUT VOLTAGE (VOL) vs. VCC



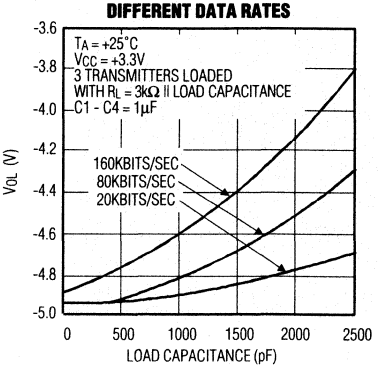
OUTPUT VOLTAGE V+, V- vs. LOAD CURRENT



TRANSMITTER OUTPUT VOLTAGE (VOH) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



TRANSMITTER OUTPUT VOLTAGE (VOL) vs. LOAD CAPACITANCE AT DIFFERENT DATA RATES



+3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown

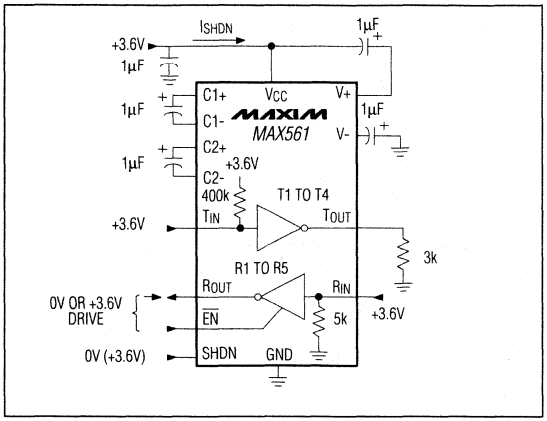


Figure 1. MAX561 Shutdown-Current Test Circuit

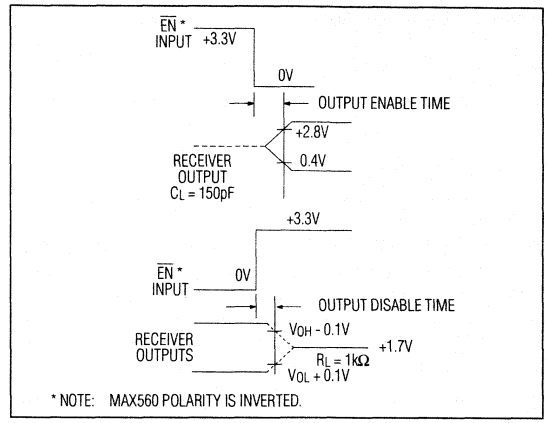


Figure 2. Receiver Output Enable and Disable Timing

Pin Description

PIN	NAME	FUNCTION		
1, 2, 3, 28	T_OUT	EIA/TIA-562 Voltage-Level Driver Outputs		
4, 9, 18, 23, 27	R_IN	EIA/TIA-562 Voltage-Level Receiver Inputs		
5, 8, 19, 22, 26	R_OUT	CMOS Receiver Outputs. When using the MAX560, receivers R4 and R5 are active in shutdown mode when EN = 1. When using the MAX561, all receivers are inactive in shutdown.		
6, 7, 20, 21	T_IN	CMOS Driver Inputs		
10	GND	Ground		
11	VCC	+3.0V to +3.6V Supply Voltage		
12, 14	C1+, C1-	Terminals for positive charge-pump capacitor		
13	V+	+2VCC Voltage generated by the charge pump		
15, 16	C2+, C2-	Terminals for negative charge-pump capacitor		
17	V-	-2VCC Voltage generated by the charge pump		
24	EN (MAX560)	Receiver Enable	Active high	See *Shutdown and Enable Control* section.
	$\overline{EN}$ (MAX561)		Active low	
25	$\overline{SHDN}$ (MAX560)	Shutdown Control	Active low	See *Shutdown and Enable Control* section.
	SHDN (MAX561)		Active high	

Detailed Description

The MAX560/MAX561 consist of three sections: charge-pump voltage converters, transmitters (drivers), and receivers. Each section is described in detail below.

+3.3V to ±6.6V Dual Charge-Pump Voltage Converter

The +3.3V to ±6.6V conversion is performed by two charge-pump voltage converters (Figure 3). The first uses capacitor C1 to double the +3.3V to +6.6V, storing the +6.6V on the V+ output filter capacitor, C3. The second charge-pump voltage converter uses capacitor C2 to invert the +6.6V to -6.6V, storing the -6.6V on the V- output filter capacitor, C4.

In shutdown mode, V+ is internally connected to VCC by a 1kΩ pull-down resistor and V- is internally connected to ground by a 1kΩ pull-up resistor.

EIA/TIA-562 Drivers

The drivers are inverting level translators that convert +3V logic input levels to EIA/TIA-562 voltage levels. The driver outputs are inverting since the EIA/TIA-562 specification defines a receiver input voltage level greater than +3V as a 0, and a voltage level less than -3V as a 1. With

+3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown

Table 1. Receiver Operation and Control

	MAX560	MAX561
Normal Operation	$\overline{SHDN}$ = 1: receivers active (EN = 1), receivers inactive (EN = 0)	SHDN = 0: receivers active ($\overline{EN}$ = 0), receivers inactive (EN = 1)
Shutdown Mode	$\overline{SHDN}$ = 0: receivers R1-R3 inactive (EN = 1), receivers R4 and R5 active (EN = 1), receivers R1-R5 inactive (EN = 0)	SHDN = 1: receivers inactive ($\overline{EN}$ = 0), receivers inactive (EN = 1)

V_{CC} = +3.0V, the typical output voltage swing is 4.1V when driving three transmitters, each with the worst-case 3kΩ load. Under such conditions, the output swing is guaranteed to meet the EIA/TIA-562 minimum specification of 3.7V output voltage swing. The open-circuit output voltage swings from (V+ - 0.6V) to V-.

The inputs of unused driver sections should be connected to V_{CC}, but can be left unconnected; an internal 400kΩ input pull-up resistor to V_{CC} will pull the inputs high, forcing unused transmitter outputs low. The input pull-up resistors typically source 6µA; therefore, the driver inputs should be driven high or open circuited to minimize power-supply current in shutdown mode.

When in the low-power shutdown mode, the driver outputs are turned off and their leakage current is less than 1µA with the driver output pulled to ground. The driver output leakage remains less than 1µA, even if the transmitter output is backdriven between 0V and (V_{CC} + 6V). Below -0.5V, the transmitter input is diode clamped to ground with a 1kΩ series impedance. The transmitter input is also zener clamped to approximately (V_{CC} + 6V), with a 1kΩ series impedance.

EIA/TIA-562 Receivers

The receivers convert ±3.7V to ±13.2V EIA/TIA-562 level signals to +3V logic output levels. The receiver outputs are inverting, maintaining compatibility with the driver outputs. Maxim has set guaranteed receiver input thresholds of 0.4V and 2.4V, which are significantly tighter than the ±3.0V thresholds required by the EIA/TIA-562 specification. This allows the receivers to respond to +3V logic levels as well as EIA/TIA-562 levels.

The MAX560/MAX561's guaranteed 0.4V lower threshold ensures that a receiver shorted to ground will have a logic 1 output. The 5kΩ input resistance to ground ensures that a receiver with its input left open will also have a logic 1 output.

The receivers have approximately 0.3V hysteresis. This provides clean output transitions, even with slow rise and fall time input signals with moderate amounts of noise and ringing. In shutdown, the MAX560 receivers R4 and R5 have no hysteresis.

Shutdown and Enable Control

THE POLARITY OF THE RECEIVER ENABLE AND SHUTDOWN LOGIC LEVELS FOR THE MAX560 ARE THE INVERSE OF THOSE FOR THE MAX561.

Table 1 shows the polarity of the shutdown and enable controls for the MAX560/MAX561.

In shutdown mode, the MAX560/MAX561 charge pump is turned off, V+ is pulled down to V_{CC}, and V- is pulled to ground. Also, the receiver outputs are put into a high-impedance state (R4 and R5 status depend on the EN pin if using the MAX560) and the transmitter outputs are disabled. This drops the supply current to approximately 8µA for the MAX560 and 1µA for the MAX561. The time required to exit shutdown is typically 1ms, as shown in the *Typical Operating Characteristics* graphs.

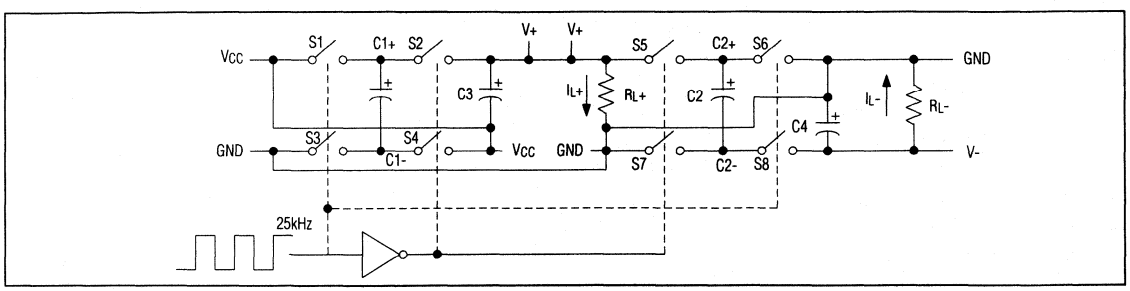


Figure 3. Charge Pump

+3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown

Applications Information

Capacitor Selection

The type of capacitor used is not critical for proper MAX560/MAX561 operation. Aluminum electrolytic, ceramic, or tantalum capacitors are suggested. To ensure proper EIA/TIA-562 signal levels over temperature when using 1µF capacitors, make sure the capacitance value does not degrade excessively as the temperature varies. If in doubt, use capacitors with a larger nominal value. Also observe the effective series resistance (ESR) value of the capacitors over temperature, since it will influence the amount of ripple on V+ and V-. To reduce the output impedance at V+ and V-, larger capacitors (up to 10µF) can be used.

Driving Multiple Receivers

Each transmitter is designed to drive a single receiver. Transmitters can be paralleled to drive multiple recievers.

Transmitter Outputs when Exiting Shutdown

The *Typical Operating Characteristics* section shows the reaction of the MAX560 transmitter outputs when exiting shutdown. Two transmitter outputs are shown going to opposite RS-232 levels as they become active (one transmitter is high, the other low). Each transmitter is loaded with 3kΩ in parallel with 2500pF. The transmitter outputs display no ringing or undesirable transients as they come out of shutdown.

MAX560 Receiver Operation in Shutdown

During normal operation, the MAX560's receiver propagation delay is typically 1µs. When entering shutdown with the receiver active, the receiver outputs R4 and R5 are not valid until 80µs after $\overline{SHDN}$ is driven low. In shutdown mode, propagation delay increases to a typical 4µs for a high to low transition and 6µs for a low to high transition (V_{CC} = +3.3V), as shown in the Receiver Propagation Delay in Shutdown graph in the *Typical Operating Characteristics*. Irrespective of EN, receiver outputs R1, R2, and R3 are inactive in shutdown. When exiting shutdown, all receiver outputs are invalid until the charge pumps reach nominal levels (500µs when using 1µF capacitors).

Power-Supply Decoupling

In applications that are sensitive to power-supply noise, decouple V_{CC} to ground with a capacitor of the same value as the charge-pump capacitors.

V+ and V- as Power Supplies

A small amount of power can be drawn from V+ and V-, although this will reduce transmitter noise margins. See the Output Voltage vs. Load Current graph in the *Typical Operating Characteristics* section.

High Data Rates

The MAX560/MAX561 maintain the EIA/TIA-562 ±3.7V minimum transmitter output voltage even at high data rates. The *Typical Operating Characteristics* show a transmitter output at 160kbits/sec.

EIA/TIA Standards

Before the MAX232 was invented, many "quasi" RS-232 interfaces were implemented with ±5.0V power supplies. Output levels from the transmitters often failed to meet the RS-232 specifications, but the interfaces were functional over short distances, often at data rates above 20kbits/sec, due to the RS-232's 2V margin between its ±5V minimum transmitter output specification and the ±3V receiver input specification. The advent of +3V-powered systems led to the creation of the EIA/TIA-562 specification. Table 2 summarizes both specifications.

Table 2. Summary of EIA/TIA-232E/V.28 and EIA/TIA-562 Specifications

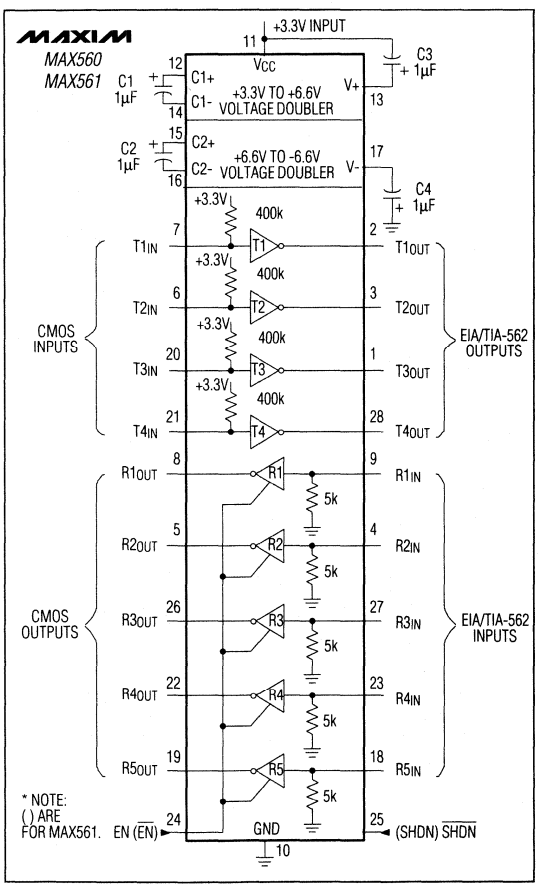
PARAMETER	CONDITION	EIA/TIA-232E/V.28 SPECIFICATION	EIA/TIA-562 SPECIFICATION
Driver Output Voltage			
0 Level	3kΩ to 7kΩ Load	5.0V to 15.0V	3.7V to 13.2V
1 Level		-5.0V to -15.0V	-3.7V to -13.2V
Maximum Output Level	No load	±25V	±13.2V
Signal Rate (3kΩ ≤ R_L ≤ 7kΩ)	C_L = 2500pF	Up to 20kbits/sec	Up to 20kbits/sec
	C_L = 1000pF	Not defined	Up to 64kbits/sec

+3.3V Transceiver with Two EIA/TIA-562 Receivers Active in Shutdown

Table 2. Summary of EIA/TIA-232E/V.28 and EIA/TIA-562 Specifications (continued)

PARAMETER	CONDITION	EIA/TIA-232E/V.28 SPECIFICATION	EIA/TIA-562 SPECIFICATION
Receiver Input Thresholds			
0 Level		3.0V to 15.0V	3.0V to 15.0V
1 Level		-3.0V to -15.0V	-3.0V to -15.0V
Maximum Input Level		±25V	±25V
Maximum Instantaneous Slew Rate		30V/µs	30V/µs
Maximum Driver Output Short-Circuit Current		100mA	60mA
Transition Rate on Driver Output		V.28 1ms or 3% of the period	4V/µs
		RS-232 4% of the period	
Driver Output Resistance with Power Off	-2V < V_{OUT} < 2V	300Ω	300Ω

Typical Operating Circuit



Op Amps/Buffers/Comparators

* Advance Information – first page of data sheet in preparation.

Part Number	V_{OS} (mV max)	TCV_{OS} (µV/°C max)	I_{BIAS} (nA max)	Unity GBW (MHz)	Supply Voltage (V)	Supply Current (mA max)	Features	Price† 1000-up ($)
MAX400	10 to 15µV	0.3	2	0.4	±3 to ±18	4	Ultra-low V_{OS} & drift non-chopper stabilized	5.16
MAX402	2	25	5	2/6(Av≥5)	±5	75µA	High-speed,micropower	1.98
MAX403	2	33	25	10/30(Av≥5)	±5	375µA	High-speed, micropower	2.75
MAX406	0.5 to 2.0	10	10pA	0.008 to 0.040	+2.5 to +10	1.2µA	Lowest power, single supply, output swings rail-to-rail	2.54
MAX407	1.0 to 3.0	10	10pA	0.04	+2.5 to +10	1.2µA/amp.	Dual MAX406, unity-gain stable	††
MAX408/428/448	6 to 12	15 to 20	1.1µA	100 (Av ≥ 3)	±5	10/amp.	Single/dual/quad high-speed, high output current	3.072/4.06/6.74
MAX409	3	-	10pA	150kHz (Av≥10V/V)	+2.5 to +10	1.2µA	High-speed, decompensated MAX406	††
MAX410/412/414	250µV	1.0	150	28	±2.4 to ±5	2.62/amp.	Single/dual/quad, high-speed, low noise, <2.4nV/√Hz at 1kHz guaranteed, unity-gain stable	††/2.98/††
MAX420/422	5 to 10µV	0.05	0.03 to 0.10	0.125 to 0.5	±15	0.5 to 2	±15V chopper stabilized	3.77/4.21
MAX421/423	5 to 10µV	0.05	0.03 to 0.10	0.125 to 0.5	±15	0.5 to 2	±15V chopper stabilized with clamped output and INT/EXT clock option	4.21/5.57
MAX430/432	5µV	0.05	0.1	0.125 to 0.5	±15	0.5 to 2	±15V chopper stabilized with internal caps	4.80/5.29
MAX438	2	25 typ	5	6(Av≥5V/V)	±5	75µA	High-speed,micropower; 10V/µs slew rate	1.98
MAX439	2	25 typ	25	25(Av≥5V/V)	±5	375µA	High-speed,micropower; 48V/µs slew rate	2.75
MAX480	70µV	1.5	3	0.02	±0.8 to ±18 ±1.6 to ±36	15µA	Low V_{OS} & drift, micropower, single supply, input/output extend to negative rail	3.68
LH0101	3 to 10	10 typ	300 to 1k	5	±5 to ±15	35	5A peak power op amp	18.98
MAX427/437	15µV	0.6	40	8/63 (Av≥5V/V)	±4 to ±18	4.7	High-speed, low noise, 3nV/√Hz precision	††
ICL7611	2 to 15	10 to 25	0.05	0.044 to 1.4	±1.0 to ±8	0.02 to 2.5	Programmable quiescent current	1.58
ICL7612	5 to 15	15 to 25	0.05	0.044 to 1.4	±1.0 to ±8	0.02 to 2.5	Programmable quiescent current, rail-to-rail input and output	1.81
ICL7614	2 to 15	15 to 25	0.05	0.48*	±1.0 to ±8	0.25	External compensation	0.95
ICL7616	2 to 15	15 to 25	0.05	0.044 to 1.4	±1.0 to ±8	0.02 to 2.5	Programmable quiescent current, extended CMVR	1.62
ICL7621/7622	5 to 15	15 to 25	0.05	0.48	±1.0 to ±8	0.25	Dual, low I_{BIAS} & I_{OS}	1.55/1.48
ICL7631/7632	5 to 20	15 to 30	0.05	0.044 to 1.4	±1.0 to ±8	0.022 to 2.5	Triple op amp, programmable quiescent current–ICL7632 is externally compensated	2.27/2.12
ICL7641/7642	5 to 25	15 to 30	0.05	0.044 to 1.4	±1.0 to ±8	0.015 to 2.5	Quad	1.70/1.91
ICL7650	5 to 10µV	0.05 to 0.10	0.01 to 0.02	2	±5	2	Industry-standard chopper stabilized	2.39
ICL7652	5 to 10µV	0.05	0.03	0.45	±5	2	Low noise, industry-standard, chopper stabilized	3.06

* External 39pF compensation capacitor added.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.

Op Amps (continued)

Part Number	Vos (µV max)	TCVos (µV/°C max)	IBIAS (nA max)	Unity GBW (MHz)	Supply Voltage (V)	Supply Current (mA max)	Features	Price† 1000-up ($)
LT1001	15 to 60	0.6 to 1	2 to 4	0.8	±3 to ±18	2	Industry-standard precision	1.73
LT1028	40 to 80	0.8 to 1	90 to 180	75 (Av > 2)	±4 to ±18	9.5 to 10.5	Lowest noise, high-speed	4.21
OP07	25 to 150	0.6 to 2.5	2 to 12	0.6	±3 to ±18	4	Industry-standard precision	1.58
OP27	25 to 100	0.6 to 1.8	40 to 80	8	±3 to ±18	4.6 to 5.6	Industry-standard low noise	††
OP37	25 to 100	0.6 to 1.8	40 to 80	63 (Av ≥ 5)	±3 to ±18	4.6 to 5.6	Industry-standard low noise	††
OP90	150 to 450	2 to 5	15 to 25	0.020	±0.8 to ±18 ±1.6 to ±36	15 to 20µA	Industry-standard micropower	1.60
PGA100	1mV	6 typ	0.1 typ	5	æ15	27 (I_{cc})		56.14

Comparators

Part Number	# Comps	Logic	Latched Outputs	Supply Current (mA max)	Tpd (ns typ)	Features	Price† 1000-up ($)
HIGH SPEED							
MAX900	4	TTL	Yes	15 (I_{cc})	8.0	Single +5V capability, low power, CMVR extends to neg. rail, separate analog & digital supplies, internal pull-up resistors	7.01
MAX901	4	TTL	No	15 (I_{cc})	8.0	MAX900 without output latch	5.98
MAX902	2	TTL	Yes	8 (I_{cc})	8.0	Dual MAX900	4.01
MAX903	1	TTL	Yes	4 (I_{cc})	8.0	Single MAX900	3.15
MAX905	1	ECL	Yes	24 (I_{ee})	1.8	Edge-triggered master/slave architecture eliminates oscillations and resolves 3mV input voltages	3.58
MAX906	2	ECL	Yes	48 (I_{ee})	1.8	Dual MAX905	5.29
MAX907	2	TTL	No	475µA/comp.	30	High speed, ultra low power, single +5V, 8-pin DIP/SO, 2mV hysteresis	††
MAX908	4	TTL	No	475µA/comp.	30	High speed, ultra low power, single +5V, 14-pin DIP/SO, 2mV hysteresis	††
MAX910	1	TTL	Yes	30 (I_{cc})	8.0	TTL-compatible, 8-bit digitally programmable input voltage threshold, on-board reference	5.20
MAX911	1	ECL	Yes	30 (I_{cc})	4.0	MAX910 with differential ECL outputs	5.20
MAX9685	1	ECL	Yes	32 (I_{ee})	1.3	Higher speed industry-standard	3.38
MAX9686	1	TTL	Yes	25 (I_{cc})	6.0	Higher speed industry-standard	2.31
MAX9687	2	ECL	Yes	68 (I_{ee})	1.4	Higher speed industry-standard	5.12
MAX9690	1	ECL	No	32 (I_{ee})	1.3	8-lead PDIP/SO	3.29
MAX9698	2	TTL	Yes	50 (I_{cc})	6.0	Higher speed industry-standard	3.92
SPECIAL							

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.

COMPARATORS

SPECIAL

★ **MAX516**
(quad, programmable VTH)

HIGH-SPEED COMPARATORS

TTL OUTPUT

MAX900 (quad, single supply)
MAX901 (quad, single supply)
★ **MAX902** (dual, single or dual supply)
★ **MAX903** (single or dual supply)
★ **MAX907** (dual, single supply, low power)
★ **MAX908** (quad, single supply, low power)
★ **MAX910** (programmable VTH)
MAX9686
MAX9698 (dual)

ECL OUTPUT

★ **MAX905** (master/slave, clocked)
MAX906 (dual, master/slave, clocked)
★ **MAX911** (programmable VTH)
★ **MAX9686** (dual, master/slave, clocked)
MAX9685
MAX9687 (dual)
MAX9690

★ New product since the publication of the 1990 Short Form Product Guide.

AMPLIFIERS

PRECISION

LOW VOS

BIPOLAR

- MAX400
- ★ MAX427
- ★ MAX437
- MAX480
- OP07
- OP27
- OP37
- OP90
- LT1001
- LT1028

CHOPPER

- MAX420
- MAX421
- MAX422
- MAX423
- MAX430 (internal caps)
- MAX432 (internal caps)
- ICL7650
- ICL7652

PROG. GAIN

- PGA100

LOW IB

- MAX406 (<1pA)
- ★ MAX407 (< 1pA, dual)
- ★ MAX409 (< 1pA)
- MAX420
- MAX421
- MAX422
- MAX423
- MAX430
- MAX432
- ICL761X
- ICL762X
- ICL763X
- ICL764X
- ICL7650
- ICL7652

LOW NOISE

- MAX400
- ★ MAX412 (dual MAX410)
- ★ MAX410 (<2.4nV/$\sqrt{Hz}$)
- ★ MAX414 (quad MAX410)
- ★ MAX427
- ★ MAX437
- OP07
- OP27
- OP37
- LT1001
- LT1028

HIGH SPEED

BANDWIDTH

- MAX402 (2-10MHz)
- MAX403 (2-10MHz)
- ★ MAX404 (80MHz)
- MAX408 (100MHz)
- ★ MAX410 (28MHz)
- ★ MAX412 (dual MAX410)
- ★ MAX414 (quad MAX410)
- MAX428 (dual, 100MHz)
- ★ MAX438 (6MHz, IQ = 75µA)
- ★ MAX439 (25MHz, IQ = 375µA)
- MAX448 (quad, 100MHz)
- MAX452 (50MHz)
- MAX457 (dual 70MHz)
- BB3554 (1700MHz GBW)
- OP37 (63MHz)
- LT1028 (75MHz)

SPECIAL

- MAX405 (high acc. buffer)
- ★ MAX440 (160MHz 8-ch mux/amp)
- ★ MAX441 (160MHz 4-ch mux/amp)
- ★ MAX442 (160MHz 2-ch mux/amp)
- MAX453 (50MHz mux/amp)
- MAX454 (50MHz mux/amp)
- MAX455 (50MHz mux/amp)
- MAX456 (video crosspoint switch)
- MAX460 (buffer)
- BB3553 (buffer)
- LH0033 (buffer)
- LH0063 (buffer)
- LH0101 (power amp)
- PGA100

LOW POWER

- MAX402
- MAX403
- MAX406 (1µA)
- ★ MAX409 (1µA)
- MAX422
- MAX423
- MAX432
- ★ MAX438 (6MHz, IQ = 75µA)
- ★ MAX439 (25MHz, IQ = 375µA)
- MAX480
- OP90
- ICL761X
- ICL762X
- ICL763X
- ICL764X

★ New product since the publication of the 1990 Short Form Product Guide.

19-4739; Rev 0; 2/92

MAXIM

1.2µA Max, Single/Dual, Single-Supply Op Amps

General Description

The MAX406/MAX407 are low-voltage, micropower, precision op amps designed for battery-operated systems. They feature a 1µA per amplifier quiescent current that is relatively constant over the entire supply range. This represents a significant improvement in supply current over industry-standard micropower op amps. A unique design technique allows the devices to operate at ultra-low quiescent current while maintaining linearity under loaded conditions. The output is capable of sourcing 2mA when powered by a 9V battery and drives smaller loads from a 3V battery.

The MAX406/MAX407 common-mode input voltage range extends from the negative rail to within 1.1V (1.2V MAX407) of the positive supply, and the output stage swings rail-to-rail. The MAX406/MAX407 maintain good DC characteristics, minimizing the input referred errors.

The MAX406 is a single op amp with two modes of operation: compensated mode and decompensated mode. Connecting BW (pin 8) to V-, or left floating, internally compensates the amplifier. In this mode, the MAX406 is unity-gain stable with a 5V/ms typical slew rate and an 8kHz gain bandwidth. Connecting BW to V+ puts the MAX406 into decompensated mode with a 20V/ms typical slew rate and a 40kHz gain bandwidth ($A_{VCL} \geq 2V/V$). The MAX407 is a dual, unity-gain stable op amp available in 8-pin DIP and SO packages.

Applications

Battery-Powered Systems

Medical Instruments

Electrometer Amplifiers

Intrinsically Safe Systems

Photodiode Pre-Amp

pH Meters

Features

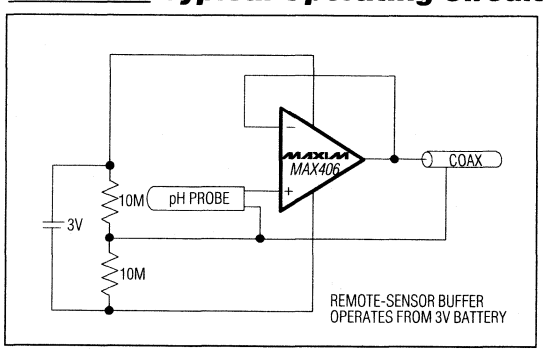
- ♦ **1.2µA Max Quiescent Current per Amplifier**
- ♦ **+2.5V to +10V Supply Range**
- ♦ **0.5mV Max Offset Voltage (MAX406A)**
- ♦ **< 0.1pA Typical Input Bias Current**
- ♦ **Output Swings Rail-to-Rail**
- ♦ **Input Voltage Range Includes Negative Rail**
- ♦ **Output Sources 2mA**
- ♦ **MAX407 Dual Available in 8-Pin DIP/SO**

Ordering Information

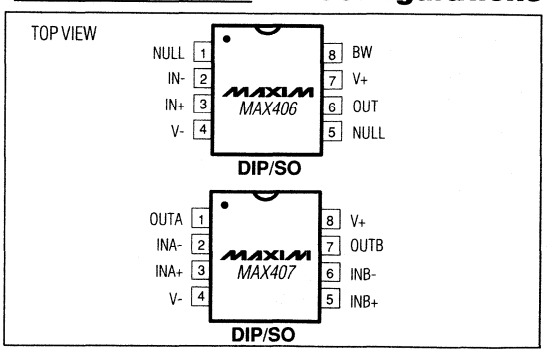
PART	TEMP. RANGE	PIN-PACKAGE
MAX406ACPA	0°C to +70°C	8 Plastic DIP
MAX406BCPA	0°C to +70°C	8 Plastic DIP
MAX406ACSA	0°C to +70°C	8 SO
MAX406BCSA	0°C to +70°C	8 SO
MAX406BC/D	0°C to +70°C	Dice*
MAX406AEPA	-40°C to +85°C	8 Plastic DIP
MAX406BEPA	-40°C to +85°C	8 Plastic DIP
MAX406AESA	-40°C to +85°C	8 SO
MAX406BESA	-40°C to +85°C	8 SO
MAX406AMJA	-55°C to +125°C	8 CERDIP**
MAX406BMJA	-55°C to +125°C	8 CERDIP**
MAX407CPA	0°C to +70°C	8 Plastic DIP
MAX407CSA	0°C to +70°C	8 SO
MAX407C/D	0°C to +70°C	Dice*
MAX407EPA	-40°C to +85°C	8 Plastic DIP
MAX407ESA	-40°C to +85°C	8 SO
MAX407MJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at +25°C, DC parameters only.*
*** Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configurations



1.2µA Max, Single/Dual, Single-Supply Op Amps

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V+ to V-) 12V
Input Voltage ..... (V+ + 0.3V) to (V- - 0.3V)
Continuous Current
Pins 2, 3 (MAX406);
Pins 2, 3, 5, 6 (MAX407) 10mA
Pins 1, 5, 6, 8 (MAX406);
Pins 1, 7 (MAX407) 50mA
Short-Circuit Duration ..... Indefinite
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 6.90mW/°C above +70°C) 552mW
SO(derate 5.88mW/°C above +70°C) 471mW
CERDIP(derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX40_C__ ..... 0°C to +70°C
MAX40_E__ ..... -40°C to +85°C
MAX40_M__ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Absolute Maximum Ratings apply to packaged parts.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX406A			0.25	0.5	mV
		MAX406B			0.75	2.0	
		MAX407			1.0	3.0	
Input Bias Current	I_B	V_{CM} = 0V (Note 2)			<0.1	10.0	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A	200	1000		V/mV
			MAX406B, MAX407	100	1000		
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = 5V, V- = -5V		10	23		
Gain Bandwidth	GBW	MAX406A/B	Compensated mode	4	8		kHz
			Decompensated mode	20	40		
		MAX407		4	8		
Input Common-Mode Range	CMR	MAX406A/B		V-		V + -1.1	V
		MAX407		V-		V + -1.2	
Output Voltage Swing	V_O	R_L = 1MΩ		±2.47	±2.49		V
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A	70	80		dB
			MAX406B	54	65		
			MAX407	60	65		
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = 2.5V to 7.5V	MAX406A		50	100	µV/V
			MAX406B		150	300	
			MAX407		200	600	
Slew Rate	SR	MAX406A/B	Compensated mode	3	5		V/ms
			Decompensated mode	12	20		
		MAX407		3	5		
Supply Current	I_{SY}	MAX406A/B			1.0	1.2	µA
		MAX407 (All amplifiers)			2.0	2.4	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 2.5V, V- = -2.5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Sink Current	I_{OSINK}	V_{OUT} = 0V	100	200		µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V	300	600		µA
Supply Voltage (V+ to V-)	V_S		2.5		10.0	V
Input Noise Voltage	e_n	f_O = 1kHz		150		$nV/\sqrt{Hz}$
		f_O = 0.1Hz to 10Hz		6		μV_{P-P}

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 4)	MAX406A			0.95	mV
			MAX406B			3.00	
			MAX407			4.00	
Offset-Voltage Tempco	TC_{VOS}	MAX406A			2	10	µV/°C
Input Bias Current	I_B	V_{CM} = 0V				20	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A	100			V/mV
			MAX406B	50			
			MAX407	50			
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = 5V, V- = -5V		10			
Output Voltage Swing	V_O	R_L = 1MΩ		±2.45			V
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A	66			dB
			MAX406B	50			
			MAX407	60			
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V- = 0V, V+ = 2.5V to 7.5V	MAX406A			150	µV/V
			MAX406B			450	
			MAX407			800	
Supply Current	I_{SY}	MAX406A/B				1.6	µA
		MAX407 (All amplifiers)				3.2	
Output Sink Current	I_{OSINK}	V_{OUT} = 0V		50			µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V		250			µA

1.2μA Max, Single/Dual, Single-Supply Op Amps

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 4)	MAX406A			1.10	mV
			MAX406B			3.00	
			MAX407			4.00	
Offset-Voltage Tempco	TC_{VOS}	MAX406A				10	μV/°C
Input Bias Current	I_B	V_{CM} = 0V				50	pA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A	50			V/mV
			MAX406B, MAX407	25			
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = 5V, V- = -5V		10			
Output Voltage Swing	V_O	R_L = 1MΩ		±2.45			V
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A	66			dB
			MAX406B	50			
			MAX407	60			
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = 2.5V to 7.5V	MAX406A			150	μV/V
			MAX406B			450	
			MAX407			800	
Supply Current	I_{SY}	MAX406A/B				1.7	μA
		MAX407 (All amplifiers)				3.4	
Output Sink Current	I_{OSINK}	V_{OUT} = 0V		40			μA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V		250			μA

ELECTRICAL CHARACTERISTICS

(V+ = 2.5V, V- = -2.5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 4)	MAX406A			1.5	mV
			MAX406B			4.0	
			MAX407			5.0	
Offset-Voltage Tempco	TC_{VOS}	MAX406A				10	μV/°C
Input Bias Current	I_B	V_{CM} = 0V				1.0	nA
Large-Signal Voltage Gain	A_{VOL}	R_L = 1MΩ, V_{OUT} = ±2V	MAX406A	20			V/mV
			MAX406B	10			
			MAX407	10			
		R_L = 1MΩ, V_{OUT} = ±4V, V+ = 5V, V- = -5V		10			
Output Voltage Swing	V_O	R_L = 1MΩ		±2.45			V

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 2.5V, V- = -2.5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio	CMRR	(Note 3)	MAX406A	66			dB
			MAX406B	50			
			MAX407	60			
Power-Supply Rejection Ratio	PSRR	V_{IN} = 0V, V+ = 2.5V to 7.5V	MAX406A			150	µV/V
			MAX406B			450	
			MAX407			800	
Supply Current	I_{SY}	MAX406A/B				2.0	µA
		MAX407 (All amplifiers)				4.0	
Output Sink Current	I_{OSINK}	V_{OUT} = 0V		20			µA
Output Source Current	$I_{OSOURCE}$	V_{OUT} = 0V		200			µA

Note 2: Production-automated test equipment cannot resolve input bias currents below 1pA. Lab equipment has shown the MAX406 and MAX407 typical input bias currents below 0.1pA.

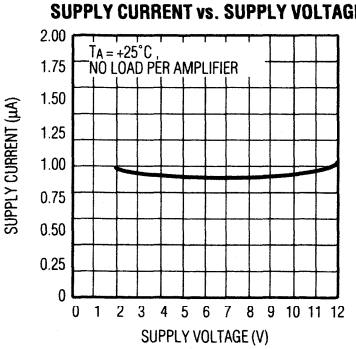
Note 3: MAX406: V_{CM} = V- to (V+ -1.1V). MAX407: V_{CM} = V- to (V+ -1.2V).

Note 4: MAX406A: Calculated from guaranteed drift specification and maximum offset voltage at room temperature. The 10µV/°C drift limit is 100% tested. MAX406B: Guaranteed 100% tested limit.

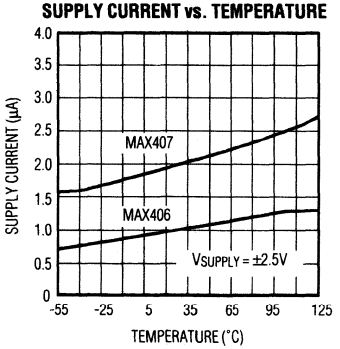
3

Typical Operating Characteristics

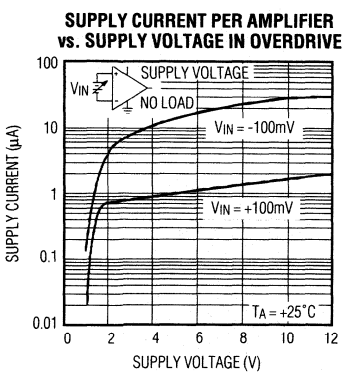
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



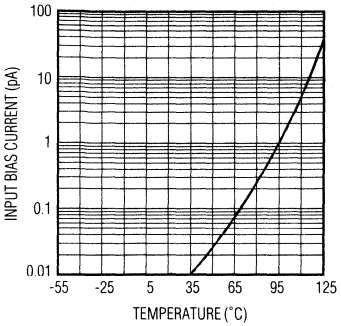
SUPPLY CURRENT PER AMPLIFIER vs. SUPPLY VOLTAGE IN OVERDRIVE



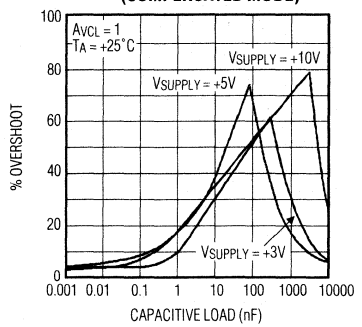
1.2μA Max, Single/Dual, Single-Supply Op Amps

Typical Operating Characteristics (continued)

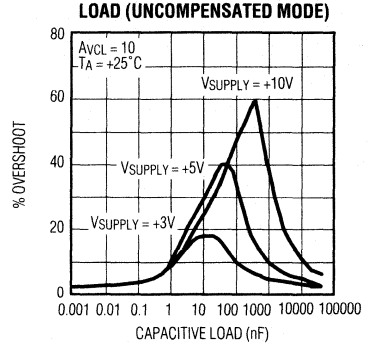
INPUT BIAS CURRENT vs. TEMPERATURE



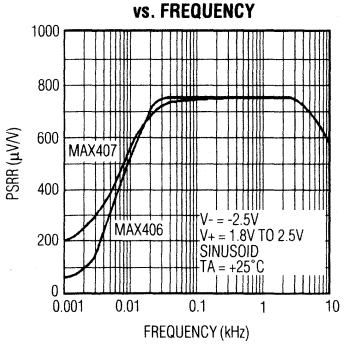
PERCENT OVERSHOOT vs. CAPACITIVE LOAD (COMPENSATED MODE)



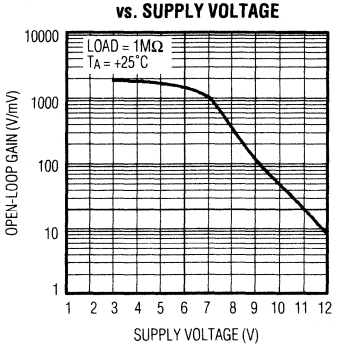
PERCENT OVERSHOOT vs. CAPACITIVE LOAD (UNCOMPENSATED MODE)



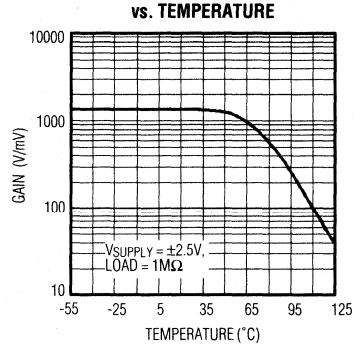
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



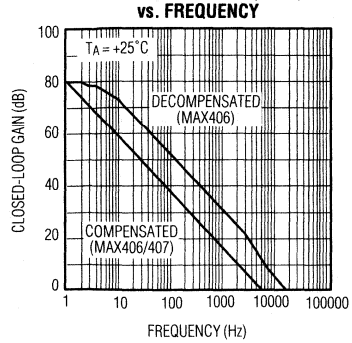
LARGE SIGNAL GAIN vs. SUPPLY VOLTAGE



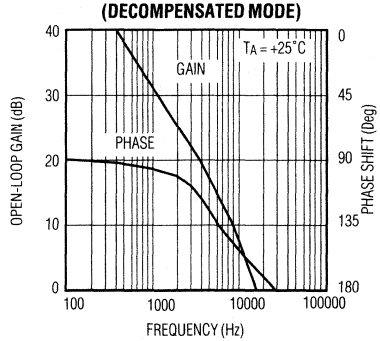
LARGE-SIGNAL GAIN vs. TEMPERATURE



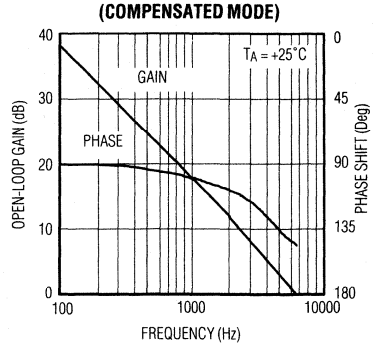
CLOSED-LOOP GAIN (80dB) vs. FREQUENCY



MAX406 OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (DECOMPENSATED MODE)

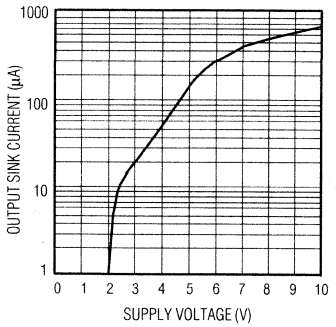


OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (COMPENSATED MODE)

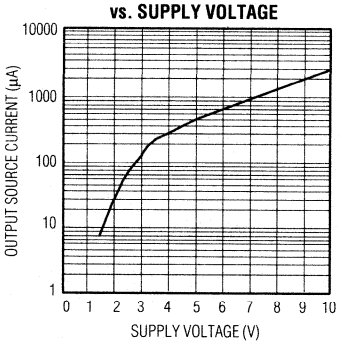


Typical Operating Characteristics (continued)

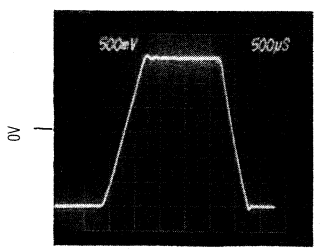
MAXIMUM OUTPUT SINK CURRENT vs. SUPPLY VOLTAGE



MAXIMUM OUTPUT SOURCE CURRENT vs. SUPPLY VOLTAGE

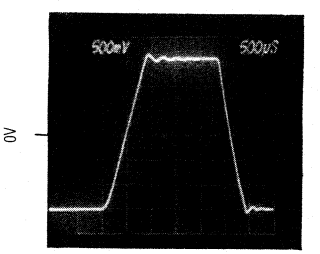


LARGE-SIGNAL TRANSIENT RESPONSE (COMPENSATED MODE)



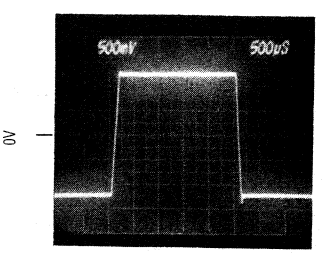
NONINVERTING, A_{VCL} = 1,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ//250pF

LARGE-SIGNAL TRANSIENT RESPONSE (COMPENSATED MODE)



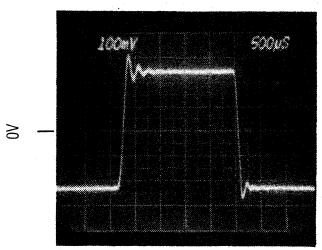
NONINVERTING, A_{VCL} = 1,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ//1000pF

MAX406 LARGE-SIGNAL TRANSIENT RESPONSE (DECOMPENSATED MODE)



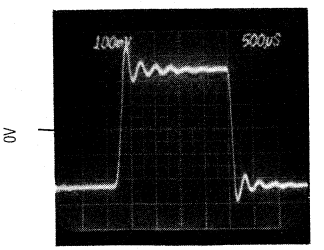
V_{SUPPLY} = ±2.5V, A_{VCL} = 2V/V, LOAD = 1MΩ//15pF

SMALL-SIGNAL TRANSIENT RESPONSE (COMPENSATED MODE)



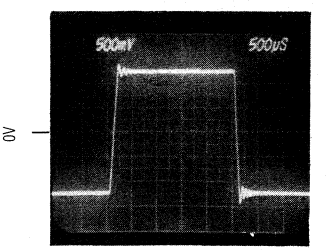
NONINVERTING, A_{VCL} = 1,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ//250pF

SMALL-SIGNAL TRANSIENT RESPONSE (COMPENSATED MODE)



NONINVERTING, A_{VCL} = 1,
V_{SUPPLY} = ±2.5V, LOAD = 1MΩ//1000pF

MAX406 LARGE-SIGNAL TRANSIENT RESPONSE (DECOMPENSATED MODE)



V_{SUPPLY} = ±2.5V, A_{VCL} = 2V/V, LOAD = 1MΩ//250pF

1.2µA Max, Single/Dual, Single-Supply Op Amps

Pin Description

MAX406 PIN	MAX407 PIN	NAME	FUNCTION
1		NULL	Nulling. Connect to one end of 100kΩ potentiometer for voltage-offset trimming (see Figure 1).
	1	OUTA	Amplifier A Output
2		IN-	Inverting Input
	2	INA-	Inverting Input to Amplifier A
3		IN+	Noninverting Input
	3	INA+	Noninverting Input to Amplifier A
4	4	V-	Negative Power-Supply Pin. Connect to (-) terminal of power supply or ground.
5		NULL	Nulling. Connect to other end of 100kΩ potentiometer for voltage-offset trimming (connect wiper to V+). See Figure 1.
	5	INB+	Noninverting Input to Amplifier B
6		OUT	Output
	6	INB-	Inverting Input to Amplifier B
	7	OUTB	Amplifier B Output
7	8	V+	Positive Supply Pin. Connect to (+) terminal of power supply.
8		BW	Bandwidth Selection Pin. Leave floating; connect to V- for unity-gain stability (compensated mode), connect to V+ for higher speed (decompensated mode).

Application Information

Trimming Voltage Offset

The MAX406's typical input offset voltage is between 0.25mV and 0.75mV, depending on the grade. If the application requires additional offset adjustment, connect a 100kΩ trim pot between pins 1, 5, and 7 for the MAX406 (Figure 1). The MAX407's offsets are not adjustable.

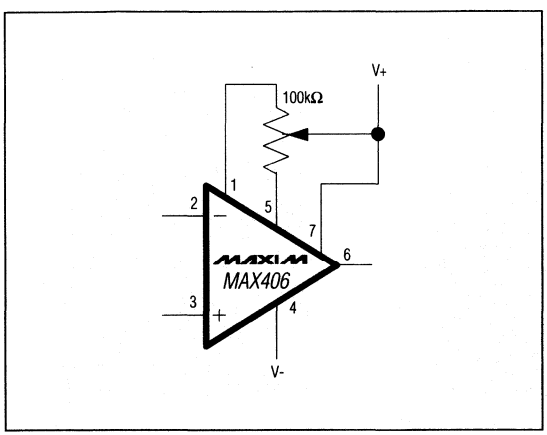


Figure 1. Offset-Voltage Adjustment

Input Overdrive vs. Supply Current

The MAX406/MAX407 supply current remains relatively constant over the supply range, providing the amplifier output is not overdriven to the negative supply rail. For example, when connecting the amplifier as a comparator and applying a -100mV input overdrive, supply current rises above 1µA per amplifier and varies with supply voltage (see *Supply Current vs. Supply Voltage in Overdrive, Typical Operating Characteristics*).

Total Supply-Voltage Considerations

Although the MAX406/MAX407 operate with supply voltages between 2.5V and 10V, best performance is achieved with supply voltages below 7V. The *Open-Loop Gain vs. Supply Voltage* graph in the *Typical Operating Characteristics* section shows how open-loop gain is reduced at voltages that exceed 7V.

Stability

Unlike other industry-standard micropower CMOS op amps, the MAX406/MAX407 maintain stability while driving heavy capacitive loads as demonstrated in the graph of *Percent Overshoot vs. Capacitive Load*, in the *Typical Operating Characterstics* section.

Bandwidth

The MAX407 is internally compensated for unity-gain stable operation, with an 8kHz typical gain bandwidth. The MAX406 operates in one of two modes. Floating the

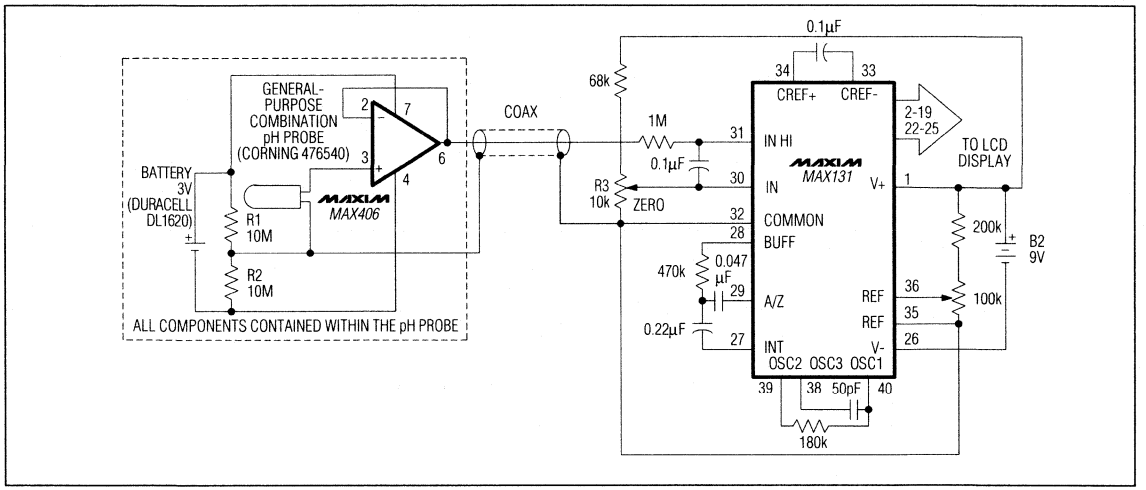


Figure 2. Buffered pH Probe Allows Low-Cost Cable

BW pin, or connecting it to V-, internally compensates the amplifier for unity-gain stable operation. Connecting the BW pin to V+ reduces the compensation and allows the amplifier to be used at higher speeds. When operating in high-speed mode, the MAX406 is stable for closed-loop gains ≥ 2V/V, with a 40kHz typical gain bandwidth and a 20V/ms typical slew rate.

Typical Application Circuits

Buffered pH Probe Allows Low-Cost Cable

The MAX406 has less than 20pA input leakage current over commercial temperature, and is typically less than 100fA at +25°C. These characteristics are ideal for buffering pH probes and a variety of other high output-impedance chemical sensors. The circuit in Figure 2 eliminates expensive low-leakage cables that often connect pH probes to meters. A MAX406 and a lithium battery are included in the probe housing. A conventional low-cost coaxial cable carries the buffered pH signal to the MAX131 A/D converter. In most cases, the probe assembly's battery life exceeds the functional life of the probe itself.

Mircopower, 4-Channel Simultaneous Sample-and-Hold

Switch leakage and buffer input bias current in sample and hold circuits limit performance by discharging the signal voltage on the hold capacitor, an effect called "droop." The 2pA typical room temperature leakage current for the MAX327 and 100fA typical input bias current for the MAX407 translates to a typical droop rate of 50µV/s for the circuit in Figure 3. Another advantage is low power consumption. The MAX327 guarantees no more than 250µA supply current with ±15V supplies, but most of this is drawn by internal logic-level translators. By using rail-to-rail logic (CD4000, 74C00, or 74HC00 families) to drive IN1-IN3, the level translators are turned off and the supply current falls well below 1µA when the switches are off. This technique turns any Maxim switch or multiplexer into an ultra-low power device. The circuit in Figure 3 typically draws 6µA with 0V to 8V logic input levels.

Remotely Powered Sensor Amp

Figure 4 shows a simple 2-wire current transmitter that uses no power at the transmitting end except from the transmitted signal itself. At the transmitter, a 0V to 1V input drives both a MAX406 and an NPN transistor connected as a voltage-controlled current sink. The 0mA to 2mA output is sent through a twisted pair to the receiver and develops a voltage across the receiver sense resistor R2. The resulting sense voltage is buffered by another MAX406, producing a 0V to 1V ground-referenced output signal. R1 and R2 should be well matched. The MAX406's supply current is added to the 0mA to 2mA signal, resulting in a 500µV offset at the output. This offset, in addition to the MAX406's input offset, varies with temperature.

1.2µA Max, Single/Dual, Single-Supply Op Amps

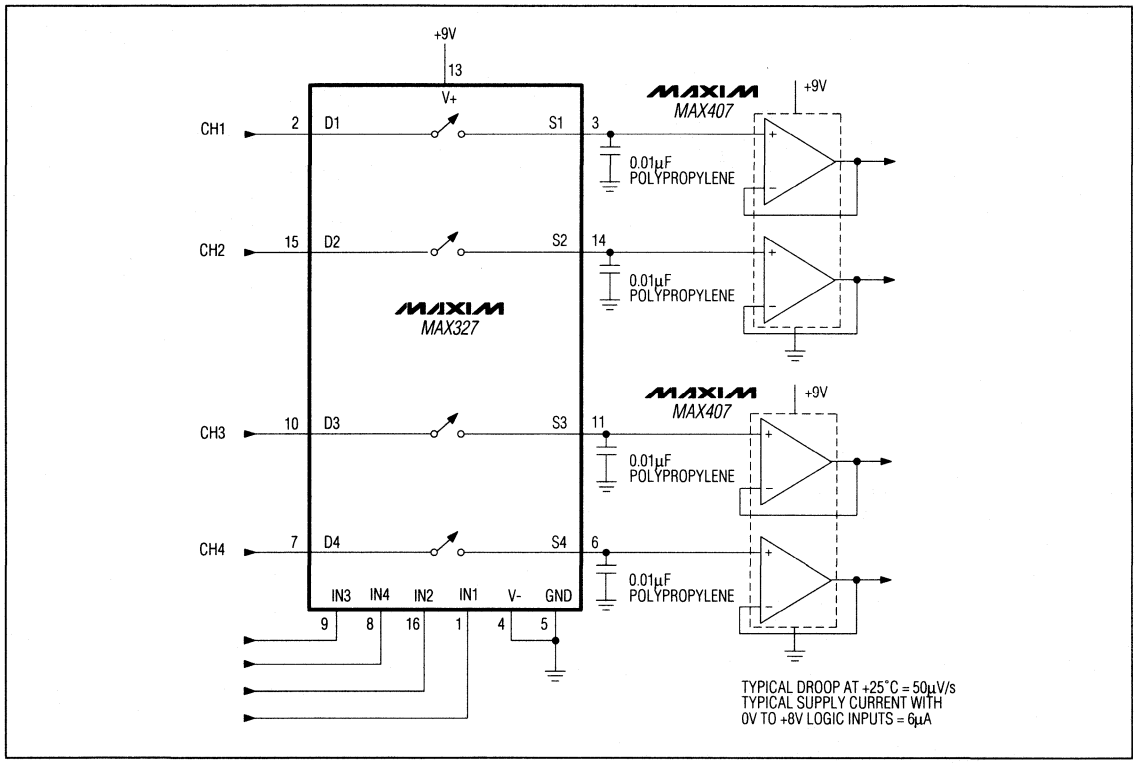


Figure 3. Micropower, 4-Channel, Simultaneous Sample-and-Hold

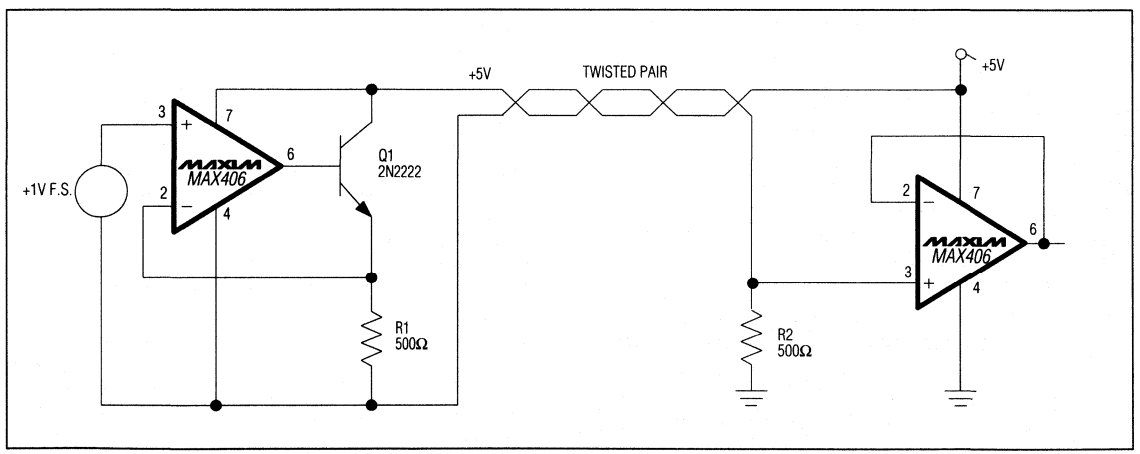
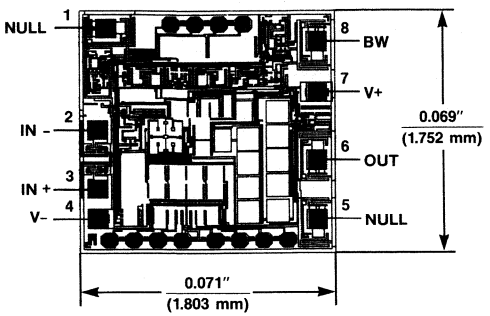


Figure 4. Remotely Powered Sensor Amp

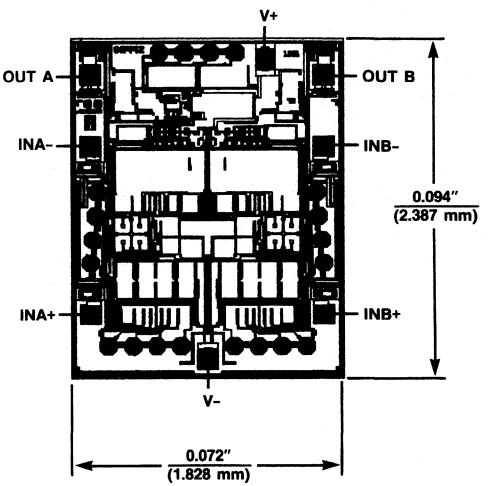
Chip Topography

MAX406



TRANSISTOR COUNT: 148
NOTE: SUBSTRATE IS CONNECTED TO V+

MAX407



TRANSISTOR COUNT: 129
NOTE: SUBSTRATE IS CONNECTED TO V+

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

Single/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

General Description

The MAX410/MAX414 single/quad op amps set a new standard for noise performance in high-speed, low-voltage systems. Input voltage-noise density is 100% tested and is guaranteed to be less than 2.4nV/√Hz at 1kHz. A unique design not only combines low noise with +5V operation, but also consumes less than 2.5mA supply current per amplifier. Low-voltage operation is guaranteed with an output voltage swing of +3.6V into 2kΩ. The MAX410/MAX414 also operate from supply voltages between +2.4V and +5V for greater supply flexibility.

Unity-gain stability, 28MHz bandwidth, and 4.5V/µs slew rate ensure low-noise performance in a wide variety of wideband and measurement applications. The MAX410/MAX414 are available in DIP and SO packages in the industry-standard single/quad op-amp pin configurations.

Applications

Low-Noise Frequency Synthesizers

Infrared Detectors

High-Quality Audio Amplifiers

Ultra Low-Noise Instrumentation Amplifiers

Bridge-Signal Conditioning

Features

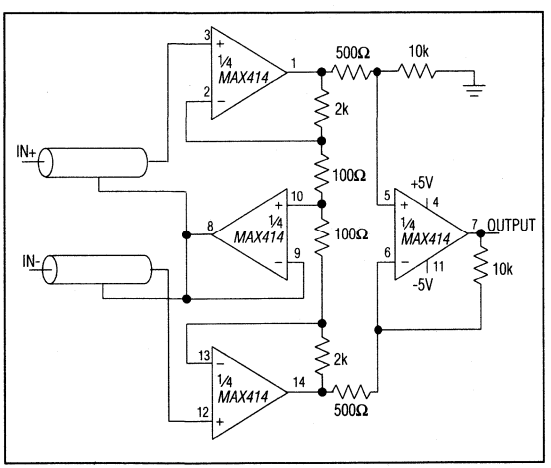
- ♦ **100% Tested Voltage Noise: 2.4nV/√Hz Max at 1kHz**
- ♦ **2.5mA Supply Current Per Amplifier**
- ♦ **Low Supply Voltage Operation: ±2.4V to ±5V**
- ♦ **28 MHz Unity-Gain Bandwidth**
- ♦ **4.5V/µs Slew Rate**
- ♦ **250µV Max Offset Voltage (MAX410)**
- ♦ **115dB Min Voltage Gain**

Ordering Information

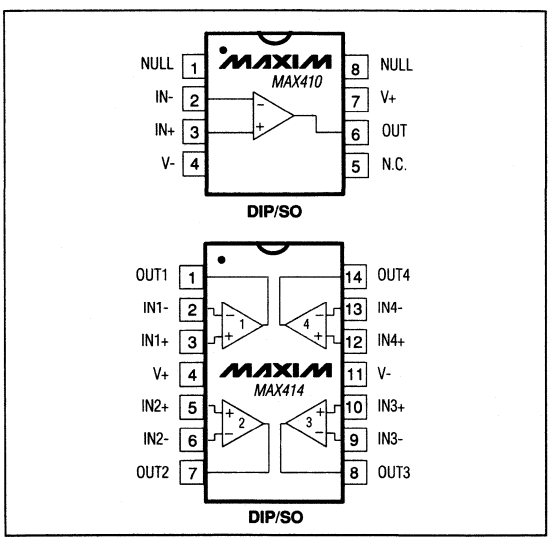
PART	TEMP. RANGE	PIN-PACKAGE
MAX410CPA	0°C to +70°C	8 Plastic DIP
MAX410CSA	0°C to +70°C	8 SO
MAX410C/D	0°C to +70°C	Dice*
MAX410EPA	-40°C to +85°C	8 Plastic DIP
MAX410ESA	-40°C to +85°C	8 SO
MAX410MJA	-55°C to +125°C	8 CERDIP
MAX414CPD	0°C to +70°C	14 Plastic DIP
MAX414CSD	0°C to +70°C	14 SO
MAX414EPD	-40°C to +85°C	14 Plastic DIP
MAX414ESD	-40°C to +85°C	14 SO
MAX414MJD	-55°C to +125°C	14 CERDIP

** Dice are specified at T_A = +25°C, DC parameters only.*

Typical Operating Circuit



Pin Configurations



Single/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-) 12V
Differential Input Current (Note 1) ..... ±20mA
Differential Input Voltage ..... V+ to V-
Common-Mode Input Voltage ..... (V+ + 0.3V) to (V- - 0.3V)
Short-Circuit Current Duration ..... Indefinite
Continuous Power Dissipation (T_A = +70°C)
MAX410
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW
MAX414
14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) . 800mW
14-Pin SO (derate 8.00mW/°C above +70°C) 640mW
14-Pin CERDIP (derate 9.09mW/°C above +70°C) ... 727mW
Operating Temperature Ranges:
MAX41_C _ _ ..... 0°C to +70°C
MAX41_E _ _ ..... -40°C to +85°C
MAX41_MJ_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The amplifier inputs are connected by internal back-to-back clamp diodes. In order to minimize noise in the input stage, current-limiting resistors are not used. If differential input voltages exceeding ±1.0V are applied, limit input current to 20mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX410		±120	±250	µV
		MAX414		±150	±320	
Input Bias Current	I_B			±80	±150	nA
Input Offset Current	I_{OS}			±40	±80	nA
Differential Input Resistance	R_{IN}(Diff)			20		kΩ
Common-Mode Input Resistance	R_{IN}(CM)			150		MΩ
Input Capacitance	C_{IN}			4		pF
Input Noise-Voltage Density	e_n	f_O = 10Hz		7		nV/√Hz
		f_O = 1000Hz (100% tested)		1.8	2.4	
Input Noise-Current Density	i_n	f_O = 10Hz		2.6		pA/√Hz
		f_O = 1000Hz		1.2		
Common-Mode Input Voltage	V_{CM}		+3.5 -3.5	+3.7 -3.8		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	115	130		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	96	103		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = 3.6V to -3.7V	115	122		dB
		R_L = 600Ω, V_O = ±3.5V	110	120		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	+3.6 -3.7	+3.7 -3.8		V
Short-Circuit Output Current	I_{SC}			35		mA
Slew Rate	SR	10kΩ/20pF load		4.5		V/µs
Unity-Gain Bandwidth	GBW	10kΩ/20pF load		28		MHz
Settling Time	t_S	To 0.1%		1.3		µs
Channel Separation	CS	f_O = 1kHz		135		dB
Operating Supply Voltage Range	V_S		±2.4		±5.25	V
Supply Current per Amplifier	I_S			2.5	2.7	mA

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX410		±150	±350	µV
		MAX414		±190	±450	
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±100	±200	nA
Input Offset Current	I_{OS}			±80	±150	nA
Common-Mode Input Voltage	V_{CM}		+3.5 -3.5	+3.7 -3.8		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	121		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	97		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = ±3.6V	110	120		dB
		R_L = 600Ω, V_O = ±3.5V	90	119		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	±3.6	±3.7		V
Supply Current per Amplifier	I_S				3.2	mA

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX410		±200	±400	µV
		MAX414		±260	±520	
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±130	±350	nA
Input Offset Current	I_{OS}			±100	±200	nA
Common-Mode Input Voltage	V_{CM}		+3.5 -3.5	+3.7 -3.6		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	120		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	94		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = 3.6V to -3.5V	110	118		dB
		R_L = 600Ω, V_O = ±3.5V	90	114		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	+3.6 -3.5	+3.7 -3.6		V
Supply Current per Amplifier	I_S				3.2	mA

Single/Quad, 28MHz, Low-Noise, Low-Voltage, Precision Op Amps

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	MAX410		±200	±400	µV
		MAX414		±260	±520	
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±130	±350	nA
Input Offset Current	I_{OS}			±100	±200	nA
Common-Mode Input Voltage	V_{CM}		+3.5 -3.5	+3.7 -3.6		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	120		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	94		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = 3.6V to -3.5V	110	118		dB
		R_L = 600Ω, V_O = ±3.5V	90	114		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	+3.6 -3.5	+3.7 -3.6		V
Supply Current per Amplifier	I_S				3.5	mA

19-4194; Rev. 0; 8/91

MAXIM

Dual, Low-Noise Low-Voltage Precision Op Amp

General Description

The MAX412 dual operational amplifier sets a new standard for noise performance in low-voltage systems. Input voltage noise density is 100% tested and is guaranteed to be less than 2.4nV/√Hz at 1kHz. A unique design not only combines low noise with ±5V operation, but also consumes less than 2.5mA supply current per amplifier. Low voltage operation is assured with a guaranteed output voltage swing of ±3.6V into 2kΩ. The MAX412 also operates from supply voltages between ±2.4V and ±5V for greater supply flexibility.

Unity-gain stability, 28MHz bandwidth, and 4.5V/μs slew rate ensure low noise performance in a variety of wideband and measurement applications. The MAX412 is available in 8-pin DIP and SO packages in the industry-standard dual op amp pin configuration.

Applications

Low Noise-Frequency Synthesizers
Infrared Detectors
High-Quality Audio Amplifiers
Accelerometer and Gyro Amplifiers
Magnetic Search Coil Amplifiers
Ultra-Low Noise Instrumentation Amplifiers
Bridge Signal Conditioning

Features

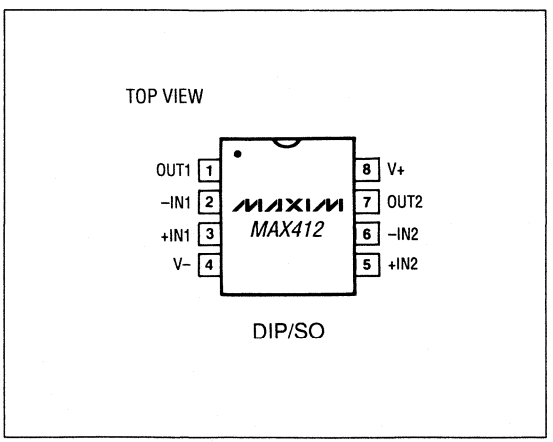
- **100% Tested Voltage Noise: 2.4nV/√Hz Max at 1kHz**
- **2.5mA Supply Current Per Amplifier**
- **Low Supply Voltage Operation: ±2.4V to ±5V**
- **28MHz Unity-Gain Bandwidth**
- **4.5V/μs Slew Rate**
- **250μV Max Offset Voltage**
- **115dB Min Voltage Gain**
- **2 Amplifiers in One 8-Pin DIP/SO**

Ordering Information

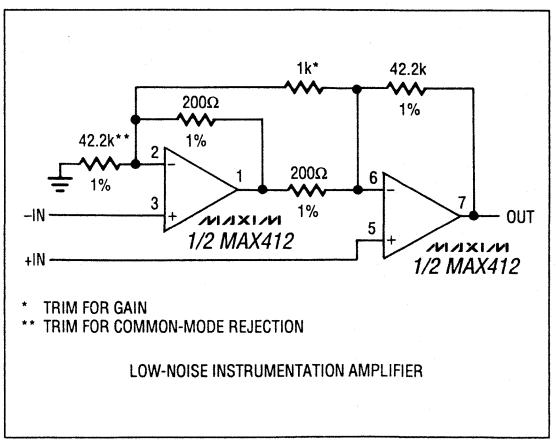
PART	TEMP. RANGE	PIN-PACKAGE
MAX412CPA	0°C to +70°C	8 Plastic DIP
MAX412CSA	0°C to +70°C	8 SO
MAX412C/D	0°C to +70°C	Dice*
MAX412EPA	-40°C to +85°C	8 Plastic DIP
MAX412ESA	-40°C to +85°C	8 SO
MAX412MJA	-55°C to +125°C	8 CERDIP

** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configuration



Typical Operating Circuit



Dual, Low-Noise, Low-Voltage Precision Op Amp

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V–) 12V
Differential Input Current (Note 1) ..... ±20mA
Differential Input Voltage ..... V+ to V–
Common-Mode Input Voltage ..... (V+ +0.3V) to (V– –0.3V)
Short-Circuit Current Duration ..... Indefinite
Continuous Power Dissipation (T_A = +70°C)
8-pin Plastic DIP (derate 6.9mW/°C above +70°C) .. 552mW
8-pin SO (derate 5.88mW/°C above +70°C) 471mW
8-pin CERDIP (derate 8.0mW/°C above +70°C) ... 640mW

Operating Temperature Ranges:
MAX412C_A ..... 0°C to +70°C
MAX412E_A ..... -40°C to +85°C
MAX412MJA ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The amplifier inputs are connected by internal back-to-back clamp diodes. In order to minimize noise in the input stage, current-limiting resistors are not used. If differential input voltages exceeding ±1.0V are applied, input current should be limited to 20mA.

Stresses beyond those under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V– = –5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}			±120	±250	µV
Input Bias Current	I_B			±80	±150	nA
Input Offset Current	I_{OS}			±40	±80	nA
Differential Input Resistance	R_{IN}(Diff)			20		kΩ
Common-Mode Input Resistance	R_{IN}(CM)			40		MΩ
Input Capacitance	C_{IN}			4		pF
Input Noise-Voltage Density	e_n	f_o = 10Hz		7		nV/√Hz
		f_o = 1000Hz (100% tested)		1.8	2.4	
Input Noise-Current Density	i_n	f_o = 10Hz		2.6		pA/√Hz
		f_o = 1000Hz		1.2		
Common-Mode Input Voltage	V_{CM}		+3.5 –3.5	+3.7 –3.8		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	115	130		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	96	103		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = 3.6V to -3.7V	115	122		dB
		R_L = 600Ω, V_O = ±3.5V	110	120		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	+3.6 –3.7	+3.7 –3.8		V
Short-Circuit Output Current	I_{SC}			35		mA
Slew Rate	SR	10kΩ/20pF load		4.5		V/µs
Unity-Gain Bandwidth	GBW	10kΩ/20pF load		28		MHz
Settling Time	t_S	To 0.1%		1.3		µs
Channel Separation	CS	f_o = 1kHz		135		dB
Operating-Supply Voltage Range	V_S		±2.4		±5.25	V
Supply Current	I_S	Both amplifiers		5	5.25	mA

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V– = –5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}			±150	±350	µV
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±100	±200	nA
Input Offset Current	I_{OS}			±80	±150	nA
Common-Mode Input Voltage	V_{CM}		+3.5 –3.5	+3.7 –3.8		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	121		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	97		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = ±3.6V	110	120		dB
		R_L = 600Ω, V_O = ±3.5V	90	119		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	±3.6	±3.7		V
Supply Current	I_S	Both amplifiers			6.5	mA

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V– = –5V, T_A = –40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}			±200	±400	µV
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±130	±350	nA
Input Offset Current	I_{OS}			±100	±200	nA
Common-Mode Input Voltage	V_{CM}		+3.5 –3.5	+3.7 –3.6		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	120		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	94		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = +3.6V to –3.5V	110	118		dB
		R_L = 600Ω, V_O = ±3.5V	90	114		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	+3.6 –3.5	+3.7 –3.6		V
Supply Current	I_S	Both amplifiers			6.5	mA

Dual, Low-Noise, Low-Voltage Precision Op Amp

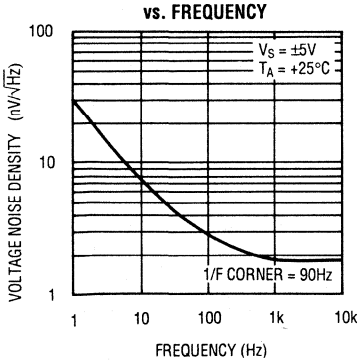
ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = -55°C to +125°C, unless otherwise noted.)

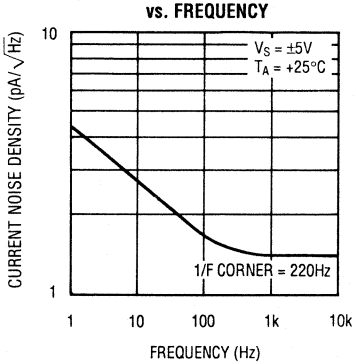
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}			±200	±400	µV
Offset-Voltage Tempco	$\Delta V_{OS}/\Delta T$	Over operating temperature range		±1		µV/°C
Input Bias Current	I_B			±130	±350	nA
Input Offset Current	I_{OS}			±100	±200	nA
Common-Mode Input Voltage	V_{CM}		+3.5 -3.5	+3.7 -3.6		V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	105	120		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±2.4V to ±5.25V	90	94		dB
Large-Signal Gain	A_{VOL}	R_L = 2kΩ, V_O = +3.6V to -3.5V	110	118		dB
		R_L = 600Ω, V_O = ±3.5V	90	114		
Output Voltage Swing	V_{OUT}	R_L = 2kΩ	+3.6 -3.5	+3.7 -3.6		V
Supply Current	I_S	Both amplifiers			7	mA

Typical Operating Characteristics

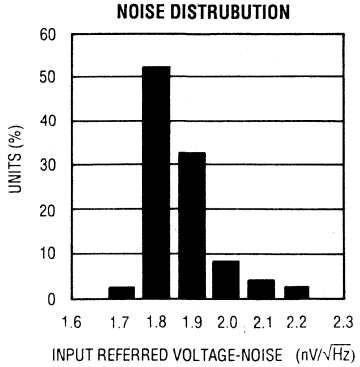
VOLTAGE NOISE DENSITY vs. FREQUENCY



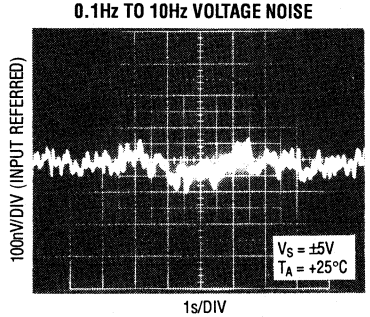
CURRENT NOISE DENSITY vs. FREQUENCY



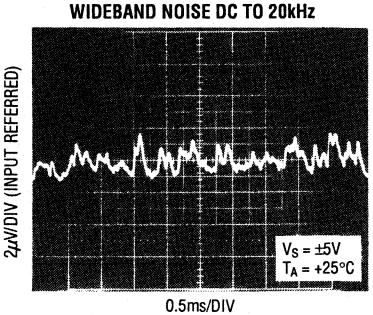
1kHz VOLTAGE NOISE DISTRUBUTION



0.1Hz TO 10Hz VOLTAGE NOISE



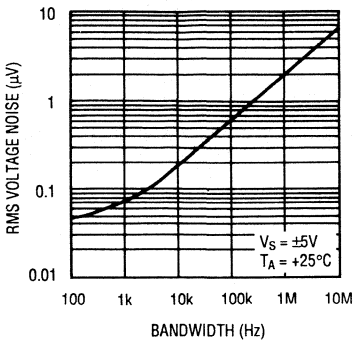
WIDEBAND NOISE DC TO 20kHz



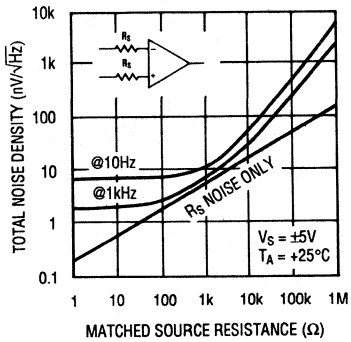
Dual, Low-Noise, Low-Voltage Precision Op Amp

Typical Operating Characteristics (continued)

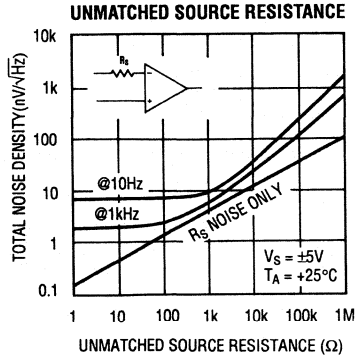
WIDEBAND VOLTAGE NOISE
(0.1Hz TO FREQUENCY INDICATED)



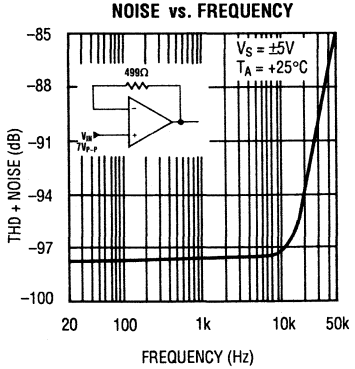
TOTAL NOISE DENSITY
vs. MATCHED SOURCE RESISTANCE



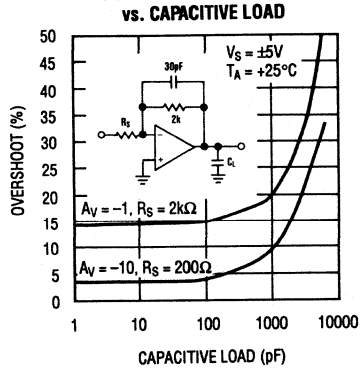
TOTAL NOISE DENSITY vs.
UNMATCHED SOURCE RESISTANCE



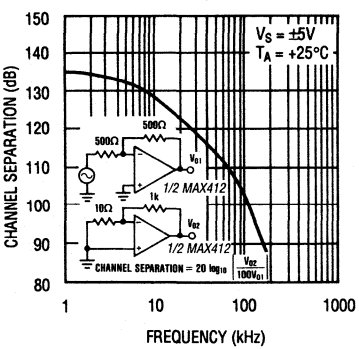
TOTAL HARMONIC DISTORTION +
NOISE vs. FREQUENCY



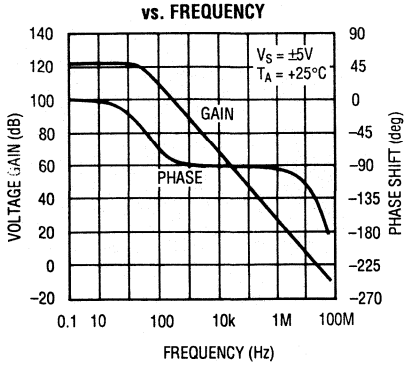
PERCENTAGE OVERSHOOT
vs. CAPACITIVE LOAD



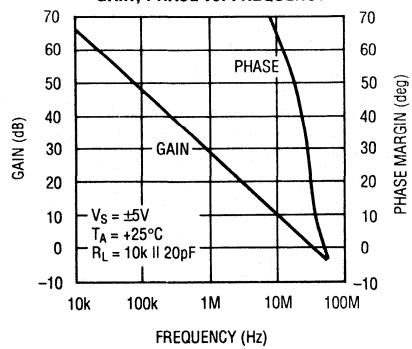
CHANNEL SEPARATION
vs. FREQUENCY



VOLTAGE GAIN, PHASE SHIFT
vs. FREQUENCY



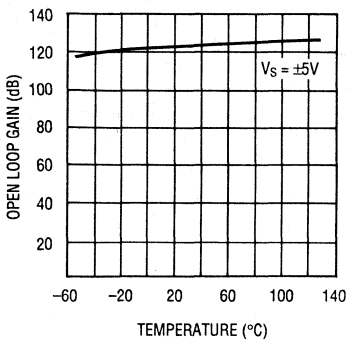
GAIN, PHASE vs. FREQUENCY



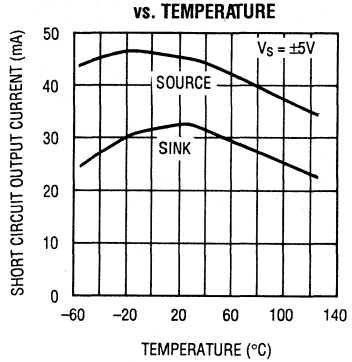
Dual, Low-Noise, Low-Voltage Precision Op Amp

Typical Operating Characteristics (continued)

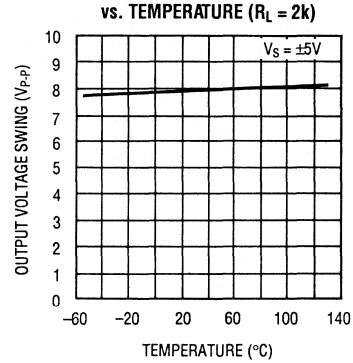
OPEN LOOP GAIN vs. TEMPERATURE



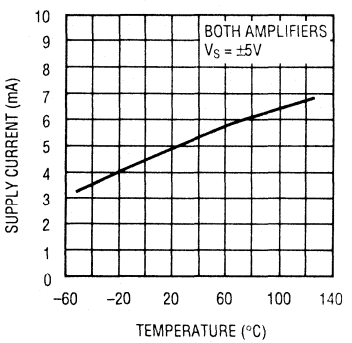
SHORT CIRCUIT OUTPUT CURRENT vs. TEMPERATURE



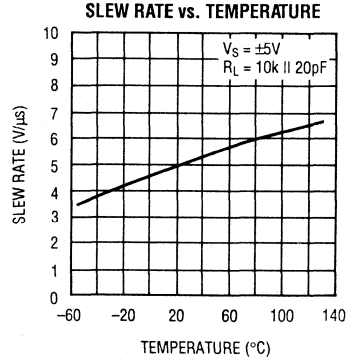
OUTPUT VOLTAGE SWING vs. TEMPERATURE (R_L = 2k)



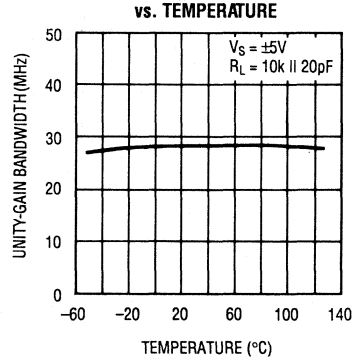
SUPPLY CURRENT vs. TEMPERATURE



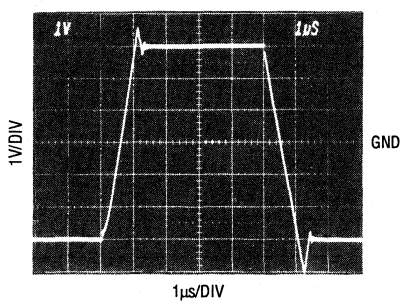
SLEW RATE vs. TEMPERATURE



UNITY-GAIN BANDWIDTH vs. TEMPERATURE

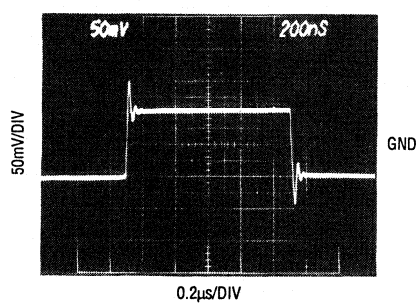


LARGE-SIGNAL TRANSIENT RESPONSE



A_V = +1, R_F = 499Ω, R_L = 2k II 20pF
V_S = ±5V, T_A = +25°C

SMALL-SIGNAL TRANSIENT RESPONSE



A_V = +1, R_F = 200Ω, R_L = 2k II 20pF
V_S = ±5V, T_A = +25°C

Dual, Low-Noise, Low-Voltage Precision Op Amp

Pin Description

PIN	NAME	FUNCTION
1	OUT1	Amplifier Signal Output 1.
2	IN1-	Inverting Input 1.
3	IN1+	Non-Inverting Input 1.
4	V-	Negative Power Supply (V_{EE}).
5	IN2+	Non-Inverting Input 2.
6	IN2-	Inverting Input 2.
7	OUT2	Amplifier Signal Output 2.
8	V+	Positive Power Supply (V_{CC}).

Applications Information

The MAX412 is designed to provide low voltage noise performance. Obtaining low voltage noise from a bipolar op amp requires high collector currents in the input stage, since voltage noise is inversely proportional to the square root of the input stage collector current. However, op amp current noise is proportional to the square root of the input stage collector current, and input bias current is proportional to input stage collector current. Therefore, to obtain optimum low noise performance, DC accuracy, and AC stability, the value of the feedback and source resistance used with the MAX412 should be minimized.

Total Noise Density vs. Source Resistance

The industry standard expression for the total input referred noise of a real op amp at a given frequency is:

$$e_t = \sqrt{e_n^2 + (R_p + R_n)^2 i_n^2 + 4kT (R_p + R_n)}$$

Where:

R_n = Inverting input effective series resistance
R_p = Non-inverting input effective series resistance
e_n = Input voltage noise density at the frequency of interest
i_n = Input current noise density at the frequency of interest
T = Ambient temperature in Kelvin (K)
k = 1.38×10^{-23} j/K (Boltzman's constant).

In Figure 1, R_p = R3 and R_n = R1 || R2. In a real application, the output resistance of the source driving the input must be included with R_p and R_n. The following example demonstrates how to calculate the total output noise density at a frequency of 1kHz for the MAX412 circuit in Figure 1.

Gain = 1000
4kT at +25°C = $1.68 \times 10^{-20} V^2/\Omega Hz$
R_p = 100Ω
R_n = 100Ω || 100k = 99.9Ω
e_n = 1.8nV/√Hz
i_n = 1.2pA/√Hz

$$e_t = \sqrt{(1.8 \times 10^{-9})^2 + (100 + 99.9)^2 (1.2 \times 10^{-12})^2}$$
$$\sqrt{+ (1.68 \times 10^{-20}) (100 + 99.9)} = 2.58nV/\sqrt{Hz} \text{ at } 1kHz$$

Output noise density = $(1000)e_t = 2.58\mu V/\sqrt{Hz}$ at 1kHz.

In general, the amplifier's voltage noise dominates with equivalent source resistances less than 200Ω. As the equivalent source resistance increases, resistor noise becomes the dominant term, eventually making the voltage noise contribution from the MAX412 negligible. As the source resistance is further increased, current noise becomes dominant. For example, when the equivalent source resistance is greater than 3kΩ at 1kHz, the current noise component is larger than the resistor noise. The graph of *Total Noise Density vs. Matched Source Resistance* shows this phenomenon. Optimal MAX412 noise performance and minimum total noise is achieved with an equivalent source resistance of less than 10kΩ.

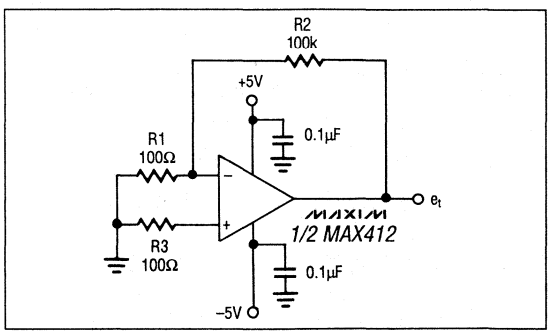


Figure 1. Total Noise vs. Source Resistance Example

Voltage Noise Testing

The RMS voltage noise density of the MAX412 is measured with the circuit shown in Figure 2, using the QuanTech Model 5173 noise analyzer, or equivalent. The voltage noise density at 1kHz is 100% tested on all production units. When measuring op amp voltage noise, only metal film resistors should be used in the test fixture, and resistor values should be minimized.

Dual, Low-Noise, Low-Voltage Precision Op Amp

The 0.1Hz to 10Hz peak-to-peak noise of the MAX412 is measured using the test circuit shown in Figure 3. The frequency response of this circuit is shown in Figure 4. The test time for the 0.1Hz to 10Hz noise measurement should be limited to 10 seconds, which has the effect of adding a second zero to the test circuit, providing increased attenuation for frequencies below 0.1Hz.

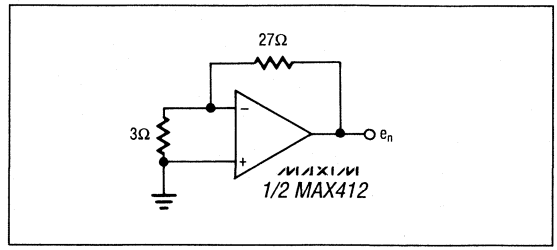


Figure 2. Voltage-Noise Density Test Circuit

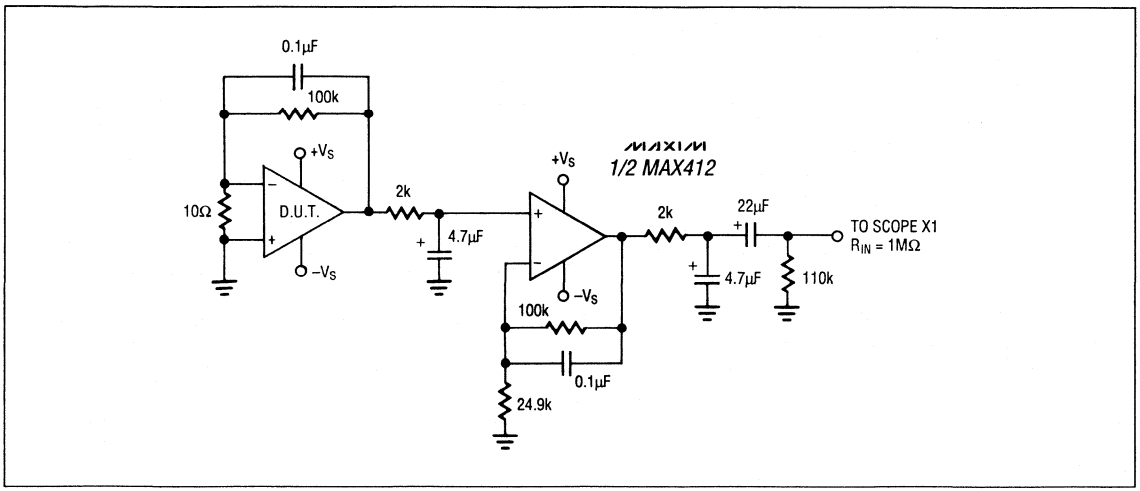


Figure 3. 0.1Hz to 10Hz Voltage-Noise Test Circuit

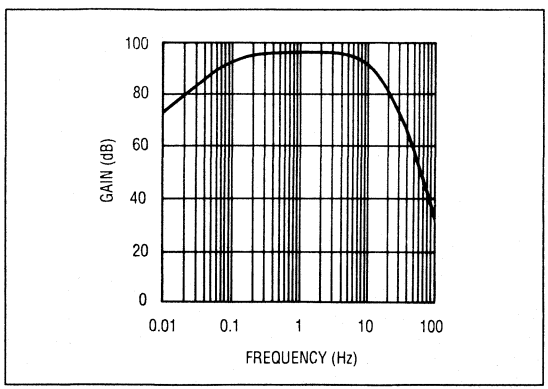


Figure 4. 0.1Hz to 10Hz Voltage-Noise Test Circuit, Frequency Response

Current Noise Testing

The current noise density of the MAX412 is measured with the QuanTech Model 5173 or equivalent using the test circuit shown in Figure 5. After the value of the input referred noise for the test circuit is measured, the current noise density can be calculated using the industry standard expression given below:

$$i_n = \frac{\sqrt{e_{no}^2 - [(A_{VCL})(4kT)(R_n + R_p)]^2}}{(R_n + R_p)(A_{VCL})}$$

R_n = Inverting input effective series resistance
R_p = Non-inverting input effective series resistance
e_{no} = Output voltage noise density at the frequency of interest
i_n = Input current noise density at the frequency of interest
A_{VCL} = Closed-loop gain
T = Ambient temperature in Kelvin (K)
k = 1.38×10^{-23} j/K (Boltzman's constant).

R_P and R_n must include the resistances of the input driving source(s), if any. If the QuanTech Model 5173 is used to measure the voltage noise, then the A_{VCL} terms in the numerator and denominator of the equation given above should be eliminated, since the QuanTech measures input referred noise. For the circuit in Figure 5, assuming R_P is approximately equal to R_n and the measurement is taken with the QuanTech Model 5173, the equation simplifies to:

$$i_n = \frac{\sqrt{e_{no}^2 - [(16.6 \times 10^{-21})(20 \times 10^3)]^2}}{(20 \times 10^{-3})}$$

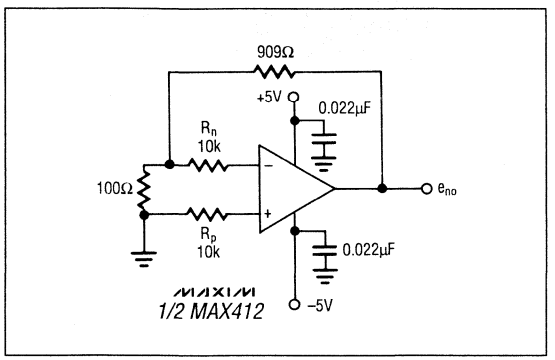


Figure 5. Current-Noise Test Circuit

Input Protection

To protect amplifier inputs from excessive differential input voltages, most modern op amps contain input protection diodes and current limiting resistors. These resistors increase the input referred noise of the amplifier. To optimize noise performance, they have not been included in the MAX412. The MAX412 does contain back-to-back input protection diodes, which will protect the amplifier for differential input voltages of ±1.0V. If the amplifier must be protected from higher differential input voltages, external current limiting resistors should be added in series with the op amp inputs to limit the potential input current to no more than 20mA.

Capacitive Load Driving

Driving large capacitive loads will increase the likelihood of oscillation in amplifier circuits. This is especially true for circuits with high loop gains, like voltage followers. The output impedance of the amplifier and a capacitive load will form an RC network that adds a pole to the loop response. If the pole frequency is low enough, as when driving a large capacitive load, the circuit phase margin is degraded.

In voltage follower circuits, the MAX412 will remain stable while driving capacitive loads as great as 100pF. Figure 6 is a photograph of the MAX412 driving a 100pF load in a closed loop gain configuration of +1V/V, with R_F = 499Ω.

When driving capacitive loads of greater than 100pF, an output isolation resistor should be added to the voltage follower circuit, as shown in Figure 7. This resistor isolates the load capacitance from the amplifier output and restores the phase margin. Figure 8 is a photograph of the response of a MAX412 driving a 6800pF load with a 22Ω isolation resistor.

For inverting configurations, the capacitive load driving performance of the MAX412 is plotted for closed loop gains of -1V/V and -10V/V in the %Overshoot vs. Capacitive Load graph in the typical operating characteristics section.

Total Supply Voltage Considerations

Although the MAX412 is specified with ±5V power supplies, it is also capable of operating with a total supply voltage as low as 4.8V. The input voltage range for normal amplifier operation is between V- +1.5V and V+ -1.5V. The output voltage range (with a 2K load) is from V+ -1.4V and V- +1.3V, for total supply voltages from 4.8V to 10V. Operating characteristics at total supply voltages of less than 10V are guaranteed by design and PSRR tests.

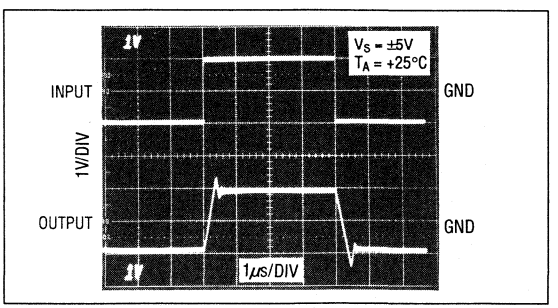


Figure 6. MAX412 Driving 100pF Load with No Isolation Resistor

Dual, Low-Noise, Low-Voltage Precision Op Amp

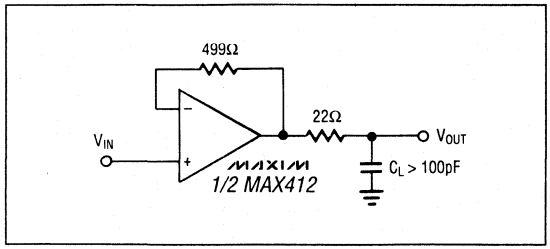


Figure 7. Capacitive Load Driving Circuit

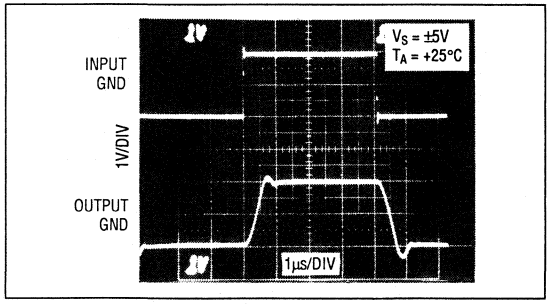
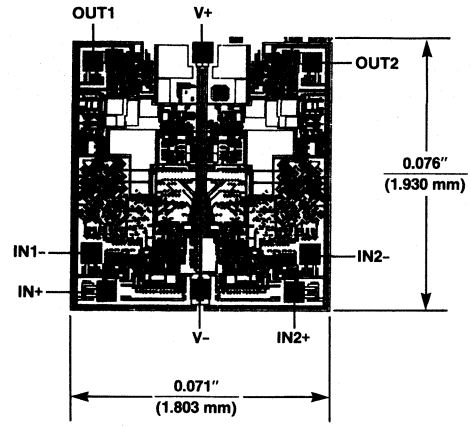


Figure 8. MAX412 Driving 6800pF Load with 22Ω Isolation Resistor

Chip Topography



MAXIM

High-Speed, Micropower Op Amps

General Description

The MAX438/MAX439 high-speed, low-voltage, micropower op amps feature a unique combination of high-speed performance and low-power operation. Both parts are designed for applications that require a closed-loop gain (A_{VCL}) of 5V/V or greater.

The MAX438 requires less than 75µA supply current while delivering a 6MHz gain-bandwidth product and a 10V/µs slew rate. For applications requiring increased speed, the MAX439 provides a 25MHz gain-bandwidth product and 60V/µs slew rate while consuming less than 375µA supply current. The MAX438/MAX439 micropower op amps have excellent output drive capability – the MAX438 drives ±3.6V into a 10kΩ load and the MAX439 drives ±3.3V into a 2kΩ load. Both op amps operate from dual ±3V to ±5V supplies, or from a single +6V to +10V.

Applications

Low-Power Signal Processing
Filters
Portable Instruments
Remote Sensors

Features

MAX438

- **6MHz Gain Bandwidth (A_{VCL} ≥ 5V/V)**
- **10V/µs Slew Rate**
- **75µA Max Supply Current**

MAX439

- **25MHz Gain Bandwidth (A_{VCL} ≥ 5V/V)**
- **60V/µs Slew Rate**
- **375µA Max Supply Current**

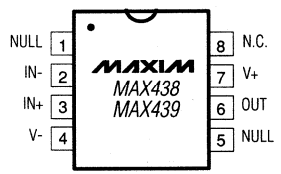
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX438CPA	0°C to +70°C	8 Plastic DIP
MAX438CSA	0°C to +70°C	8 SO
MAX438C/D	0°C to +70°C	Dice*
MAX438EPA	-40°C to +85°C	8 Plastic DIP
MAX438ESA	-40°C to +85°C	8 SO
MAX439CPA	0°C to +70°C	8 Plastic DIP
MAX439CSA	0°C to +70°C	8 SO
MAX439C/D	0°C to +70°C	Dice*
MAX439EPA	-40°C to +85°C	8 Plastic DIP
MAX439ESA	-40°C to +85°C	8 SO
MAX439MJA	-55°C to +125°C	8 CERDIP

** Dice are specified at TA = +25°C, DC parameters only.*
*** Contact factory for availability and processing to MIL-STD-883..*

Pin Configuration

TOP VIEW



DIP/SO

High-Speed, Micropower Op Amps

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V+ to V-) 12V
Input Voltage Range ..... (V+ + 0.3V) to (V- - 0.3V)
Differential Input Voltage ..... V+ to V-
Short-Circuit Current Duration ..... Indefinite
Maximum Current into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 909mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX43 _ C _ _ ..... 0°C to +70°C
MAX43 _ E _ _ ..... -40°C to +85°C
MAX439MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Absolute maximum ratings apply to packaged parts only, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX438			MAX439			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			0.5	2		0.5	2	mV
Offset Voltage Tempco $\Delta V_{OS}/\Delta T$	TCV_{OS}	$T_A = T_{MIN}$ to T_{MAX}		25			25		µV/°C
Input Bias Current	I_B			±2	±5		±5	±25	nA
Input Voltage Range	IVR		±3.5	±3.8		±3.5	±3.8		V
Differential Input Resistance	R_{IN} (DIFF)			90			18		MΩ
Common-Mode Input Resistance	R_{IN} (CM)			1			1		GΩ
Input Noise-Voltage Density	e_n	f_O = 10Hz		43			33		nV/√Hz
		f_O = 1000Hz		26			14		
Input Noise-Current Density	i_n	f_O = 10Hz		0.06			0.25		pA/√Hz
		f_O = 1000Hz		0.03			0.07		
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	75	95		66	80		dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	56	65		60	70		dB
Large-Signal Gain	A_{VOL}	R_L = 10kΩ	68	75			80		dB
		R_L = 2kΩ				68	75		
Output Voltage Swing	V_{OUT}	R_L = 10kΩ	±3.6	±3.9		±3.6	±3.9		V
		R_L = 2kΩ				±3.3	±3.6		
Short-Circuit Output Current	I_{SC}			3			5		mA
Slew Rate	SR	10kΩ | | 20pF load	7	10		40	60		V/µs
Gain Bandwidth	GBW	10kΩ | | 20pF load	4	6		18	25		MHz
Quiescent Current	I_Q		40	50	75	200	250	375	µA
Minimum Closed-Loop Gain	A_{VCL}		±5			±5			V/V

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = 0°C to +70°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX438			MAX439			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}				4			4	mV
Input Bias Current	I_B				±10			±50	nA
Input Voltage Range	IVR		±3.5			±3.5			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	70			66			dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	54			60			dB
Large-Signal Gain	A_{VOL}	R_L = 10kΩ	66						dB
		R_L = 2kΩ				66			
Output Voltage Swing	V_{OUT}	R_L = 10kΩ	±3.5			±3.5			V
		R_L = 2kΩ				±3.2			
Slew Rate	SR	10kΩ I I 20pF load	6.3			36			V/µs
Gain Bandwidth	GBW	10kΩ I I 20pF load	3.7			16.5			MHz
Quiescent Current	I_Q		35		90	175		450	µA
Minimum Closed-Loop Gain	A_{VCL}		±5			±5			V/V

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, T_A = -40°C to +85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MAX438			MAX439			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}				5			5	mV
Input Bias Current	I_B				±20			±100	nA
Input Voltage Range	IVR		±3.5			±3.5			V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±3.5V	68			66			dB
Power-Supply Rejection Ratio	PSRR	V_S = ±4.5V to ±5.5V	52			58			dB
Large-Signal Gain	A_{VOL}	R_L = 10kΩ	63						dB
		R_L = 2kΩ				63			
Output Voltage Swing	V_{OUT}	R_L = 10kΩ	±3.4			±3.4			V
		R_L = 2kΩ				±3.0			
Slew Rate	SR	10kΩ I I 20pF load	5.6			32			V/µs
Gain Bandwidth	GBW	10kΩ I I 20pF load	3.4			15			MHz
Quiescent Current	I_Q		30		95	150		475	µA
Minimum Closed-Loop Gain	A_{VCL}		±5			±5			V/V

19-4446; Rev. 0; 8/91

MAXIM

Quad Comparator with Programmable Threshold

General Description

The MAX516 combines four low-power, programmable-threshold comparators on a single CMOS IC. Separate 8-bit digital-to-analog converters (DACs) drive the comparator inverting (-) inputs so that individual trip thresholds can be digitally set. All noninverting (+) comparator inputs are brought out as analog inputs (AIN0-AIN3). Each comparator output swings high when its analog input exceeds its digitally set threshold. All four DACs share a common reference input to optimize matching and eliminate external trims.

Digital inputs and comparator outputs are compatible with TTL and CMOS logic. A separate logic supply (V_{CC}) allows comparator output levels to be set independently of V_{DD}. The MAX516 operates conveniently from a single supply with V_{DD} tied to V_{CC}. Commercial, extended, and military temperature ranges are provided in 24-pin narrow DIP and wide SO packages.

Applications

Window Comparators

Power-Supply Monitors

Alarm Limit Detectors

Battery Chargers

Automated Test Equipment

Process Control

Features

- ♦ **4 Comparators and 4 DACs**
- ♦ **Digitally Set Threshold**
- ♦ **Monotonic Over Temperature**
- ♦ **Parallel Microprocessor Interface**
- ♦ **+5V to +15V Supply Operation**

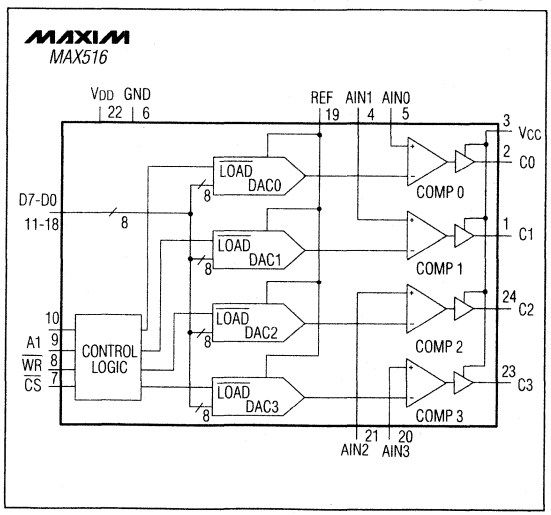
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX516ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX516BCNG	0°C to +70°C	24 Narrow Plastic DIP	±2
MAX516ACWG	0°C to +70°C	24 Wide SO	±1
MAX516BCWG	0°C to +70°C	24 Wide SO	±2
MAX516BC/D	0°C to +70°C	Dice*	±2
MAX516AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX516BENG	-40°C to +85°C	24 Narrow Plastic DIP	±2
MAX516AEWG	-40°C to +85°C	24 Wide SO	±1
MAX516BEWG	-40°C to +85°C	24 Wide SO	±2
MAX516AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1
MAX516BMRG	-55°C to +125°C	24 Narrow CERDIP**	±2

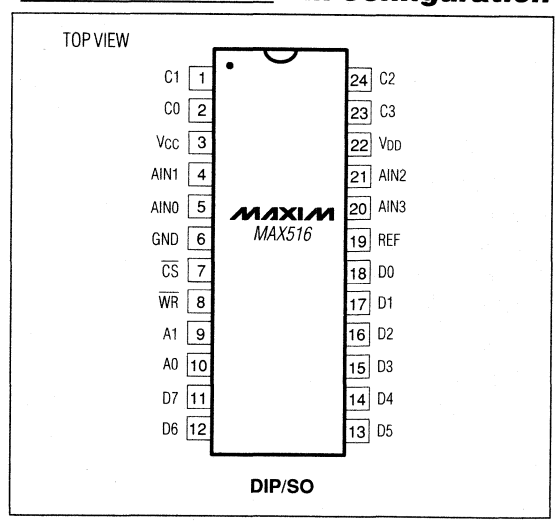
** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



Quad Comparator with Programmable Threshold

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND . . . . . -0.3V, +17V
V_{CC} to GND . . . . . -0.3V, V_{DD} + 0.3V
V_{DD} to V_{CC} . . . . . -0.3V, +17V
Digital Input Voltage to GND . . . . . -0.3V, V_{DD} + 0.3V
REF to GND . . . . . -0.3V, V_{DD} + 0.3V
Comparator Input to GND . . . . . -0.3V, V_{DD} + 0.3V
C0–C3 to GND (Note 1) . . . . . GND, V_{CC} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 8.7mW/°C above +70°C) 480mW
Wide SO (derate 11.8mW/°C above +70°C) 650mW
Narrow CERDIP (derate 12.5mW/°C above +70°C) . 690mW

Operating Temperature Ranges:
MAX516_ C__ . . . . . 0°C to +70°C
MAX516_ E__ . . . . . -40°C to +85°C
MAX516_ MRG . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +165°C
Lead Temperature (soldering, 10 sec) . . . . . +300°C

Note 1: The outputs may be shorted to GND or V_{DD}, provided the package's power dissipation is not exceeded.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = +4.75V, REF = +1.25V or V_{DD} = V_{CC} = +16.5V, REF = +10V; GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			8			Bits
Total Unadjusted Error	TUE	MAX516A				±1	LSB
		MAX516B				±2	
Relative Accuracy	INL	MAX516A				±0.5	LSB
		MAX516B				±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Full-Scale Error		MAX516A				±0.5	LSB
		MAX516B				±1	
Full-Scale Temperature Coefficient		V_{DD} = 15V, REF = 10V			±5		ppm/°C
Zero-Code Error		T_A = +25°C	MAX516A			±5	mV
		T_A = T_{MIN} to T_{MAX}	MAX516A			±10	
		T_A = +25°C	MAX516B			±10	
		T_A = T_{MIN} to T_{MAX}	MAX516B			±15	
Zero-Code Temperature Coefficient					±30		µV/°C
REFERENCE INPUT (4.75V ≤ V_{DD} ≤ 16.5V)							
Reference Input Range	REF			1.25		V_{DD} -3.50	V
Reference Input Resistance	RREF	Worst-case code		3.0	4.5		kΩ
Reference Input Capacitance	CREF	Worst-case code (Note 2)			100	250	pF
COMPARATOR INPUT (4.75V ≤ V_{DD} ≤ 16.5V)							
Comparator Input Range	V_{AIN}			0		V_{DD}	V
Comparator Input Bias Current	I_B	T_A = +25°C			50	300	nA
		T_A = T_{MIN} to T_{MAX}			100	400	

ELECTRICAL CHARACTERISTICS (continued)

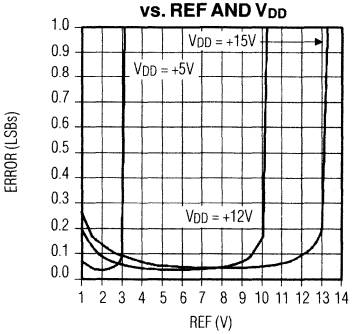
(V_{DD} = V_{CC} = +4.75V, REF = +1.25V or V_{DD} = V_{CC} = +16.5V, REF = +10V; GND = 0V; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS D0-D7, $\overline{WR}$, $\overline{CS}$, (4.75V ≤ V_{DD} ≤ 16.5V)						
Input High Voltage	V_{INH}		2.4			V
Input Low Voltage	V_{INL}				0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
Input Capacitance	C_{IN}	(Note 2)			10	pF
DIGITAL OUTPUTS C0-C3 (V_{CC} = 5V)						
Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	V_{CC}-1			V
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA			0.4	V
DYNAMIC PERFORMANCE (1.25V ≤ REF ≤ V_{DD} -3.5V, 0V ≤ AIN < V_{DD} -2V)						
Digital Input to Comparator Out Delay	t_{DCO}	(Note 3)		0.8	2.0	µs
Analog Input to Comparator Out Delay	t_{ACO}	(Note 4)		0.8	1.5	µs
TIMING CHARACTERISTICS						
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CH}		0			ns
Address to $\overline{WR}$ Setup TIme	t_{AS}		50	30		ns
Address to $\overline{WR}$ Hold TIme	t_{AH}		5	0		ns
Data Valid to $\overline{WR}$ Setup Time	t_{DS}		50	30		ns
Data Valid after $\overline{WR}$ Hold TIme	t_{DH}		5	0		ns
$\overline{WRITE}$ Pulse Width	t_{WR}		120	50		ns
POWER SUPPLIES						
V_{DD} Range	V_{DD}		4.75		16.5	V
V_{CC} Range	V_{CC}		4.75		V_{DD}+0.30	V
Positive Supply Current	I_{DD}	Logic inputs < V_{IL} or > V_{IH}			10	mA
Logic Supply	I_{CC}				10	µA

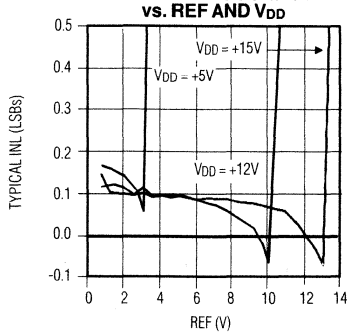
Note 2: Guaranteed by design. Not production tested.
Note 3: V_{DD} = 5.00V, differential comparator input voltage changes by 1.25V with 5mV overdrive. V_{IN} must be 3.5V less than V_{DD}, or longer propagation delays will result.
Note 4: Not tested, but guaranteed by correlation to t_{DCO}.

Typical Operating Characteristics

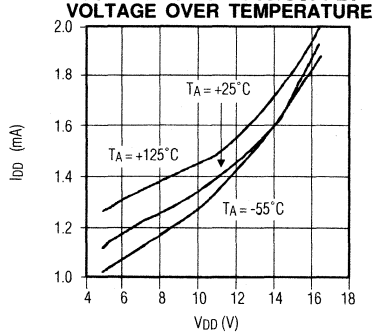
COMPARATOR ERROR AT CODE 255 vs. REF AND V_{DD}



RELATIVE ACCURACY vs. REF AND V_{DD}



SUPPLY CURRENT vs. SUPPLY VOLTAGE OVER TEMPERATURE



Quad Comparator with Programmable Threshold

Pin Description

PIN	NAME	FUNCTION
1, 2	C1, C0	Comparator Outputs
3	V_{CC}	Comparator Output Supply
4, 5	AIN1, AIN0	Comparator Analog Inputs
6	GND	Ground
7	$\overline{CS}$	CHIP SELECT
8	$\overline{WR}$	WRITE
9, 10	A1 , A0	DAC Address Inputs
11-18	D7-D0	DAC Data Inputs, 8 bits
19	REF	Reference Input
20, 21	AIN3, AIN2	Comparator Analog Inputs
22	V_{DD}	Positive Supply Voltage
23, 24	C3, C2	Comparator Outputs

Detailed Description

The MAX516 contains four analog comparators and four matched 8-bit digital-to-analog converters (DACs). The voltage output of each DAC is expressed in the equation:

$$V_{DAC} = REF \times N/256,$$

where N is the numerical equivalent of the 8-bit DAC input code (D0-D7). N ranges from 0 to 255 and may be set to a different level for each DAC (Table 1). The DAC output, V_{DAC}, does not appear on an output pin of the MAX516 but is instead compared to an analog input signal by one of four internal comparators (see *Functional Diagram*). A comparator output is high when AIN is more positive than the comparator's digitally set threshold.

Table 1. Comparator Threshold vs. DAC Input Code

DAC CODE MSB	DAC CODE LSB	COMPARATOR THRESHOLD
1111	1111	$+REF\left(\frac{255}{256}\right)$
1000	0001	$+REF\left(\frac{129}{256}\right)$
1000	0000	$+REF\left(\frac{128}{256}\right) = +\frac{REF}{2}$
0111	1111	$+REF\left(\frac{127}{256}\right)$
0000	0001	$+REF\left(\frac{1}{256}\right)$
0000	0000	0V

NOTE: $1LSB = (REF)(2^{-8}) = +REF\left(\frac{1}{256}\right)$

Reference Input

Comparator trip thresholds vary digitally between 0V and 1LSB below REF. All DACs share the same reference input.

The input impedance of REF is code dependent. The lowest impedance, typically 2kΩ, occurs when 0101 0101 (HEX 55) is loaded into D0-D7 on all four DACs. When 0000 0000 is loaded into all DACs, REF appears as an open circuit. Because the input resistance at REF is code dependent, the reference source should have an output impedance of no more than 4Ω to maintain linearity. Input capacitance at REF is also code dependent and typically varies between 100pF and 250pF.

Comparator Inputs

The "+" input of each comparator is brought out to AIN0-AIN3. Comparator input bias current is typically 100nA. Analog source resistances below 1.25kΩ generate less than 250µV of bias-current induced comparator offset error.

Digital Interface

The digital inputs (D0-D7, $\overline{CS}$, $\overline{WR}$) are both TTL and 5V CMOS logic compatible; however, the power-supply current, I_{DD}, depends on input logic levels. Supply currents will be highest with TTL levels (tested limits are with worst-case logic levels). Supply current is reduced when digital inputs are driven near GND and above 4V.

Address lines A0 and A1 select which DAC receives data from the input port. Because $\overline{CS}$ and $\overline{WR}$ are internally ORed, the write cycle begins only after both go low, but data is latched and transferred to a DAC when either input returns high. Figure 1 shows the input control logic, Table 2 lists DAC addresses, and Table 3 is the truth table for $\overline{WR}$ and $\overline{CS}$. Figure 2 shows write-cyle timing.

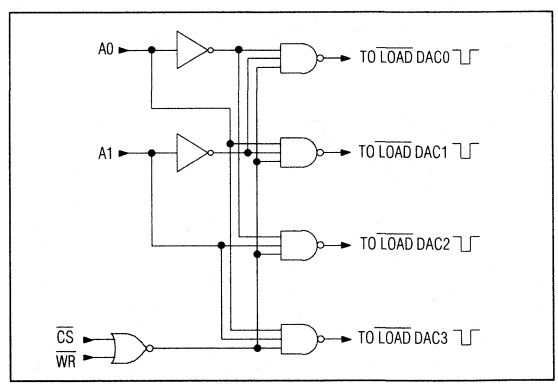


Figure 1. Input Control Logic

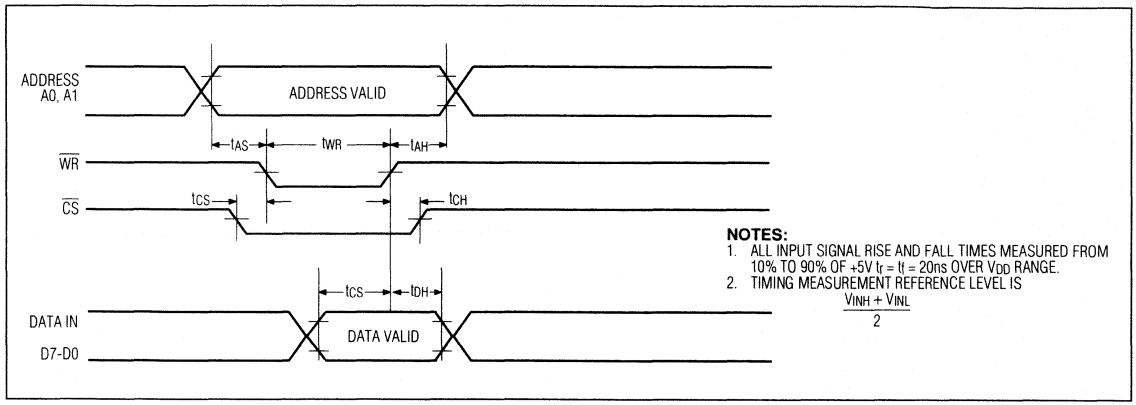


Figure 2. Write-Cycle Timing

Table 2. DAC Addressing

A1	A0	SELECTED DAC
0	0	DAC0 Input Register
0	1	DAC1 Input Register
1	0	DAC2 Input Register
1	1	DAC3 Input Register

Table 3. Write-Cycle Truth Table

CS	WR	FUNCTION
1	X	No operation. The MAX516 is deselected. Existing register contents remain unchanged.
0	0	DAC contents for selected address are loaded, but do not update the DAC until WR goes high.
0	↑	Latch D0-D7 into input register of the selected DAC on rising edge.

NOTES: X = Don't Care, ↑= Rising Edge

Applications Information

Power-Supply and Reference Operating Ranges

The MAX516 is fully specified to operate with V_{DD} between +4.75V and +16.5V and is specified to operate with a reference input range of +1.25V to V_{DD} -3.5V.

The comparator output supply, V_{CC}, has a range of +4.5V to (V_{DD} + 0.3V). This allows the comparators' logic-high output levels to be set independently from V_{DD}. In most applications, simply connect V_{CC} and V_{DD} together. Comparator outputs typically swing within 200mV of the supply rails when loaded with CMOS logic inputs.

Hysteresis

When analog input signals are slow moving or contain noise, comparator outputs may "chatter" near the threshold point. Be sure that proper power-supply bypass capacitors are in place (see *Grounds and Bypassing* section), because supply current rises when an output switches.

Hysteresis may be added to any or all comparators to further resist oscillation during output transitions. This is accomplished with two resistors, as shown in Figure 3. When hysteresis is added, the threshold point will shift slightly as a result of the voltage divider formed by R1 and R2. The amount of shift is described below:

$$V_{TH} = V_T\left(\frac{R1}{R2} + 1\right)$$

$$V_{TL} = V_T\left(\frac{R1}{R2} + 1\right) - V_{CC}\left(\frac{R1}{R2}\right)$$

$$V_{HYST} = V_{TH} - V_{TL}$$

$$V_{HYST} = V_{CC}\left(\frac{R1}{R2}\right)$$

V_T is the threshold voltage set by the internal DAC with no hysteresis connected. V_{TH} is the shifted high-going threshold with hysteresis added. V_{TL} is the shifted low-going threshold with hysteresis. V_{HYST} is the total hysteresis and equals V_{TH} - V_{TL}. Note that V_{TL} and V_{HYST} change with V_{CC}. With V_{CC} = 5V, R1 = 1kΩ, and R2 = 200kΩ, V_{HYST} = 25mV. Even though R1 is relatively small, the impedance seen by the signal source is large: R1 + R2. However, if R1 is large, input bias current (400nA

Quad Comparator with Programmable Threshold

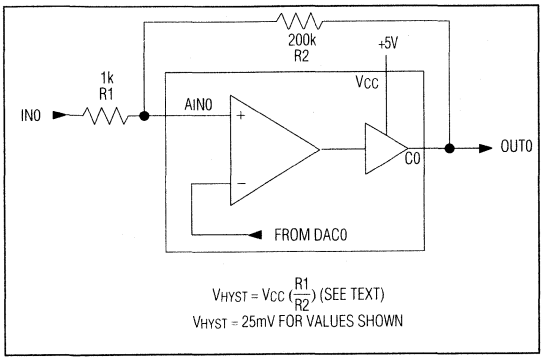


Figure 3. Adding Hysteresis to Any Comparator

max over temp.) may add offset error. 1kΩ x 400nA = 0.4mV offset error is due to bias current.

Grounds and Bypassing

Careful PC-board layout significantly minimizes crosstalk among the reference input, comparator outputs, and digital inputs. Keep digital and analog lines separate, and use ground traces as shields between them where possible. Separate AIN0-AIN3 and REF from each other by running a ground trace between these pins.

Bypass both V_{DD} and V_{CC} to GND with a combination of a 0.1µF low ESR and a 4.7µF capacitor close to the device. If V_{DD} and V_{CC} are connected together, only one set of bypass capacitors is needed. If REF is not an AC input, it should be bypassed as well. Keep bypass-capacitor leads short for best supply noise rejection.

Applications

Threshold detection is often useful in automated test applications. Four individual thresholds can be independently altered under software control.

Figure 4 shows the connection for a hardware window comparison. DAC0 provides the upper trip point, DAC1 the lower trip point. The difference between the trip points is the window size. The AIN0 and AIN1 inputs are tied together. One logic output is inverted and then ORed with the noninverted comparator output. The window output goes high when the analog input sits between the thresholds set by DAC0 and DAC1. The external logic in Figure 4 can also be simulated in software, or use a single comparator to perform a window comparison by loading two threshold limits in succession and noting the comparator results of each (Figure 5).

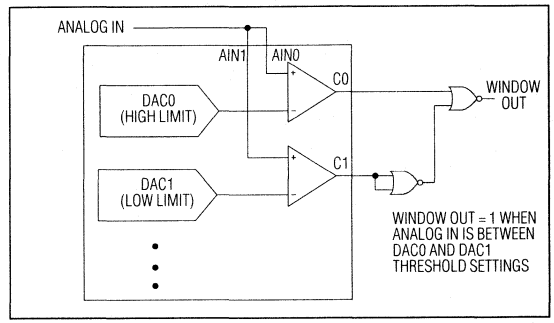


Figure 4. Window Comparison

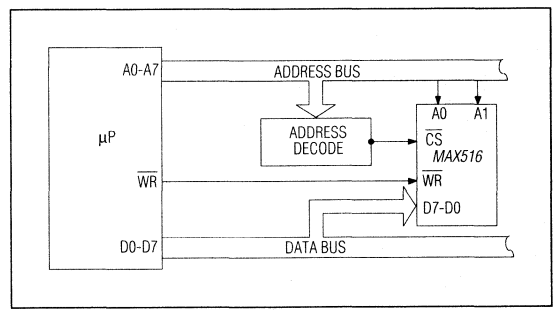
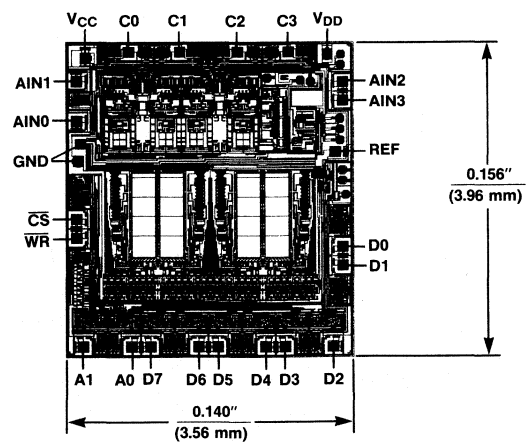


Figure 5. Microprocessor Interface

Chip Topography



NOTE: Substrate connected to V_{DD}

19-4519; Rev. 0; 1/92

MAXIM

High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

General Description

The MAX905/MAX906 high-speed, single and dual ECL-compatible voltage comparators eliminate oscillation by separating the comparator input and output stages with a positive edge-triggered master-slave D flip-flop. Comparator propagation delay is typically 2ns, and is insensitive to input overdrive. The MAX905 and MAX906 resolve input signals as small as 3mV and 4mV respectively.

These comparators feature separate analog and digital ground connections for maximum noise rejection, and operate from either dual supplies or from a single supply. Input common-mode voltage range extends to the negative supply rail for a wide 7.9V input voltage range with ±5V supplies.

The MAX905 is a single ECL comparator, available in 14-pin DIP and SO packages. The MAX906 is a dual version available in 16-pin DIP and SO packages.

Applications

High-Speed A/D Converters

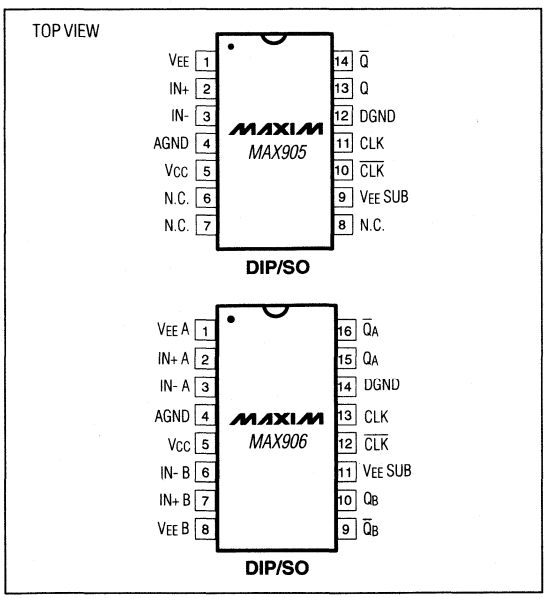
High-Speed Line Receivers

Peak Detectors

Threshold Detectors

High-Speed Triggers

Pin Configurations



Features

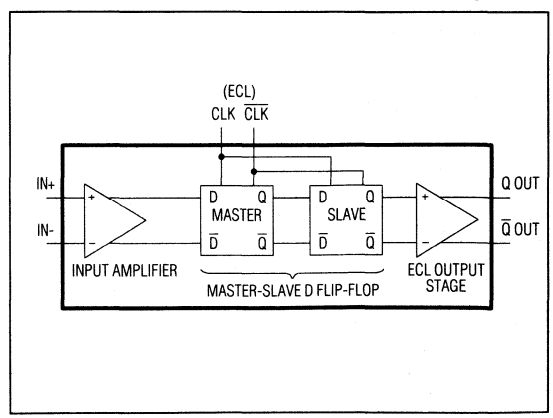
- ♦ **Immune to Oscillation: Clocked Architecture**
- ♦ **2ns Setup Time**
- ♦ **2ns Propagation Delay**
- ♦ **Prop Delay Independent of Overdrive**
- ♦ **3mV Input Resolution (MAX905)**
- ♦ **Input Range Includes Negative Supply Rail**
- ♦ **Single- or Dual-Supply Capability**
- ♦ **Separate Analog and Digital Supplies**
- ♦ **Low Power: 180mW/Comparator**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX905CPD	0°C to +70°C	14 Plastic DIP
MAX905CSD	0°C to +70°C	14 Narrow SO
MAX905C/D	0°C to +70°C	Dice*
MAX905EPD	-40°C to +85°C	14 Plastic DIP
MAX905ESD	-40°C to +85°C	14 Narrow SO
MAX905MJD	-55°C to +125°C	14 CERDIP
MAX906CPE	0°C to +70°C	16 Plastic DIP
MAX906CSE	0°C to +70°C	16 Narrow SO
MAX906C/D	0°C to +70°C	Dice*
MAX906EPE	-40°C to +85°C	16 Plastic DIP
MAX906ESE	-40°C to +85°C	16 Narrow SO

Contact factory for dice specifications.

Functional Diagram



High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

ABSOLUTE MAXIMUM RATINGS

Analog Supply Voltage (V_{CC} to V_{EE}) ..... +12V
Digital Supply Voltage (V_{EE} to GND) ..... -6V
Differential Input Voltage ..... (V_{EE} - 0.2V) to (V_{CC} + 0.2V)
Common-Mode Input Voltage .... (V_{EE} - 0.2V) to (V_{CC} + 0.2V)
Clock Input Voltage (CLK or $\overline{CLK}$) .. (V_{EE} - 0.2V) to DGND + 0.2V
Output Current (Q or $\overline{Q}$) 30mA
Output Short-Circuit Duration (Q or $\overline{Q}$ to GND) ..... Indefinite
Continuous Power Dissipation
MAX905 DIP (derate 10.00mW/°C above +70°C) 800mW
SO (derate 8.00mW/°C above +70°C) 640mW
CERDIP (derate 9.09mW/°C above +70°C) ... 727mW
MAX906 DIP (derate 10.53mW/°C above +70°C) 842mW
SO (derate 8.70mW/°C above +70°C) 696mW

Operating Temperature Ranges:
MAX90_C_ _ ..... 0°C to +70°C
MAX90_E_ _ ..... -40°C to +85°C
MAX90_MJD ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... -65°C to +170°C
Lead Temperature (soldering , 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = 0V	MAX905		0.5	1.0	mV
			MAX906		0.5	1.5	
Input Bias Current	I_B	I_{B+} or I_{B-}			4	10	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			0.1	1.0	µA
Input Referred Noise Voltage	e_n	(Note 1)			600	900	µV
Input Common-Mode Range	V_{CM}	(Note 2)		V_{EE} - 0.1		V_{CC} - 2.2	V
Common-Mode Rejection Ratio	CMRR	Over V_{CM} range	MAX905		60	120	µV/V
			MAX906		60	180	
Power-Supply Rejection Ratio	PSRR	(Note 3)			60	120	µV/V
Output High Voltage	V_{OH}	(Note 4)		-0.96		-0.81	V
Output Low Voltage	V_{OL}	(Note 4)		-1.85		-1.65	V
Clock Input Voltage High	V_{CH}			-0.96		0	V
Clock Input Voltage Low	V_{CL}			-2.00		-1.65	V
Clock Input Current High	I_{CH}					50	µA
Clock Input Current Low	I_{CL}					50	µA
Positive Supply Current	I_{CC}	(Note 5)	MAX905		5	8	mA
			MAX906		10	16	
Negative Supply Current	I_{EE}	(Note 5)	MAX905		18	24	mA
			MAX906		36	48	
Power Dissipation	PD	(Notes 5, 6)	MAX905		180	260	mW
			MAX906		360	520	
Positive Propagation Delay	t_{PD+}	(Notes 7, 8)			1.8	3.5	ns
Negative Propagation Delay	t_{PD-}	(Notes 7, 8)			1.8	3.5	ns
Clock Setup Time	t_S	V_{OD} = 5mV (Note 8)			2.0		ns
		V_{OD} = 10mV (Notes 7, 8)			1.5	3.0	

High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

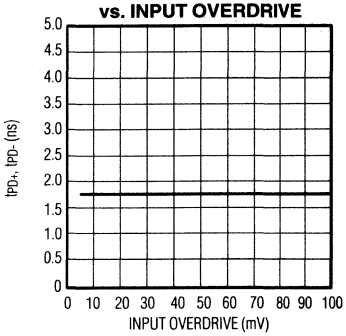
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	V_{CM} = 0V	MAX905C		0.5	1.5	mV
			MAX905E/M		0.5	2.5	
			MAX906C		0.5	2.5	
			MAX906E/M		0.5	3.5	
Input Bias Current	I_B	I_{B+} or I_{B-}			6	15	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			0.2	2.0	µA
Input Referred Noise Voltage	e_n	(Note 1)			600	900	µV
Input Common-Mode Range	V_{CM}	(Note 2)		V_{EE} - 0.1		V_{CC} - 2.2	V
Common-Mode Rejection Ratio	CMRR				80	180	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 3)			70	150	µV/V
Output High Voltage (Note 4)	V_{OH}	T_A = -55°C		-1.11		-0.93	V
		T_A = -40°C		-1.08		-0.91	
		T_A = 0°C		-1.01		-0.85	
		T_A = +70°C		-0.90		-0.72	
		T_A = +85°C		-0.89		-0.70	
		T_A = +125°C		-0.85		-0.63	
Output Low Voltage (Note 4)	V_{OL}	T_A = -55°C		-1.90		-1.69	V
		T_A = -40°C		-1.90		-1.68	
		T_A = 0°C		-1.87		-1.66	
		T_A = +70°C		-1.83		-1.62	
		T_A = +85°C		-1.83		-1.62	
		T_A = +125°C		-1.80		-1.60	
Clock Input Voltage High	V_{CH}			-1.11		0	V
Clock Input Voltage Low	V_{CL}			-2.00		-1.60	V
Clock Input Current High	I_{CH}					50	µA
Clock Input Current Low	I_{CL}					50	µA
Positive Supply Current	I_{CC}	(Note 5)	MAX905		6	10	mA
			MAX906		12	20	
Negative Supply Current	I_{EE}	(Note 5)	MAX905		23	32	mA
			MAX906		46	64	
Power Dissipation	PD	(Notes 5, 6)	MAX905		220	320	mW
			MAX906		440	640	
Positive Propagation Delay	t_{PD+}	(Notes 7, 8)			2.0	4.0	ns
Negative Propagation Delay	t_{PD-}	(Notes 7, 8)			2.0	4.0	ns
Clock Setup Time	t_S	V_{OD} = 10mV (Notes 7, 8)			2.0	4.0	ns

Note 1: Guaranteed by design. Input Referred Noise Voltage uncertainty is specified over the full bandwidth of the device.
Note 2: The input common-mode voltage or either input signal voltage should not be allowed to go more than 0.2V below V_{EE}. The upper input common-mode range limit is typically V_{CC} - 2V, but either input can go to V_{CC} + 0.2V without damage.
Note 3: Tested for +4.75V < V_{CC} < +5.25V and -5.50V < V_{EE} < -4.75V.
Note 4: Tested with R_{LOAD} = 50Ω terminated in -2V.
Note 5: I_{CC}, I_{EE} and PD tested for worst-case condition of V_{CC} = +5.25V and V_{EE} = -5.5V.
Note 6: Includes internal power dissipation due to external load resistors.
Note 7: Guaranteed by design. Measured in a high-speed fixture with R_{LOAD} = 50Ω, and C_{LOAD} = 15pF, terminated into -2V.
Note 8: Clock input voltage rise and fall times should not exceed 50ns for correct triggering of comparator.

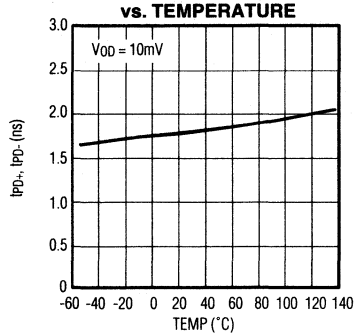
High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

Typical Operating Characteristics

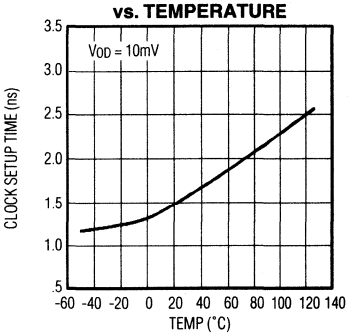
PROPAGATION DELAY vs. INPUT OVERDRIVE



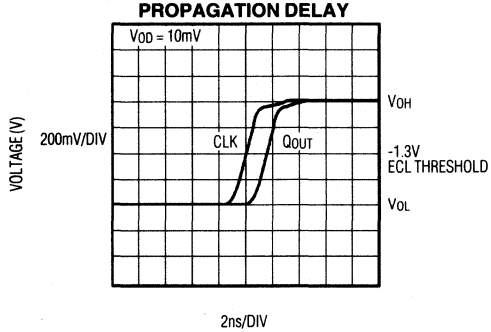
PROPAGATION DELAY vs. TEMPERATURE



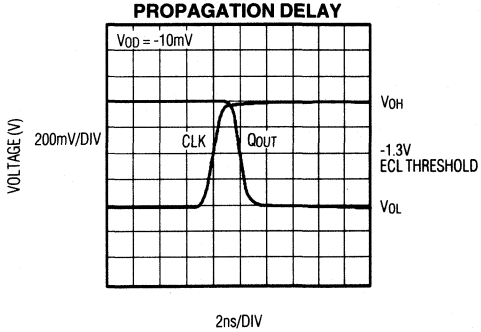
CLOCK SETUP TIME vs. TEMPERATURE



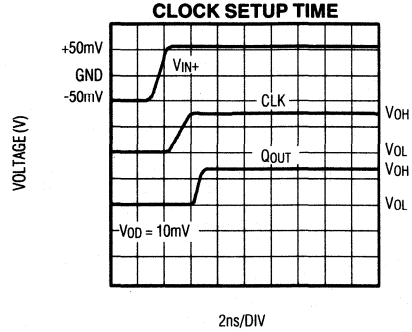
POSITIVE PROPAGATION DELAY



NEGATIVE PROPAGATION DELAY



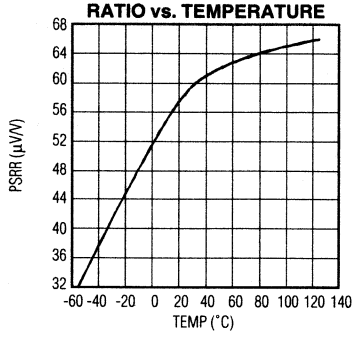
CLOCK SETUP TIME



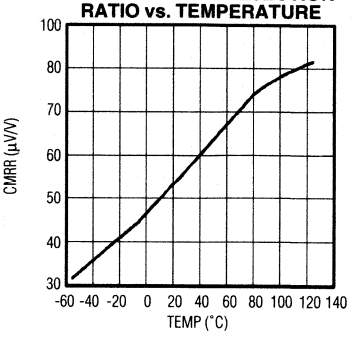
High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

Typical Operating Characteristics (continued)

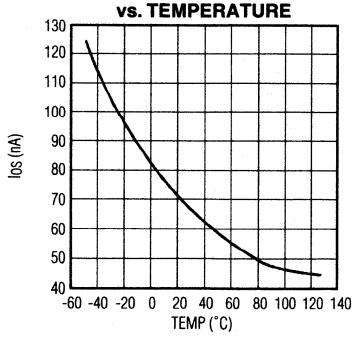
POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



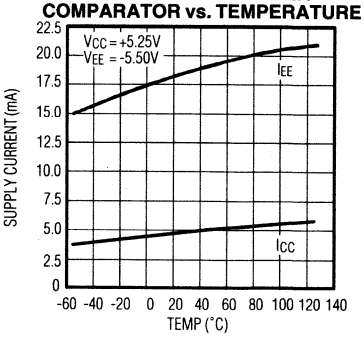
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



INPUT OFFSET CURRENT vs. TEMPERATURE



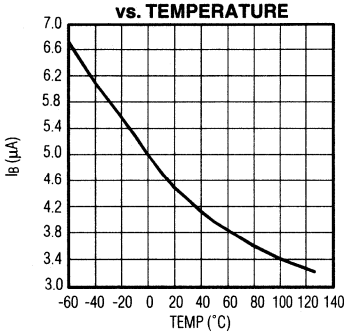
SUPPLY CURRENT PER COMPARATOR vs. TEMPERATURE



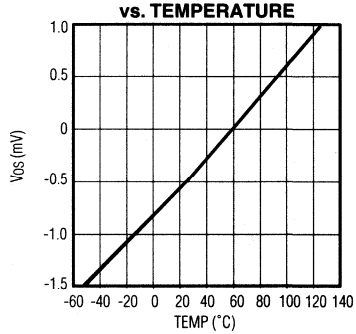
High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

Typical Operating Characteristics (continued)

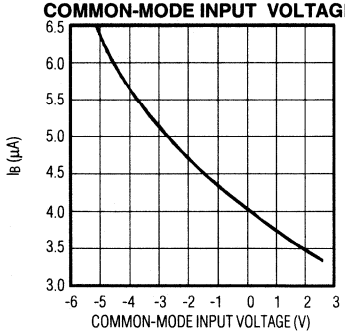
INPUT BIAS CURRENT vs. TEMPERATURE



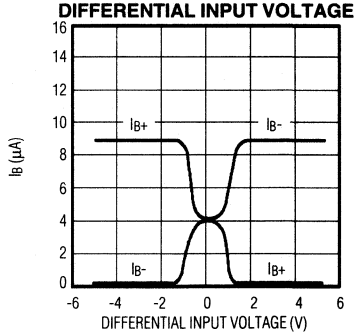
INPUT OFFSET VOLTAGE vs. TEMPERATURE



INPUT BIAS CURRENT vs. COMMON-MODE INPUT VOLTAGE



INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

Pin Description

MAX905		
PIN	**NAME**	**FUNCTION**
1	V_{EE}	Negative Digital Supply
2	IN+	Positive Input
3	IN-	Negative Input
4	AGND	Analog Ground Terminal
5	V_{CC}	Positive Analog Supply
6,7,8	N.C.	No Connect
9	V_{EE} SUB	Negative Analog Supply
10	$\overline{CLK}$	Negative ECL Clock Input
11	CLK	Positive ECL Clock Input
12	DGND	Digital Ground Terminal
13	Q	Positive ECL Output
14	$\overline{Q}$	Negative ECL Output

MAX906		
PIN	**NAME**	**FUNCTION**
1	$V_{EE}A$	Negative Digital Supply (Channel A)
2	IN+ A	Positive Input (Channel A)
3	IN- A	Negative Input (Channel A)
4	AGND	Analog Ground Terminal
5	V_{CC}	Positive Analog Supply
6	IN- B	Negative Input (Channel B)
7	IN+ B	Positive Input (Channel B)
8	$V_{EE}B$	Negative Digital Supply (Channel B)
9	$\overline{Q}_B$	Negative ECL Output (Channel B)
10	Q_B	Positive ECL Output (Channel B)
11	V_{EE} SUB	Negative Analog Supply
12	$\overline{CLK}$	Negative ECL Clock Input
13	CLK	Positive ECL Clock Input
14	DGND	Digital Ground Terminal
15	Q_A	Positive ECL Output (Channel A)
16	$\overline{Q}_A$	Negative ECL Output (Channel A)

Device Overview

The MAX905 (single) and MAX906 (dual) are ultra high-speed ECL-compatible comparators with an internal positive edge-triggered master-slave D flip-flop. Unlike industry-standard ECL comparators, this architecture breaks the input-to-output signal path to accomplish the following:

1) Prevent oscillations caused by unwanted parasitic feedback when the comparator is in its linear region. No minimum input slew rate is required.

2) Propagation delay remains constant with varying input overdrive.

Detailed Description

The comparator can be divided into three stages, as shown in Figure 1:

1) Input Amplifier

2) Master-Slave D Flip-Flop

3) ECL Output Stage

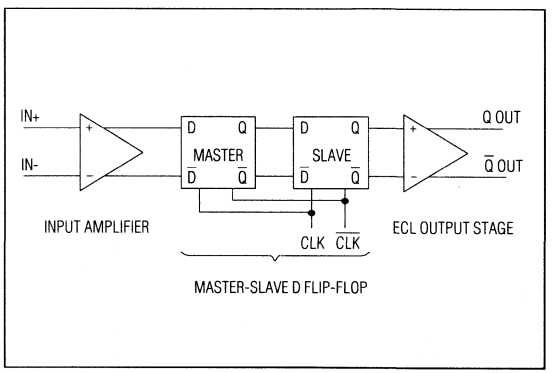


Figure 1. MAX905/MAX906 Block Diagram

Input Amplifier

The comparator input amplifier is fully differential. Input offset voltage is trimmed to less than 1.0mV for the MAX905, and less than 1.5mV for the MAX906. Input common-mode range extends from 100mV below the negative supply rail (V_{EE}) to 2.2V below the positive supply rail (V_{CC}). Total input voltage range is 7.9V when operating from ±5V supplies.

The master-slave architecture enables the MAX905 to compare input signals down to 3mV over its entire common-mode range. Similarly, the MAX906 compares input signals as low as 4mV (see Table 1). Any input signal less than 3mV (4mV for MAX906) may not be distinguished from the comparator's total worst-case DC error. The MAX905/MAX906 total worst-case DC error is calculated by summing input offset voltage (V_{OS}), input referred noise (e_n), common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSRR). Table 1 shows the maximum total input referred error at +25°C and over temperature. For many applications, take the RMS summation of the individual errors for a more meaningful representation of the total input referred error (see Table 2).

High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

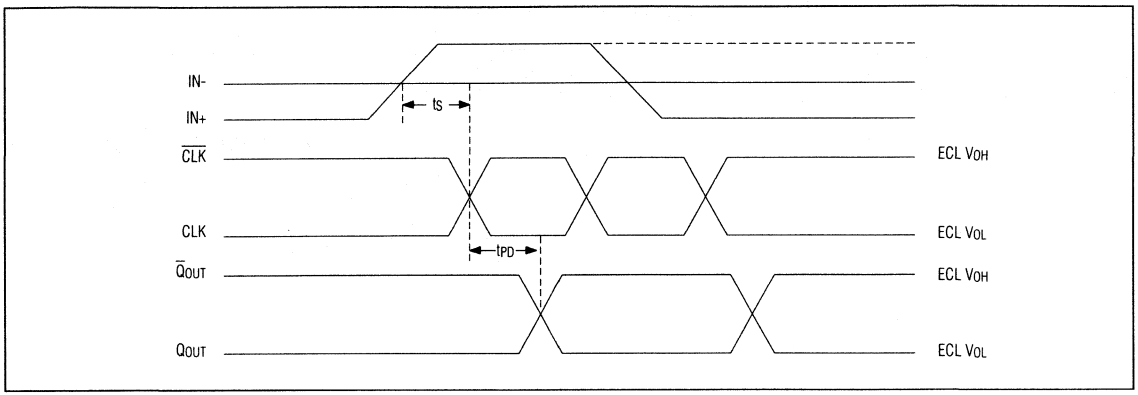


Figure 2. Timing Diagram

Table 1. Total Worst-Case Input Referred Error/Resolution

Part	+25°C (mV)	Commercial Temp. (mV)	Ext. Ind/Military Temp. (mV)
MAX905	3	4	5
MAX906	4	5	6

Table 2. Total RMS Input Referred Error/Resolution

Part	+25°C (mV)	Commercial Temp. (mV)	Ext. Ind/Military Temp. (mV)
MAX905	1.7	2.3	3.0
MAX906	2.3	3.0	3.9

Master-Slave D Flip-Flop

The master-slave D flip-flop is immune to metastability by design, and propagation delay is independent of input overdrive (V_{OD}). The MAX905/MAX906 master flip-flop has an input stage that samples the output of the input amplifier and a latch to hold the sampled data when the master input stage is disabled. The latched data is transferred to the MAX905/MAX906 slave flip-flop only on the clock's rising edge. The input amplifier continuously monitors the input signal.

Clock Cycle

Clock Low: When the clock is low, the master flip-flop's input stage samples the output of the input amplifier. The slave flip-flop maintains valid outputs from the previously sampled data. The comparator inputs are isolated from the comparator outputs because the slave flip-flop's input stage is disabled. See Figure 2.

Clock Rising Edge: On the rising edge of the clock, the master flip-flop input stage turns off and the latch holds the sampled data. Shortly after, the slave input stage turns on and samples the outputs of the master. The ECL output stage simultaneously receives data from the slave.

Clock High: The slave flip-flop continues to sample data from the master while the clock is high. The master flip-flop latch holds data from the previous rising clock edge.

Clock Falling Edge: On the falling edge of the clock, data from the previous rising clock edge is latched into the slave, and the input of the master flip-flop is turned on. New data is not transferred to the ECL output stage on the falling edge of the clock cycle.

ECL Output Stage

The ECL output stage receives data from the slave flip-flop. Proper ECL output voltage levels and temperature coefficients are maintained by the output amplifier over commercial, extended industrial, and military temperature ranges. The comparator's outputs (Q and $\overline{Q}$) are fully differential and MECL 10k compatible.

Applications Information

Maximum Clock Rate

The MAX905/MAX906 maximum clock frequency is a direct function of the comparator's minimum clock setup time. Typical clock setup time is 2ns, which translates to a theoretical 500MHz maximum clock frequency. As shown in Figure 3, the maximum output toggle rate is 1/2 the clock frequency, because the comparator triggers only on the rising edge of each clock cycle.

For proper clock triggering, the MAX905/MAX906 ECL clock rise and fall times must be less than 50ns. If clock rise/fall times are greater than 50ns, the comparator may incorrectly sample the input signal at the clock's falling edge.

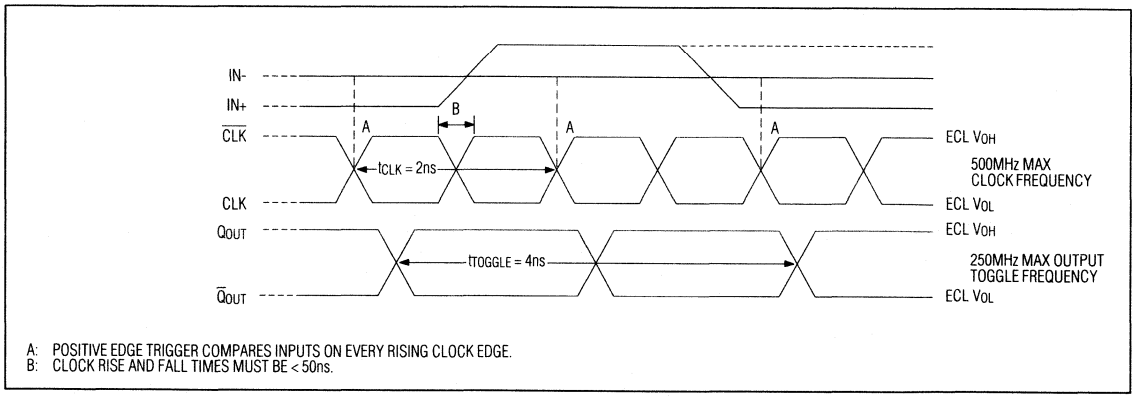


Figure 3. Maximum Clock Rate Timing Diagram

Power Supplies

The MAX905/MAX906 are tested while operating from ±5V supplies. The comparators also operate from standard ECL +5V and -5.2V power supplies with the same guaranteed performance.

In high-speed, mixed-signal applications where a common ground is shared, a noisy digital environment can adversely affect the integrity of the analog input signal. The MAX905/MAX906 isolate the analog and digital signals by providing separate analog (AGND) and digital (DGND) grounds. For applications that cannot separate analog and digital grounds, AGND and DGND may be tied together if a good ground plane is available.

The MAX905/MAX906 offer the unique ability to operate from a single supply. The comparators' input common-mode voltage range includes the negative supply rail. Figure 4 shows the two supply voltage conditions:

1) Dual ±5V Supplies (or +5V and -5.2V)

2) Single -5V Supply (or -5.2V)

Input Slew Rate

The MAX905/MAX906's master-slave architecture eliminates the minimum input slew-rate requirement common to standard comparator architectures. As long as the comparator is clocked after the minimum data-to-clock setup time requirement, and the input is greater

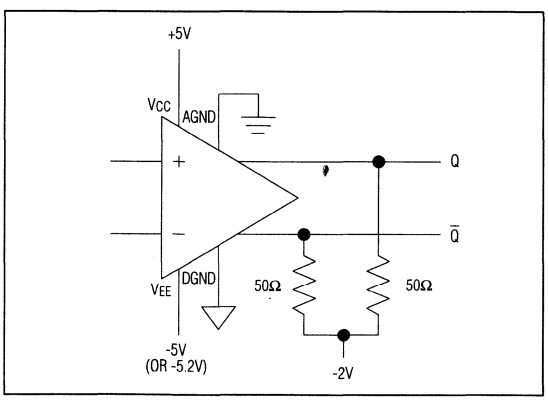


*Figure 4a. ±5V Supplies, Separate Ground**

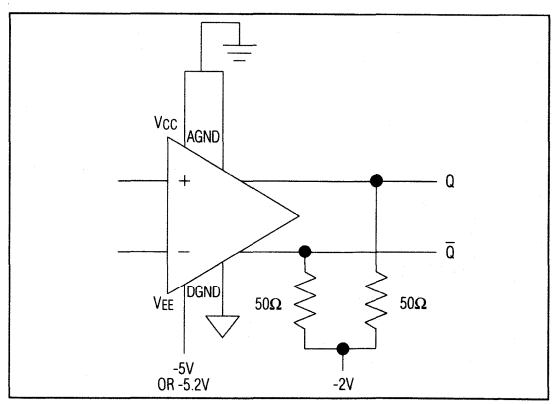


*Figure 4b. Single -5V Supply, Separate Ground**

** Separate ground is optional. DGND and AGND may be tied together.*

High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

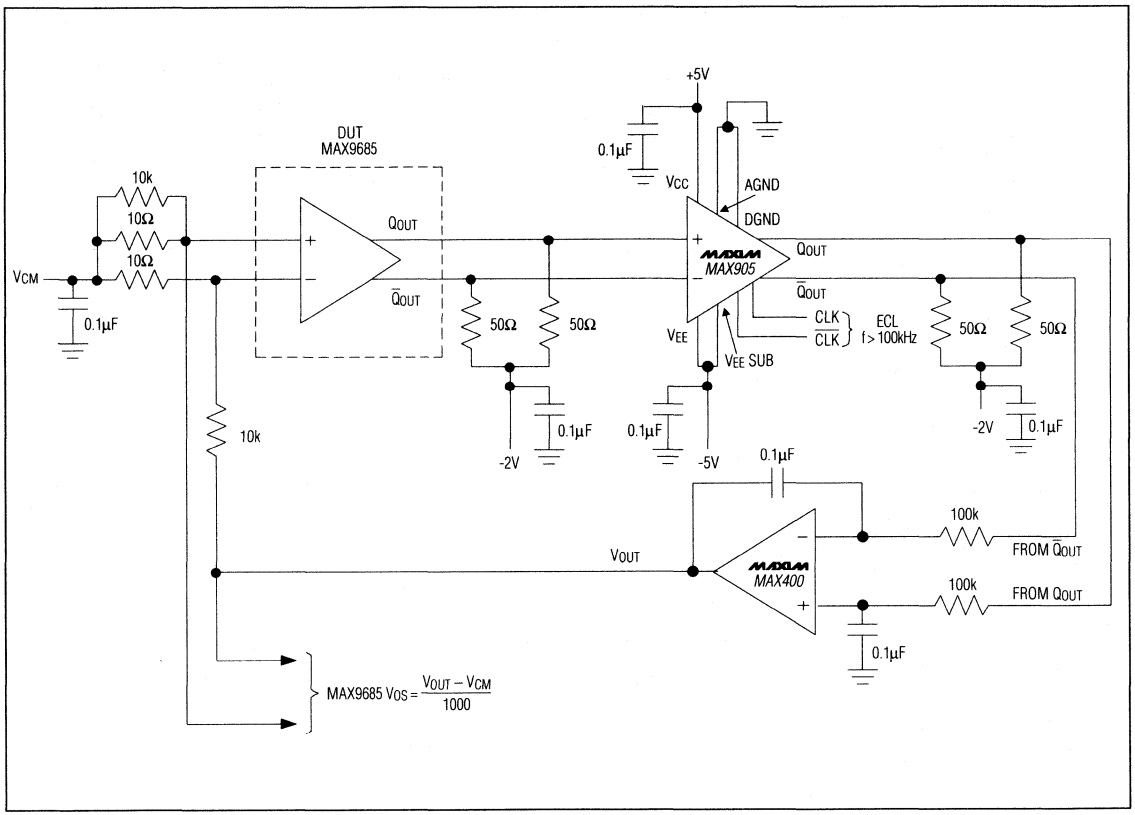


Figure 5. High-Speed Comparator V_{OS} Measurement Circuit

than the comparator's total DC error, the output data will be valid without oscillations.

Board Layout

As with all high-speed components, careful high-speed board layout and bypassing are essential for optimal performance. A printed circuit board with low inductance and separate digital and analog grounds is recommended. All decoupling capacitors should be mounted as close to the comparator power-supply pins as possible, with ground return lead lengths as short as possible. Pay close attention to the bandwidth of the decoupling and terminating components. Soldering the MAX905/MAX906 and other components directly to the board without sockets minimizes unwanted parasitic capacitance.

Typical Application

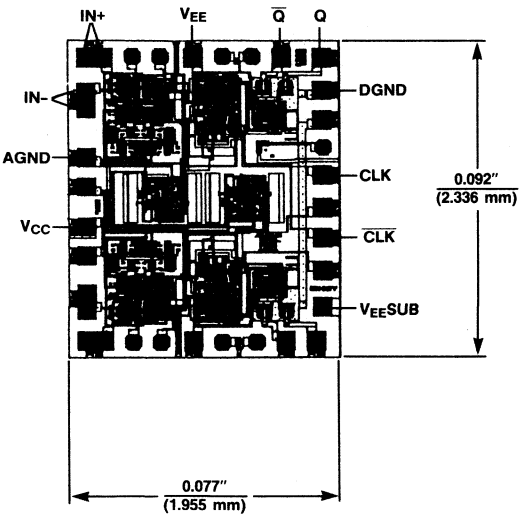
High-Speed Comparator V_{OS} Measurement Circuit: The circuit of Figure 5 shows the MAX905 used to measure input offset voltage (V_{OS}) of the MAX9685, an ultra high-speed ECL comparator. When the MAX9685 comparator is put into a standard op-amp test loop, its high-frequency open-loop gain causes oscillations. However, in this application, the MAX9685's output feeds into the MAX905, which then feeds into a differential integrator. The MAX905's D flip-flop architecture breaks the feedback path that normally causes oscillations. The test loop forces the MAX9685's output to switch with a precise 50% duty cycle, thus

$$V_{OS} = \frac{V_{OUT} - V_{CM}}{1000}.$$

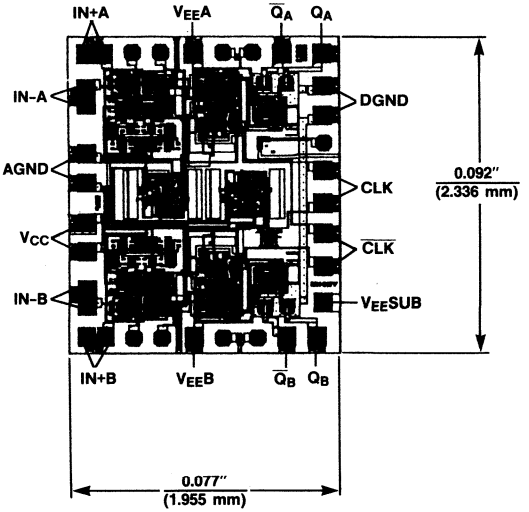
High-Speed, Positive Edge-Triggered, ECL-Compatible Voltage Comparators

Chip Topographies

MAX905



MAX906



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

High-Speed, Ultra-Low Power, Single +5V, Dual TTL Comparator

General Description

The MAX907 is a dual, high-speed, micropower comparator designed for single +5V supply systems. A 30ns propagation delay (at 5mV input overdrive) is achieved with a low power consumption of only 3.5mW per comparator. The wide input common-mode range extends from ground to within 1.5V from the positive supply rail.

The MAX907 outputs are TTL compatible and require no external pull-up circuitry. All inputs and outputs can be indefinitely shorted to either supply rail without damage. Internal hysteresis in the MAX907 ensures clean output switching, even when the device is driven by a slow-moving input signal.

The MAX907, available in both 8-pin DIP and narrow SO packages, is the ideal comparator for all applications requiring high speed and precision together with low power dissipation.

For similar high-speed, micropower applications that require four comparators, contact the factory for availability of the MAX908 quad.

Applications

Battery-Powered Systems

High-Speed A/D Converters

High-Speed V/F Converters

Line Receivers

Threshold Detectors/Discriminators

High-Speed Sampling Circuits

Zero-Crossing Detectors

Features

- ♦ **30ns Propagation Delay**
- ♦ **3.5mW Per Comparator Power Consumption**
- ♦ **+5V Single-Supply Operation**
- ♦ **Input Range Includes Ground**
- ♦ **2mV Internal Hysteresis Provides Clean Switching**
- ♦ **TTL-Compatible Outputs**
- ♦ **Input and Output Short-Circuit Protection**

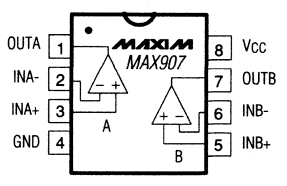
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX907CPA	0°C to +70°C	8 Plastic DIP
MAX907CSA	0°C to +70°C	8 SO
MAX907C/D	0°C to +70°C	Dice*
MAX907EPA	-40°C to +85°C	8 Plastic DIP
MAX907ESA	-40°C to +85°C	8 SO
MAX907MJA	-55°C to +125°C	8 CERDIP

** Dice are specified at +25°C, DC parameters only.*

Pin Configuration

TOP VIEW



DIP/SO

High-Speed, Ultra-Low Power, Single +5V, Dual TTL Comparator

ABSOLUTE MAXIMUM RATINGS

Power-Supply Voltage (V_{CC} to GND) ..... +7V
Differential Input Voltage ..... -0.3V to (V_{CC} + 0.3V)
Common-Mode Input Voltage ..... -0.3V to (V_{CC} + 0.3V)
Input/Output Short-Circuit Duration:
To V_{CC} ..... Indefinite
To GND ..... Indefinite
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX907C_ _ ..... 0°C to +70°C
MAX907E_ _ ..... -40°C to +85°C
MAX907MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)			1	3	mV
Input-Referred Hysteresis	V_{HYST}	(Note 2)			±2		mV
Input Bias Current	I_B	V_{CM} = 0V, V_O = 1.4V			100	300	nA
Input Offset Current	I_{OS}	V_{CM} = 0V, V_O = 1.4V			25	50	nA
Input Voltage Range	V_{CM}	(Note 3)		-0.2		V_{CC} - 1.5	V
Common-Mode Rejection Ratio	CMRR	(Note 4)			50	100	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 5)			50	100	µV/V
Output High Voltage	V_{OH}	V_{IN} = 100mV, I_{SOURCE} = 100µA		2.6	3.0		V
Output Low Voltage	V_{OL}	V_{IN} = 100mV	I_{SINK} = 2mA		0.3	0.4	V
			I_{SINK} = 4mA		0.4	0.6	
Supply Current (Per Comparator)	I_{CC}	V_{CC} = 5.5V			0.7	1.0	mA
Power Dissipation (Per Comparator)	P_{DISS}	(Note 6)			3.5	5.5	mW
Input to Output High Response Time	t_{pd+}	V_{IN} = 100mV, V_{OD} = 5mV (Note 7)			30	50	ns
Input to Output Low Response Time	t_{pd-}	V_{IN} = 100mV, V_{OD} = 5mV (Note 7)			30	50	ns

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Offset Voltage	V_{OS}	(Note 1)			1.5	5	mV
Input-Referred Hysteresis	V_{HYST}	(Note 2)			±2		mV
Input Bias Current	I_B	V_{CM} = 0V, V_O = 1.4V			200	500	nA
Input Offset Current	I_{OS}	V_{CM} = 0V, V_O = 1.4V			50	100	nA
Input Voltage Range	V_{CM}	(Note 3)		-0.2		V_{CC} - 1.5	V
Common-Mode Rejection Ratio	CMRR	(Note 4)			75	250	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 5)			75	250	µV/V
Output High Voltage	V_{OH}	V_{IN} = 100mV, I_{SOURCE} = 100µA		2.6	3.0		V
Output Low Voltage	V_{OL}	V_{IN} = 100mV	I_{SINK} = 2mA		0.3	0.4	V
			I_{SINK} = 4mA		0.4	0.6	
Supply Current (Per Comparator)	I_{CC}	V_{CC} = 5.5V			1.0	1.5	mA
Power Dissipation (Per Comparator)	P_{DISS}	(Note 6)			5	9	mW
Input to Output High Response Time	t_{pd+}	V_{IN} = 100mV, V_{OD} = 5mV (Note 7)			40	70	ns
Input to Output Low Response Time	t_{pd-}	V_{IN} = 100mV, V_{OD} = 5mV (Note 7)			40	70	ns

Note 1: In the MAX907, V_{OS} is defined as the center of the zone of input-referred hysteresis (V_{HYST}). V_{OS} is specified for V_{CM} = 0V and V_{OUT} = +1.4V (TTL threshold).

Note 2: Input-referred hysteresis zone (V_{HYST}) is defined as the difference between the upper and lower input voltage trip points required to make the output change states.

Note 3: Inferred from the CMRR test. A correct logic result is obtained at the output if at least ONE input is within the CMR limits. Either one or both inputs can be driven to a maximum of any voltage between -0.3V to (V_{CC} + 0.3V) without damage.

Note 4: Tested with V_{CC} = +5.5V and for -0.2V < V_{CM} < V_{CC} - 1.5V.

Note 5: Tested for +4.5V < V_{CC} < 5.5V (full tolerance of operating supply voltage).

Note 6: Typical power dissipation specified with V_{CC} = +5V, maximum with V_{CC} = +5.5V.

Note 7: Due to difficulties in measuring t_{pd} with 5mV of overdrive in automatic test equipment, the MAX907 is sample tested with 100mV of input overdrive. Correlation tests show that the specification can be guaranteed, if all other DC parameters are within the specified limits. V_{OS} must be added to the overdrive voltage for low values of overdrive. See *Typical Operating Characteristics*.

19-3967; Rev 0; 6/92

MAXIM

High-Speed, Threshold-Programmable Voltage Comparators

General Description

The MAX910/MAX911 are the first high-speed comparators to include an 8-bit DAC with voltage reference to set the input threshold voltage. The MAX910 has a TTL compatible output while the MAX911 output is fully differential and ECL compatible. Comparator propagation delay is 8ns for the MAX910 and only 4ns for the MAX911. For high-speed comparator applications where the threshold must be updated rapidly, such as automatic test equipment (ATE) or process control applications, the MAX910/MAX911 provide a complete, single IC solution which significantly reduces stray capacitance, board space, design time and cost over multi-chip, discrete solutions.

The comparator threshold level, set by the DAC, has 10mV or 20mV pin-selectable resolution (a full-scale range of either 2.56V or 5.12V) when used with the internal reference. An external reference input is also provided.

The MAX910/MAX911 feature separate power and comparator ground pins to eliminate coupling between the comparator output and analog input. Both parts can be powered from either ±5V, or +5V and -5.2V supplies.

Applications

Analog-to-Digital Converters

Voltage-to-Frequency Converters

Threshold Detectors

Window Discriminators

Sampling

Automatic Test Equipment

Features

- **8ns Propagation Delay, TTL-Compatible Output (MAX910)**
- **4ns Propagation Delay, ECL-Compatible Output (MAX911)**
- **200mW Power Dissipation**
- **8-Bit Digitally Programmable Threshold Level**
- **Internal +2.56V Voltage Reference**
- **2.56V or 5.12V Full-Scale Range**
- **Separate Analog and Digital Supplies**
- **Comparator Output Latch Function**

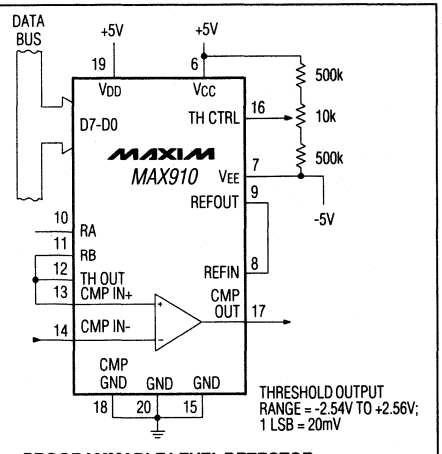
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX910CAG	0°C to +70°C	24 SSOP**
MAX910CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX910CWG	0°C to +70°C	24 Wide SO
MAX910C/D	0°C to +70°C	Dice*
MAX910EAG	-40°C to +85°C	24 SSOP**
MAX910ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX910EWG	-40°C to +85°C	24 Wide SO

** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for pricing and availability*

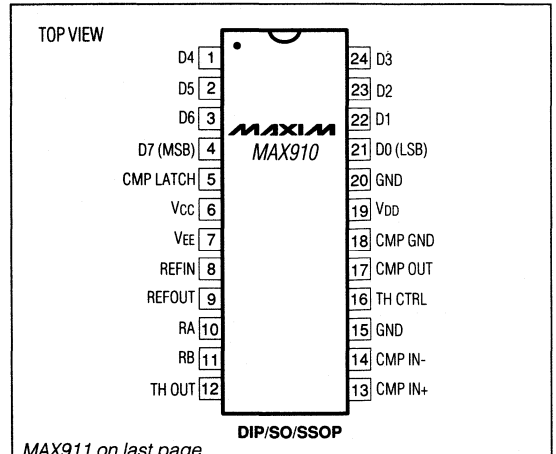
3

Typical Operating Circuit



PROGRAMMABLE LEVEL DETECTOR

Pin Configurations



DIP/SO/SSOP

MAX911 on last page

High-Speed, Threshold-Programmable Voltage Comparators

ABSOLUTE MAXIMUM RATINGS (Note 1)

Analog Supply Voltage (V_{CC} to V_{EE}) ..... +12V
Digital Supply Voltage (V_{DD} to GND) ..... +6V
V_{EE} to GND ..... -6V
CMP GND to GND ..... ±1V
CMP IN+ to CMP IN- ..... [V_{EE} - 0.2V] to [V_{CC} + 0.2V]
TH CTRL ..... [V_{EE} - 0.2V] to [V_{CC} + 0.2V]
D0-D7 ..... -0.2V to [V_{DD} + 0.2V]
REFIN ..... [V_{EE} - 0.2V] to [V_{CC} + 0.2V]
CMP OUT Short-Circuit Duration (MAX910 only)
  to GND ..... Indefinite
  to V_{CC} ..... 1 minute
Q and $\overline{Q}$ Continuous Output Current (MAX911 only) 50mA
REFOUT Short-Circuit Duration
  to GND ..... 1 minute
  to V_{CC} ..... Indefinite
TH OUT Short-Circuit Duration
  to V_{EE} ..... 1 minute
  to V_{CC} or GND ..... Indefinite
REFIN Short-Circuit Duration
  to V_{EE} ..... 1 minute
  to V_{CC} or GND ..... Indefinite
Continuous Power Dissipation (T_A = +70°C)
  Plastic DIP (derate 8.70mW/°C above +70°C) 696mW
  SO (derate 11.76mW/°C above +70°C) 941mW
  SSOP (derate 8.00mW/°C above +70°C) 600mW
Operating Temperature Ranges:
  MAX91_C_ _ ..... 0°C to +70°C
  MAX91_E_ _ ..... -40°C to +85°C
Junction Temperature (T_j) ..... -65°C to +160°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Absolute maximum ratings apply to both packaged parts and dice, unless otherwise noted.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATOR							
Input Offset Voltage	V_{OS}	V_{CM} = 0V (Note 2)			1.0	3.0	mV
Input Bias Current	I_B	I_{IN+} or I_{IN-}			3	6	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			100	400	nA
Wideband Input Voltage Noise	e_n				300		µV
Input Common-Mode Voltage Range	V_{CM}	(Note 3)		-3		3	V
Common-Mode Rejection Ratio	CMRR	-3V < V_{CM} < 3V			50	150	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 4)			100	250	µV/V
Output High Voltage	V_{OH}	MAX910	V_{IN} > 250mV, I_{SOURCE} = 1mA	2.4	3.5		V
		MAX911	V_{IN} > 250mV, R_L = 50Ω to -2V	-0.96		-0.81	
Output Low Voltage	V_{OL}	MAX910	V_{IN} > 250mV, I_{SINK} = 8mA		0.3	0.4	V
		MAX911	V_{IN} > 250mV, R_L = 50Ω to -2V	-1.85		-1.65	
CMP LATCH Input Voltage High	V_{LH}				1.4	2.0	V
CMP LATCH Input Voltage Low	V_{LL}			0.8	1.4		V
CMP LATCH Input Current High	I_{LH}	V_{LH} = 3.0V			1	20	µA
CMP LATCH Input Current Low	I_{LL}	V_{LL} = 0.3V			1	20	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input to Output High Response Time	t_{pd+}	MAX910 (Notes 5, 6)		8	10	ns
		MAX911 (Notes 6, 7)		4	6	
Input to Output Low Response Time	t_{pd-}	MAX910 (Notes 5, 6)		8	10	ns
		MAX911 (Notes 6, 7)		4	6	
Latch Disable to Output High Delay	$t_{pd+(D)}$	MAX910		5		ns
		MAX911		1		
Latch Disable to Output Low Delay	$t_{pd-(D)}$	MAX910		5		ns
		MAX911		1		
Latch Setup Time	t_S	MAX910		2.0		ns
		MAX911		0.5		
Latch Hold Time	t_h	MAX910		1.0		ns
		MAX911		0.5		
Latch-Disable Pulse Width	$t_{pw(D)}$	MAX910		5		ns
		MAX911		1		
VOLTAGE REFERENCE						
Reference Voltage Output	VREF	(Note 8)	2.55	2.56	2.57	V
D0-D7						
TTL Input Voltage High	V_{IH}			1.4	2.0	V
TTL Input Voltage Low	V_{IL}		0.8	1.4		V
TTL Input Current High	I_{IH}	V_{IH} = 3.0V		1	20	µA
TTL Input Current Low	I_{IL}	V_{IL} = 0.3V		1	20	µA
THRESHOLD VOLTAGE OUTPUT						
Threshold Voltage Range	V_{TH}	REFIN = 2.56V, TH OUT connected to RB		+2.56 to -2.54		V
		REFIN = 2.56V, TH OUT connected to RA		+2.56 to +0.01		
Threshold Resolution	$V_{TH(R)}$	TH OUT connected to RB		20		mV
		TH OUT connected to RA		10		
Upper Threshold Limit Absolute Error	$V_{TH+(E)}$	(Note 9)		±1	±3	mV
Lower Threshold Limit Absolute Error	$V_{TH-(E)}$	(Notes 10, 11)		±10	±30	mV
Wideband Threshold Voltage Noise	$V_{TH(en)}$			800		µV

High-Speed, Threshold-Programmable Voltage Comparators

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Threshold Voltage Differential Nonlinearity	$V_{TH(DNL)}$	(Notes 10, 12)			±10	mV
Threshold Trim Range	$V_{TH(TR)}$	(Note 13)			±100	mV
Threshold Settling Time	t_S (V_{TH})	To 1/2LSB (Note 14)		50	75	ns
POWER REQUIREMENTS						
Positive Analog Supply Current	I_{CC}	(Note 4)		22	30	mA
Negative Analog Supply Current	I_{EE}	(Note 4)		16	25	mA
Digital Supply Current	I_{DD}	MAX910 only; V_{DD} = 5.5V		2	5	mA
Power Dissipation	PD			200	320	mW

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
COMPARATOR							
Input Offset Voltage	V_{OS}	V_{CM} = 0V (Note 2)			2.0	5.0	mV
Input Bias Current	I_B	I_{IN+} or I_{IN-}			4	8	µA
Input Offset Current	I_{OS}	V_{CM} = 0V			150	600	nA
Input Common-Mode Voltage Range	V_{CM}	(Note 3)		-3		3	V
Common-Mode Rejection Ratio	CMRR	-3V < V_{CM} < +3V			75	250	µV/V
Power-Supply Rejection Ratio	PSRR	(Note 4)			150	400	µV/V
Output High Voltage	V_{OH}	MAX910, V_{IN} > 250mV, I_{SOURCE} = 1mA		2.4	3.5		V
		MAX911, V_{IN} > 250mV, R_L = 50Ω to -2V	-40°C	-1.080		-0.905	
			0°C	-1.010		-0.850	
			+70°C	-0.900		-0.720	
			+85°C	-0.890		-0.700	
Output Low Voltage	V_{OL}	MAX910, V_{IN} > 250mV, I_{SINK} = 8mA			0.3	0.4	V
		MAX911, V_{IN} > 250mV, R_L = 50Ω to -2V	-40°C	-1.895		-1.680	
			0°C	-1.870		-1.660	
			+70°C	-1.830		-1.620	
			+85°C	-1.825		-1.615	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, V_{EE} = -5V, V_{DD} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CMP Latch Input Voltage High	V_{LH}				1.4	2.0	V
CMP Latch Input Voltage Low	V_{LL}			0.8	1.4		V
CMP Latch Input Current High	I_{LH}	V_{LH} = 3.0V			1	20	µA
CMP Latch Input Current Low	I_{LL}	V_{LL} = 0.3V			1	20	µA
Input to Output High Response Time	t_{pd+}	MAX910 (Notes 5, 6)			10	15	ns
		MAX911 (Notes 6, 7)			5	8	
Input to Output Low Response Time	t_{pd-}	MAX910 (Notes 5, 6)			10	15	ns
		MAX911 (Notes 6, 7)			5	8	
VOLTAGE REFERENCE							
Reference Voltage Output	VREF(E)	(Note 8)		2.54	2.56	2.58	V
Reference Voltage Tempco	TC VREF				0.2		mV/°C
D0-D7							
TTL Input Voltage High	V_{IH}				1.4	2.0	V
TTL Input Voltage Low	V_{IL}			0.8	1.4		V
TTL Input Current High	I_{IH}	V_{IN} = 3.0V			1	20	µA
TTL Input Current Low	I_{IL}	V_{IL} = 0.3V			1	20	µA
THRESHOLD VOLTAGE OUTPUT							
Upper Threshold Limit Absolute Error	$V_{TH+(E)}$	(Note 9)				±5	mV
Lower Threshold Limit Absolute Error	$V_{TH-(E)}$	(Notes 10, 11)	0°C to +70°C			±30	mV
			-40°C to +85°C			±40	
Threshold Limit Tempco (Note 10)	TCV_{TH}	Positive threshold limit			0.2		mV/°C
		Negative threshold limit			0.2		
Threshold Voltage Differential Nonlinearity	$V_{TH(DNL)}$	(Notes 10, 12)				±15	mV
POWER REQUIREMENTS							
Positive Analog Supply Current	I_{CC}	(Note 4)			22	30	mA
Negative Analog Supply Current	I_{EE}	(Note 4)			16	25	mA
Digital Supply Current	I_{DD}	MAX910 only V_{DD} = 5.5V			2	5	mA
Power Dissipation	PD				200	320	mW

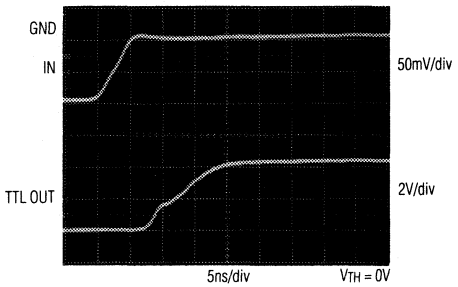
Note 2: Specifications are quoted with CMP OUT = +1.4V (TTL threshold) for the MAX910 and Q OUT, $\overline{Q}$ OUT = -1.3V (ECL threshold) for the MAX911.
Note 3: Inferred from the CMRR test.
Note 4: Tested for +4.75V ≤ V_{CC} ≤ +5.25V, and -5.5V ≤ V_{EE} ≤ +4.75V with V_{DD} = +5V.
Note 5: Conditions for MAX910 switching specifications are 100mV step input with 5mV of overdrive, 15pF of output load capacitance, and 2mA external pull-up load current.
Note 6: Parameter is guaranteed by design.
Note 7: Conditions for MAX911 switching specifications are 100mV step input with 5mV of overdrive, and with both outputs terminated to -2V through 50Ω load resistors
Note 8: VREF specified while supplying internal DAC current (i.e. REFOUT tied to REFIN).
Note 9: Specified with 2.56V applied to REFIN. Specification denotes maximum V_{TH+} deviation from 2.56V.
Note 10: Specified in a 5.10V FS system (i.e. with TH OUT terminated through internal 640Ω span resistor, 2.56V applied to REFIN, and with TH CTRL to GND).
Note 11: V_{TH-} limit quoted as a deviation from the nominal value of -2.54V with conditions specified in Note 10.
Note 12: Tested for each major carry transition of the input digital code.
Note 13: $V_{TH(TR)}$ specified for lower threshold voltage limit (i.e. with data-bits D0-D7 at logic low). A ±50mV change at TH CTRL causes a ±100mV change in V_{TH} -.
Note 14: Guaranteed by design. Specifications are taken from measurements made with a high-speed test fixture, C_{LOAD} = 2pF on TH OUT for both MAX to MIN and MIN to MAX threshold voltage transition and settling to within 10mV (1/2LSB) of the final voltage.

High-Speed, Threshold-Programmable Voltage Comparators

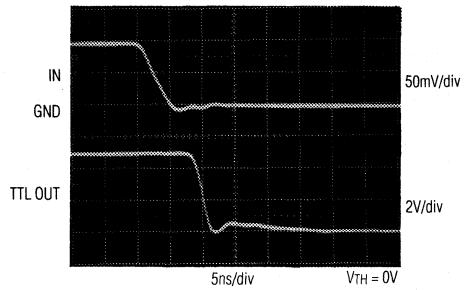
Typical Operating Characteristics

(TA = +25°C, unless otherwise noted.)

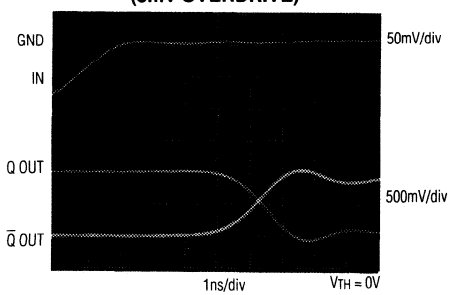
MAX910 t_{pd+} RESPONSE (5mV OVERDRIVE)



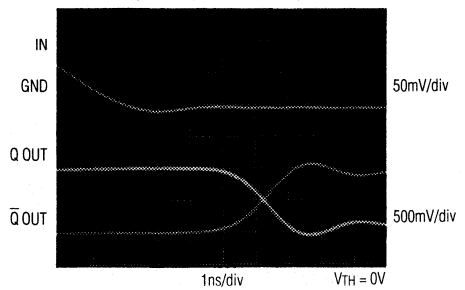
MAX910 t_{pd-} RESPONSE (5mV OVERDRIVE)



MAX911 t_{pd+} RESPONSE (5mV OVERDRIVE)



MAX911 t_{pd-} RESPONSE (5mV OVERDRIVE)

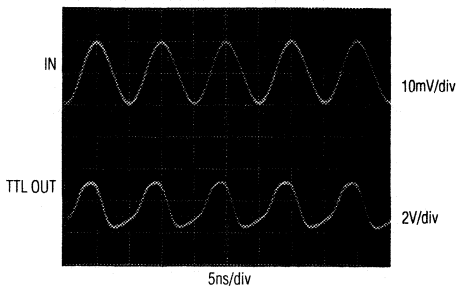


High-Speed, Threshold-Programmable Voltage Comparators

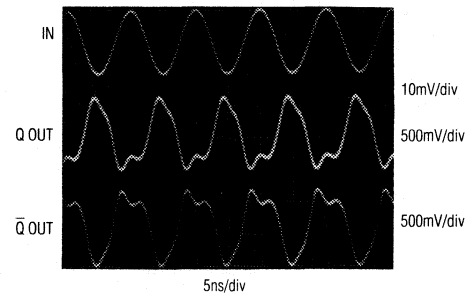
Typical Operating Characteristics (continued)

(TA = +25°C, unless otherwise noted.)

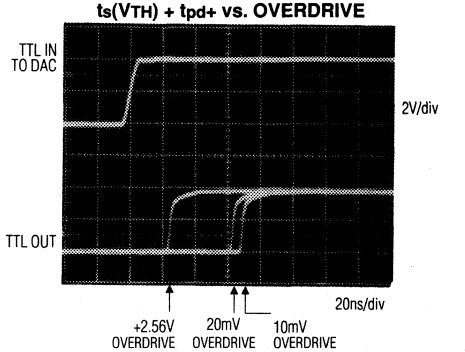
MAX910 100MHz COMPARATOR RESPONSE



MAX911 100MHz COMPARATOR RESPONSE

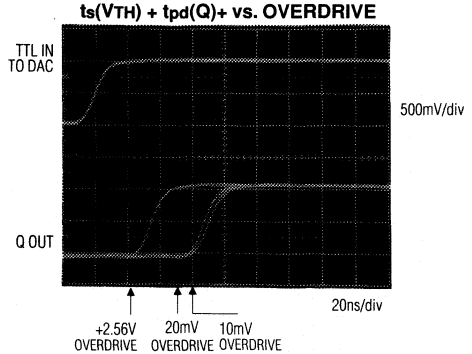


MAX910 ts(VTH) + tpd+ vs. OVERDRIVE



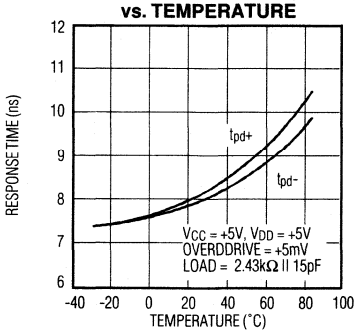
NOTE: CMP IN- CONNECTS TO GND AND TH OUT CONNECTS TO CMP IN+. THE DAC IS UPDATED, CAUSING TH OUT TO OVERDRIVE THE COMPARATOR INPUT.

MAX911 ts(VTH) + tpd(Q)+ vs. OVERDRIVE

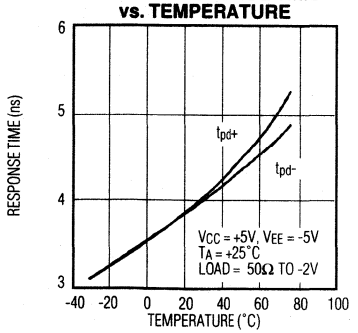


NOTE: CMP IN- CONNECTS TO GND AND TH OUT CONNECTS TO CMP IN+. THE DAC IS UPDATED, CAUSING TH OUT TO OVERDRIVE THE COMPARATOR INPUT.

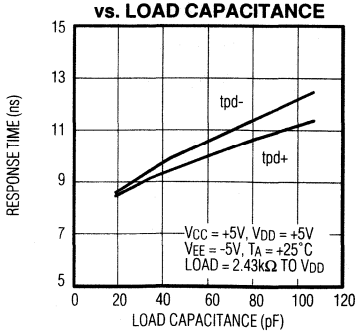
MAX910 RESPONSE TIME vs. TEMPERATURE



MAX911 RESPONSE TIME vs. TEMPERATURE



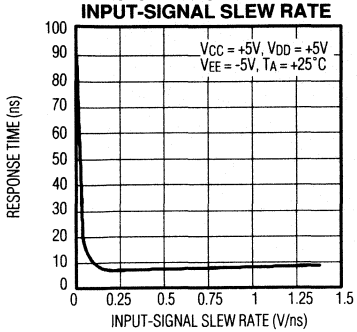
MAX910 RESPONSE TIME vs. LOAD CAPACITANCE



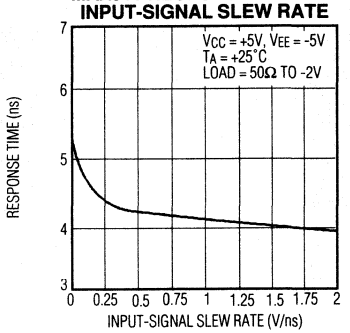
High-Speed, Threshold-Programmable Voltage Comparators

Typical Operating Characteristics (continued)

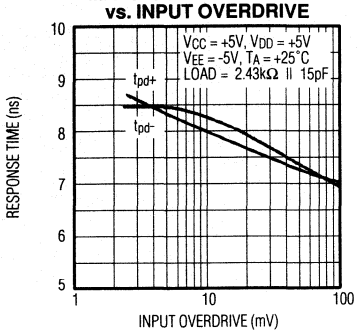
MAX910 RESPONSE TIME vs. INPUT-SIGNAL SLEW RATE



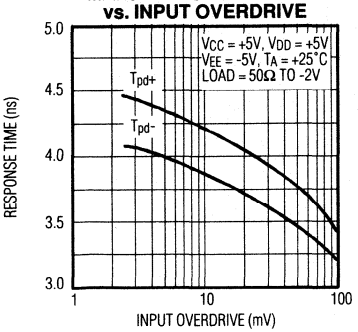
MAX911 RESPONSE TIME vs. INPUT-SIGNAL SLEW RATE



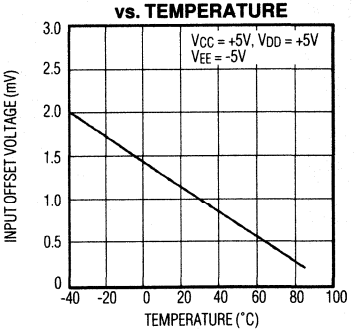
MAX910 RESPONSE TIME vs. INPUT OVERDRIVE



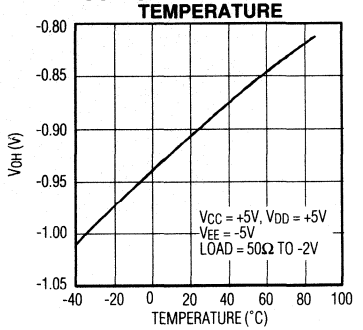
MAX911 RESPONSE TIME vs. INPUT OVERDRIVE



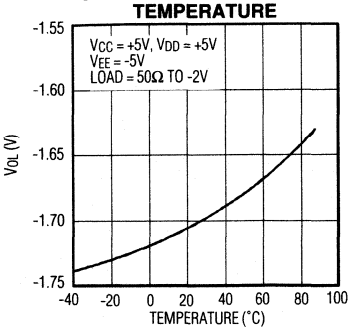
INPUT OFFSET VOLTAGE vs. TEMPERATURE



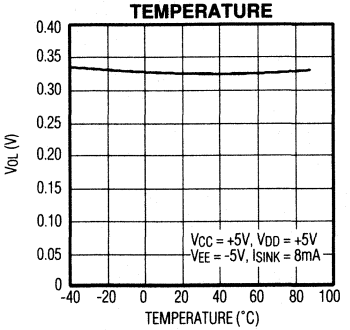
MAX911 OUTPUT HIGH VOLTAGE vs. TEMPERATURE



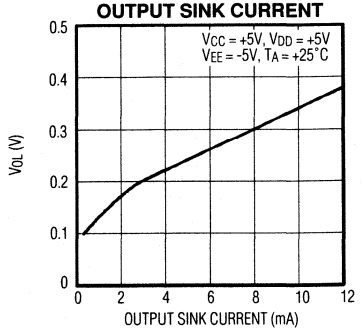
MAX911 OUTPUT LOW VOLTAGE vs. TEMPERATURE



MAX910 OUTPUT LOW VOLTAGE vs. TEMPERATURE

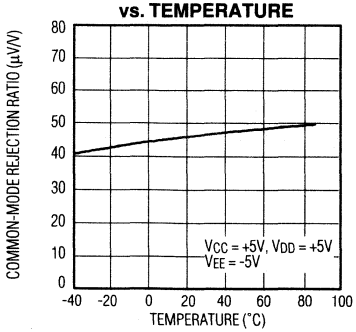


MAX910 OUTPUT LOW VOLTAGE vs. OUTPUT SINK CURRENT

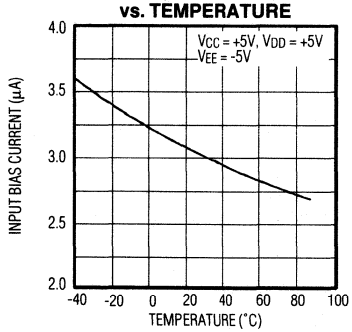


Typical Operating Characteristics (continued)

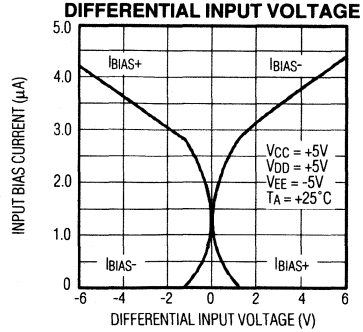
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



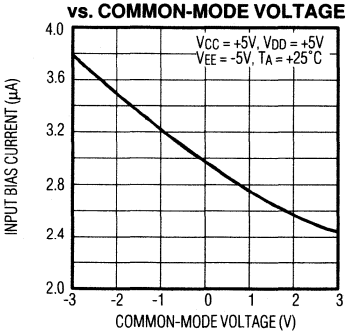
INPUT BIAS CURRENT vs. TEMPERATURE



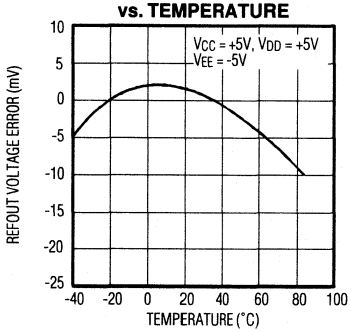
INPUT BIAS CURRENT vs. DIFFERENTIAL INPUT VOLTAGE



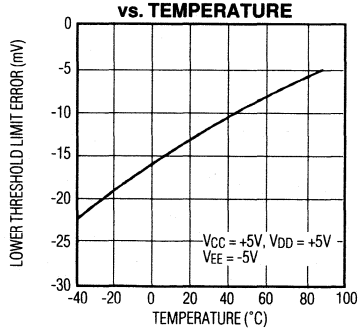
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



REFOUT VOLTAGE ERROR vs. TEMPERATURE



LOWER THRESHOLD LIMIT ERROR vs. TEMPERATURE



High-Speed, Threshold-Programmable Voltage Comparators

Pin Description

MAX910	MAX911	NAME	FUNCTION
1-4, 21-24	1-4 21-24	D4-D7, D0-D3	8-Bit DAC TTL Logic Inputs
5	5	CMP LATCH	Comparator Latch Input. A TTL logic low latches the comparator output. The comparator remains transparent to input changes when driven high or left floating.
6	6	V_{CC}	Analog Positive Supply. Connect to +5V analog supply.
7	7	V_{EE}	Analog Negative Supply. Connect to -5V or -5.2V analog supply.
8	8	REFIN	Reference Input. Connect to REFOUT or External Reference.
9	9	REFOUT	+2.56V Reference Output. Connect to REFIN for V_{TH+} = +2.56V.
10	10	RA	320Ω Span Resistor. Connect to TH OUT for 2.55V threshold range and 10mV resolution.
11	11	RB	640Ω Span Resistor. Connect to TH OUT for 5.1V range with 20mV resolution.
12	12	TH OUT	Threshold Output Voltage. Connect to span resistors RA or RB, and to either comparator input.
13	13	CMP IN+	Comparator Noninverting Input
14	14	CMP IN-	Comparator Inverting Input
15, 20	15, 20	GND	Analog power supply ground; separated from comparator's digital output ground (CMP GND).
16	16	TH CTRL	Reference Trim Input to the 8-bit DAC. Connect to the wiper of a 10kΩ trimming potentiometer between 500kΩ stop resistors for lower threshold output voltage (V_{TH-}) trimming (Figure 1).
17		CMP OUT	TTL Comparator Output
	17	Q OUT	ECL Comparator Output
18	18	CMP GND	Comparator Ground. Connect to digital ground.
19		V_{DD}	Positive Digital Supply. Connect to +5V digital supply.
	19	$\overline{Q}$ OUT	Complementary ECL Comparator Output

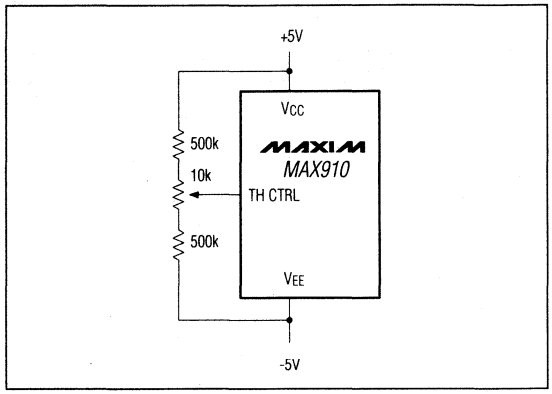


Figure 1. The lower limit of TH OUT is trimmed up to ±50mV, by connecting a 10kΩ trim pot between 500kΩ stop resistors across V_{CC} and V_{EE} with the trim pot wiper to TH CTRL.

Detailed Description

The MAX910 and MAX911 voltage comparators differ in logic compatibility. The MAX910 has a TTL compatible output, while the MAX911 output is fully differential and ECL compatible (Figures 2 and 3). Both comparators have an 8-bit, multiplying-current DAC, internal +2.56V reference, and two span resistors.

The Comparator

The comparator input common-mode range is specified between ±3V to accommodate a wide range of threshold voltages, although either comparator input can be driven to the V_{CC} or V_{EE} power-supply rails without damage. A TTL compatible latch-enable function (CMP LATCH) is supplied on both the MAX910 and MAX911. The comparator is transparent to changes at the input terminals as long as CMP LATCH is driven high or left floating. As soon as CMP LATCH is taken low, the comparator output latches. The output remains latched until CMP LATCH is again driven high or allowed to float.

The MAX910 TTL comparator, with a propagation delay of 8ns and a fan-out of four, drives low-power Schottky TTL gates and 15pF of parasitic board capacitance without significant speed degradation. The MAX911 has 4ns propagation delay, and comparator output specifications that are directly compatible with the MECL 10k series. For best performance, terminate the differential ECL outputs of the MAX911 with 50Ω pull-down resistors to a -2V supply. Both the MAX910 and MAX911 respond to 100MHz signals.

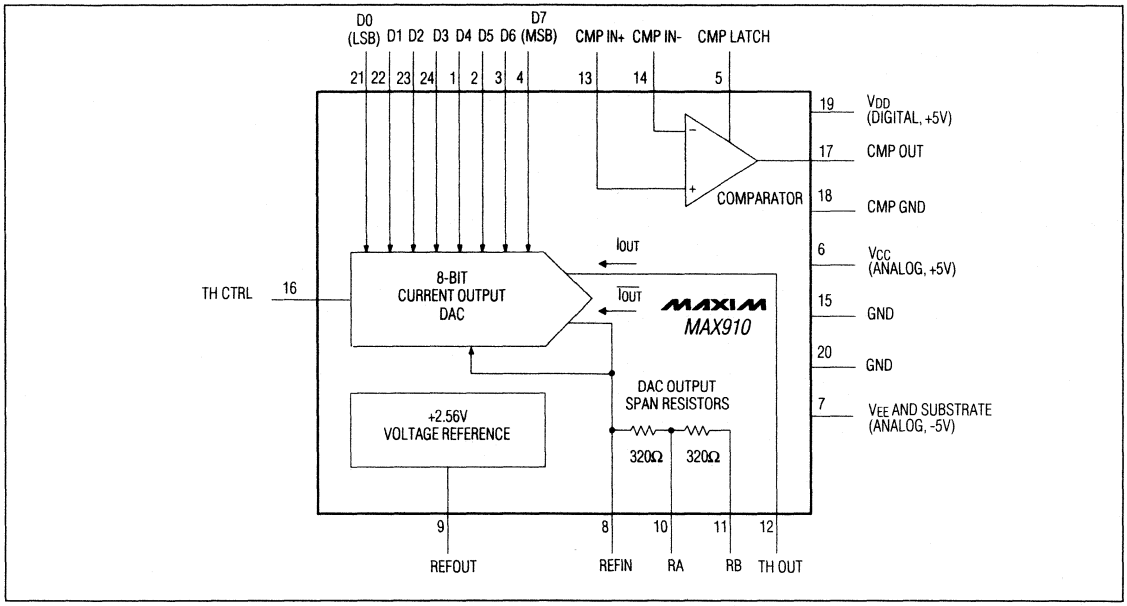


Figure 2. MAX910 Functional Diagram

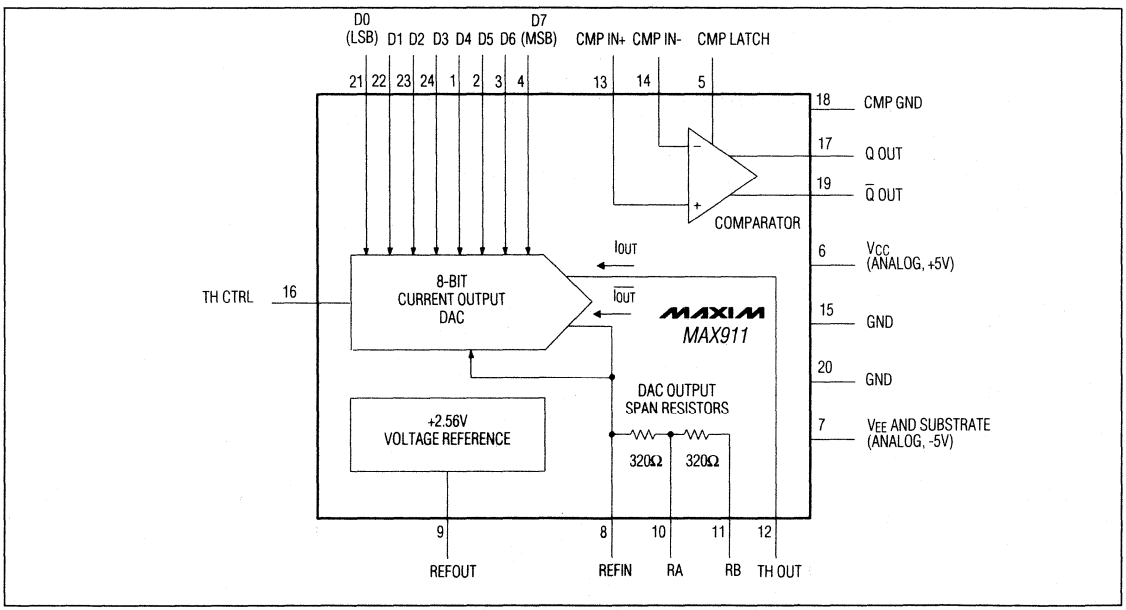


Figure 3. MAX911 Functional Diagram

High-Speed, Threshold-Programmable Voltage Comparators

Threshold Out (TH OUT)

The complementary outputs of the internal 8-bit DAC sink a full-scale output current of 8mA, which translates to either a 2.56V or a 5.12V range, depending on which span resistor input (RA or RB) connects to TH OUT. The digital code divides the output current between the I_{OUT} and $\overline{I_{OUT}}$ DAC outputs (Figures 2 and 3). With the digital input code set to all 0s, TH OUT sinks the full-scale current (less 1LSB) from I_{OUT}, and $\overline{I_{OUT}}$ sinks no current. When the input code is set to all 1s, the reverse is true: REFIN sinks the full-scale output current from $\overline{I_{OUT}}$, and TH OUT sinks no current. Intermediate input codes divide the output current between the two DAC outputs accordingly.

The DAC output current flowing through the DAC output span resistor RA or RB develops the voltage available on TH OUT. Span resistor choice determines the full-scale voltage range and resolution of TH OUT (Table 1). Note that the full-scale output current always flows into REFIN (Pin 8) regardless of the input code. This minimizes glitching on REFIN as the threshold voltage is updated.

Updating the TTL input digital code D0-D7 changes the voltage available on TH OUT.

REFIN must be terminated in a suitable voltage source. Accomplish this by connecting REFIN to REFOUT, or to an external voltage reference. The voltage termination determines the upper end of the threshold range (V_{TH+}). Table 1 lists the range and resolution of TH OUT for different pin connections in Figure 4.

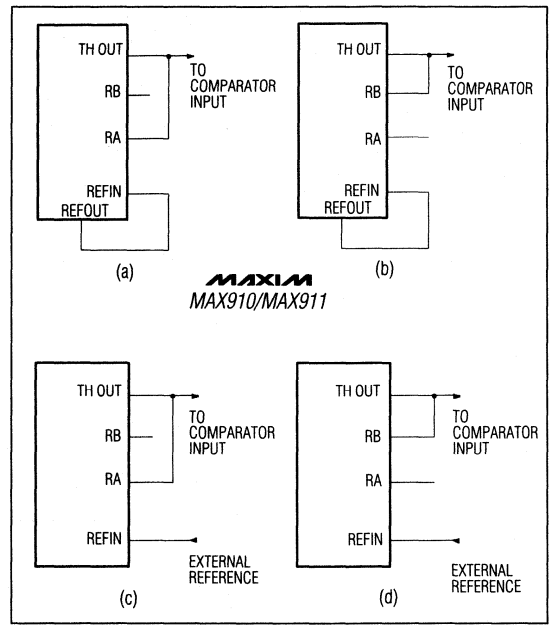


Figure 4. Configuration for the TH OUT Voltage Ranges and Resolutions Listed in Table 1

Using an External Reference

For applications requiring higher precision, connect an external reference to REFIN. The voltage applied at REFIN sets V_{TH-} and V_{TH+}. V_{TH-} and V_{TH+} must not exceed the comparator common-mode input range, and must source at least 10mA.

Choose the external reference and span resistors such that V_{TH-} is at least 2V above V_{EE}. V_{TH-} is determined by REFIN, TH CTRL, and R_{SPAN} (RA, RB):

$$V_{TH-} = V_{REFIN} - \left[\left[\frac{255}{256} \times \frac{R_{SPAN}}{320\Omega} \right] \times [V_{REFIN} - V_{TH\ CTRL}] \right]$$

Where R_{SPAN} = 320Ω when TH OUT is connected to RA;

= 640Ω when TH OUT is connected to RB.

For example, selecting R_{SPAN} = 320Ω and delivering +3V to REFIN yields a 0V to +3V threshold range. TH OUT connects to either comparator input.

Table 1. TH OUT Voltage Range and Resolution

CONNECT REFIN TO:	SPAN RESISTOR (Ω)	V_{TH+}(V)	V_{TH-}(V)	RESOLUTION	PIN CONNECTION
REFOUT (+2.56V)	RA (320)	+2.56	0.01	1LSB = 10mV	Figure 4a
REFOUT (+2.56V)	RB (640)	+2.56	-2.54	1LSB = 20mV	Figure 4b
V_{EXTREF}	RA (320)	V_{EXTREF}	V_{EXTREF} x (1/256)	1LSB = V_{EXTREF}/256	Figure 4c
V_{EXTREF}	RB (640)	V_{EXTREF}	-V_{EXTREF} x (254/256)	1LSB = 2 x V_{EXTREF}/256	Figure 4d

Note: V_{EXTREF} = External Reference Voltage

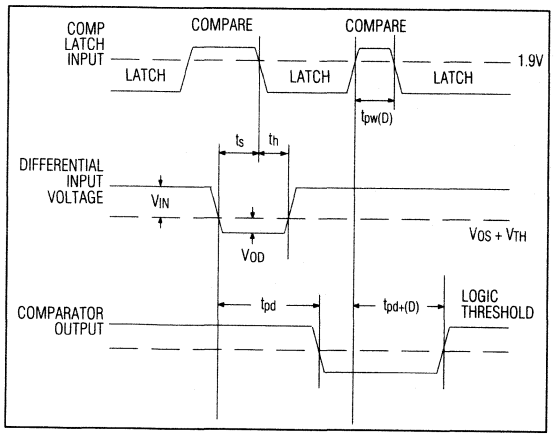


Figure 5. Comparator Timing Diagram

Definition of Terms

V_{OS} **Input Offset Voltage:** That voltage which must be applied between the two comparator input terminals to obtain TTL logic threshold (+1.4V) at the comparator output for the MAX910, or ECL logic threshold (-1.3V) at the comparator output for the MAX911.

V_{IN} **Input Voltage Pulse Amplitude;** usually set to 100mV for comparator specifications.

V_{OD} **Input Voltage Overdrive;** usually set to 5mV and in opposite polarity to V_{IN} for comparator specifications.

t_{pd+} **Input to Output High Delay:** The propagation delay measured from the time the input signal crosses the input offset voltage to the logic threshold of an output low-to-high transition.

t_{pd-} **Input to Output Low Delay:** The propagation delay measured from the time the input signal crosses the input offset voltage to the logic threshold of an output high-to-low transition.

$t_{pd+(D)}$ **Latch Disable to Output High Delay:** The propagation delay measured from the comparator latch signal crossing the TTL threshold in a low-to-high transition, to the point of the output crossing the logic threshold in a low-to-high transition.

$t_{pd-(D)}$ **Latch Disable to Output Low Delay:** The propagation delay measured from the comparator latch signal crossing the TTL threshold in a low-to-high transition, to the point of the output crossing the logic threshold in a high-to-low transition.

t_s **Setup Time:** The time before the comparator latch signal's negative transition that an input must be present to be acquired and held at the output.

t_h **Hold Time:** The time an input signal must remain unchanged after the negative transition of the comparator latch signal in order to be acquired and held at the output.

$t_{pw(D)}$ **Latch-Disable Pulse Width:** The time the comparator latch signal must remain high in order to acquire and hold an input signal change.

$t_{s(VTH)}$ **Threshold Settling Time:** The time required for the threshold voltage to be changed from V_{TH-} to V_{TH+} or from V_{TH+} to V_{TH-} and settle to within ±1/2LSB of V_{TH+} or V_{TH-}.

High-Speed, Threshold-Programmable Voltage Comparators

Applications Information

Board Layout

A printed circuit board with a good, low inductance ground plane is mandatory. Connect analog GND to the ground plane as close to the device as possible. The comparator ground (CMP GND) must be connected to the digital ground plane or bus. Connect the two grounds together at the power supply. Place all decoupling capacitors (small 100nF ceramic type are a good choice) as close as possible to the device power-supply pins. The power return side should be short and straight to the ground plane. Separate positive supplies for analog (V_{CC}) and digital (V_{DD}) are also recommended. Choose decoupling and terminating components with suitable bandwidths.

To avoid unwanted parasitic feedback, keep the comparator input and output trace and lead lengths short. Separate the digital lines driving D0-D7 as far from the analog lines as possible. Solder the device directly to the printed circuit board rather than using a socket to minimize stray capacitance.

Minimize parasitic capacitance between TH OUT, RA, RB, and CMP IN by keeping the connections short. Parasitic capacitance on this node degrades threshold voltage settling time.

Typical Application Circuits

Adding Hysteresis to the MAX910

For applications requiring fast response to slow-moving inputs, add hysteresis by connecting a resistor from CMP OUT to TH OUT (Figure 6).

$$\text{Hysteresis} = \frac{V_{OH} - V_{OL}}{1 + \frac{R_{FB}}{R_{SPAN}}}$$

where V_{OH} = Comparator Output Threshold High

V_{OL} = Comparator Output Threshold Low

R_{FB} = Feedback Resistor

R_{SPAN} = 320Ω with TH OUT connected to RA

= 640Ω with TH OUT connected to RB

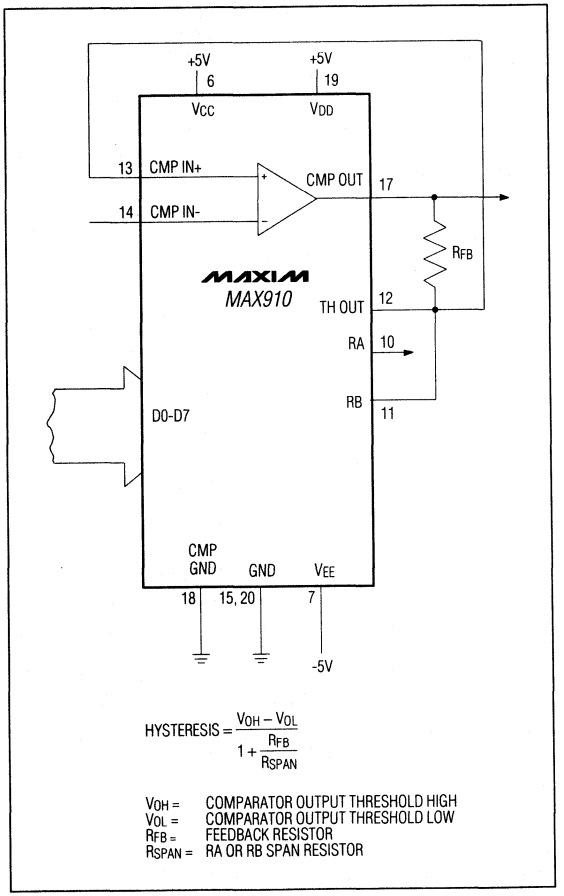


Figure 6. Adding Hysteresis to the MAX910

Window Comparator Circuit

Two MAX911s detect the upper and lower threshold limits of a logic output from a device under test (DUT) in an automatic test equipment application (Figure 7). One device is programmed for the upper threshold limit while the other detects the lower limit. Either the MAX910 or MAX911 may be used in this application depending on the propagation delay and output compatibility requirements.

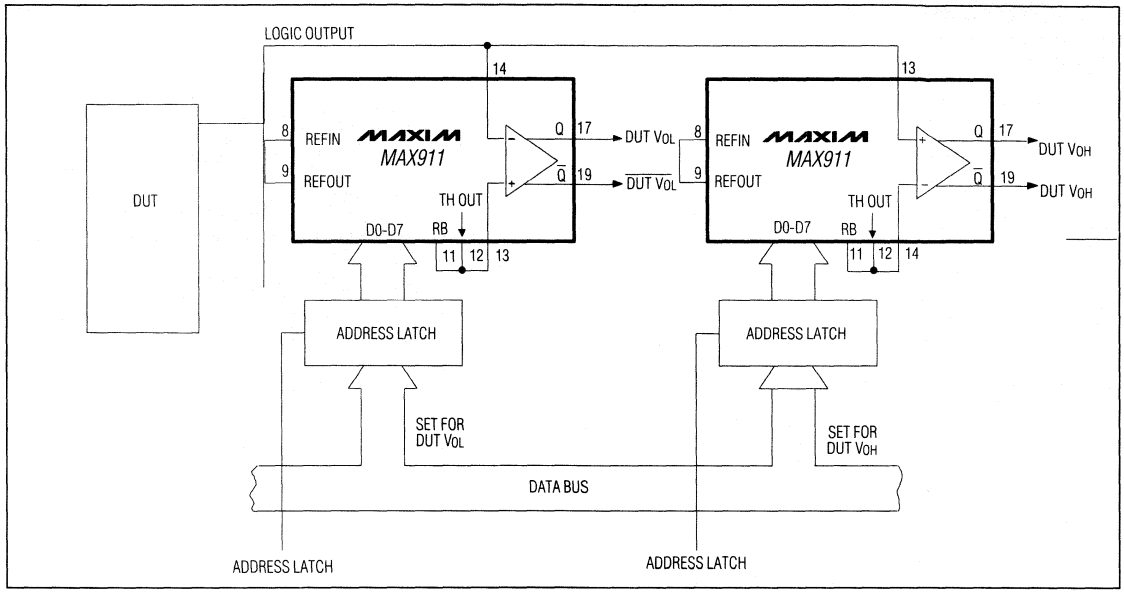
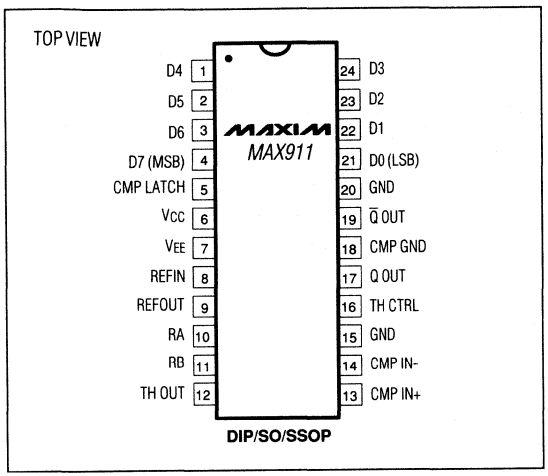


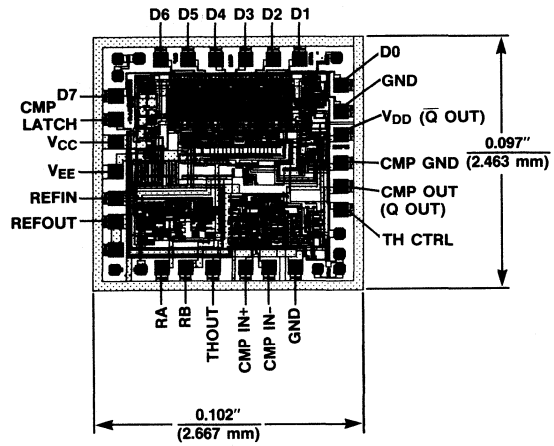
Figure 7. Automatic Test Equipment Logic Threshold Detector

High-Speed, Threshold-Programmable Voltage Comparators

Pin Configurations (continued)



Chip Topography



( ) ARE FOR MAX911 ONLY.
SUBSTRATE CONNECTED TO V_{EE}.

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX911CAG	0°C to +70°C	24 SSOP**
MAX911CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX911CWG	0°C to +70°C	24 Wide SO
MAX911C/D	0°C to +70°C	Dice*
MAX911EAG	-40°C to +85°C	24 SSOP**
MAX911ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX911EWG	-40°C to +85°C	24 Wide SO

** Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for pricing and availability*

MAXIM

Power-Supply Circuits

* Advance Information – first page of data sheet in preparation.

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA) max (typ)	Package Options*	Temp. Range**	Features	Price† 1000-up ($)
STEP-UP SWITCHING REGULATORS (PFM)							
MAX4193	2.4 to 16.5	$V_{OUT} > V_{IN}$	0.200 (0.090)	DIP, SO	C, E, M	Improved RC4193 2nd source	1.74
MAX630	2.0 to 16.5	$V_{OUT} > V_{IN}$	0.125 (0.070)	DIP, SO	C, E, M	Improved RC4193 2nd source	2.88
MAX631	1.5 to 5.6	+5, adj.	0.4 (0.135)	DIP, SO	C, E, M	Only 2 external components	2.56
MAX632	1.5 to 12.6	+12, adj.	2.0 (0.5)	DIP, SO	C, E, M	Only 2 external components	2.56
MAX633	1.5 to 15.6	+15, adj.	2.5 (0.75)	DIP, SO	C, E, M	Only 2 external components	2.56
MAX654	1.15 to 5.6	+5	(0.08)	DIP, SO	C, E, M	Optimized for 1 cell, evaluation kit available	3.35
MAX655	1.5 to 5.6	+5	(0.04)	DIP, SO	C, E, M	Optimized for 2 cells, evaluation kit available	3.35
MAX656	1.15 to 5.6	+5	(0.08)	DIP, SO	C, E, M	Drives external MOSFET	3.35
MAX657	1.15 to 3.6	+3	(0.08)	DIP, SO	C, E, M	Optimized for 1 cell, evaluation kit available	3.35
MAX658	1.5 to 5.6	+5	(0.04)	DIP, SO	C, E, M	Drives external MOSFET	3.35
STEP-UP SWITCHING REGULATORS (PWM)							
MAX731	1.8 to 5.25	+5	4 (2)	DIP, SO	C, E, M	Evaluation kit available	3.20
MAX732	4.0 to 9.0	+12	3 (1.7)	DIP, SO	C, E, M	Internal power MOSFET, ±4% output voltage tolerance, flash EEPROM programming power supply, 200mA output	2.66
MAX733	4.0 to 12.0	+15	3 (1.7)	DIP, SO	C, E, M	125mA output, evaluation kit available	3.23
MAX734	4.0 to 9.3	+12	3 (1.7)	DIP, SO	C, E, M	Flash-memory programer evaluation kit available	††
MAX751	1.8 to 5.25	+5	4 (2)	DIP, SO	C, E, M	Evaluation kit available	††
MAX752	1.8 to 16	Adj.	3 (1.7)	DIP, SO	C, E, M	Evaluation kit available	3.20
STEP-DOWN SWITCHING REGULATORS (PFM)							
MAX638	2.6 to 16.5	+5, adj.	0.6 (0.135)	DIP, SO	C, E, M	Only 3 external components	2.56
MAX639	4.0 to 11.0	+5, adj.	0.2 (0.1)	DIP, SO	C, E, M	>90% efficiencies over wide range (2mA to 225mA), DIP and SO evaluation kit available	2.96
STEP-DOWN SWITCHING REGULATORS (PWM)							
MAX730	5.2 to 11.0	+5	3 (1.7)	DIP, SO	C, E, M	300mA output, 90% efficiencies, DIP and SO evaluation kit available	3.09
MAX738	6.0 to 16.0	+5	3 (1.7)	DIP, SO	C, E, M	750mA output, >85% efficiencies, DIP and SO evaluation kit available	3.23
MAX750	4.0 to 11.0	Adj.	3 (1.7)	DIP, SO	C, E, M	1.5W output, 90% efficiencies, DIP and SO evaluation kit available	2.92
MAX758	4.0 to 16	Adj.	3 (1.7)	DIP, SO	C, E, M	3.75W output, >85% efficiencies, DIP and SO evaluation kit available	3.23

–Continued on the next page–

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, TO-99 = Can
** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product - contact factory for pricing and availability.

Part Number	Input Voltage Range (V)	Output Voltage (V)	Quiescent Supply Current (mA) max (typ)	Package Options*	Temp. Range**	Features	Price† 1000-up ($)
INVERTING SWITCHING REGULATORS (PFM)							
MAX4391	4.0 to 16.5	up to -20	0.25 (0.09)	DIP, SO	C, E, M	Improved RC4391 2nd source	2.09
MAX634	2.3 to 16.5	up to -20	0.15 (0.07)	DIP, SO	C, E, M	Improved RC4391 2nd source	2.61
MAX635	2.3 to 16.5	-5, adj.	0.15 (0.08)	DIP, SO	C, E, M	Only 3 external components	2.56
MAX636	2.3 to 16.5	-12, adj.	0.15 (0.08)	DIP, SO	C, E, M	Only 3 external components	2.56
MAX637	2.3 to 16.5	-15, adj.	10 (0.5)	DIP, SO	C, E, M	Only 3 external components	2.56
MAX650	-54 to -42	+5	0.15 (0.07)	DIP, SO	C, E, M	Telecom applications	3.50
INVERTING SWITCHING REGULATORS (PWM)							
MAX735	4.0 to 6.2	-5	3 (1.6)	DIP, SO	C, E, M	200mA output, 85% efficiencies	2.55
MAX736	4.0 to 8.6	-12	6 (4.2)	DIP, SO	C, E, M	>80% efficiencies, evaluation kit available	2.95
MAX737	4.0 to 5.5	-15	9 (6.1)	DIP, SO	C, E, M	>80% efficiencies, evaluation kit available	2.95
MAX739	4.0 to 16.0	-5	1.7 (3.5)	DIP, SO	C, E, M	300mA output, 80% efficiencies	2.95
MAX755	4.0 to 11.0	Adj.	3 (1.6)	DIP, SO	C, E, M	>80% efficiencies	††
MAX759	4.0 to 11.0	Adj.	2.2 (4.0)	DIP, SO	C, E, M	1.5W output, LCD driver, 80% efficiencies	2.95
DUAL OUTPUT SWITCHING REGULATORS (PWM)							
MAX742	4.2 to 10.0	±12, ±15	15 (8)	DIP, SO	C, E, M	Drives external MOSFETs, 30W output	3.91
MAX743	4.2 to 6.0	±12, ±15	30 (20)	DIP, SO	C, E, M	Internal power MOSFETs, evaluation kit and production kit available, 3W output	4.49
SWITCHING REGULATOR CONTROLLERS							
MAX641	1.5 to 5.6	+5, adj.	0.4 (0.135)	DIP, SO	C, E, M	PFM controller	2.87
MAX642	1.5 to 12.6	+12, adj.	2.0 (0.5)	DIP, SO	C, E, M	PFM controller	2.87
MAX643	1.5 to 15.6	+15, adj.	2.5 (0.75)	DIP, SO	C, E, M	PFM controller	2.87
MAX741U	2.7 to 15.5	+5, +12, +15, adj.	3.5 (1.6)	DIP, SO, SSOP	C, E, M	PWM step-up controller	††
MAX741D	2.7 to 15.5	+5 adj.	4.0 (2.8)	DIP, SO, SSOP	C, E, M	PWM step-down controller	††
MAX741N	2.7 to 15.5	-5, -12, -15, adj.	4.0 (2.2)	DIP, SO, SSOP	C, E, M	PWM inverting controller	††
CHARGE-PUMP CONVERTERS—UNREGULATED							
MAX660	1.5 to 5.5	+2 x V_{IN}, -V_{IN}	1.0 (0.6)	DIP, SO	C, E, M	I_{OUT} = 100mA	2.95
MAX680	2.0 to 6.0	± 2 x V_{IN}	2 (1)	DIP, SO	C, E, M		1.62
MAX681	2.0 to 6.0	± 2 x V_{IN}	2 (1)	DIP	C, E	No external components (internal caps)	4.64
ICL7660	1.5 to 10	-V_{IN}	0.175 (0.110)	DIP, SO, TO-99	C, E, M		1.09
ICL7662	4.5 to 20	-V_{IN}	0.6 (0.25)	DIP, SO, TO-99	C		1.76
Si7661	4.5 to 20	-V_{IN}	2 (0.3)	DIP, SO, TO-99	C		1.94
CHARGE-PUMP CONVERTERS—REGULATED HIGH-SIDE POWER SUPPLIES							
MAX622	3.5 to 16.5	V_{IN} + 11V	0.5 (0.07)	DIP, SO	C, E	3 external capacitors	1.99
MAX623	3.5 to 16.5	V_{IN} + 11V	0.5 (0.07)	DIP	C, E	No external capacitors	3.95

* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, TO-99 = Can
** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product - contact factory for pricing and availability.

Power Management Supplies

Part Number	Input Voltage Range (V)	Linear Output Voltage (V)	DC-DC Output Voltages (V)	Quiescent Supply Current Temp. Max Range (mA)	Features	Price† 1000-up ($)
MAX714	5.05 to 11	2 at +5V lines	-5 to -26 adj. LCD driver	0.2 per C, E, M enabled output line	Independent shutdowns, backup-battery switchover, RESET and power-fail warning outputs	6.80
MAX715	5.05 to 11	3 at +5V lines	-5 adj., -5 to -26 adj., +12 or +15 adj.	0.2 per C, E, M, enabled output line	PC layout and parts list available	9.32
MAX716	5.05 to 11	4 at +5V lines	-5 adj., -5 to -26 adj., +12 or +15 adj.	0.2 per C, E, M, enabled output line	Independent shutdowns, backup-battery switchover, RESET and power-fail warning outputs, evaluation kit available	9.54

MOSFET Drivers

Part Number	Output Resistance (Ω) max (typ)	Rise/Fall T_A = +25°C (ns max)	Rise Time Over Temp. (ns max)	Fall Time Over Temp. (ns max)	Supply Voltage (V)	Package Options*	Temp. Range**	Features	Price† 1000-up ($)
MAX4426/7/8	10 (4)	30	40	40	4.5 to 18	DIP, SO	C, E, M	Dual inverting/dual noninverting/dual combo	1.61
MAX626/7/8	15 (4)	30	40	40	4.5 to 18	DIP, SO	C, E, M	Dual inverting/dual noninverting/dual combo	1.57
TSC426/7/8	15 (10)	30	60	40	4.5 to 18	DIP, SO	C, E, M	Dual inverting/dual noninverting/dual combo	1.06
ICL7667	12 (8)	30	40	40	4.5 to 15	DIP, SO, TO -99	C, E, M	Dual inverting	1.12

High-Side MOSFET Drivers

Part Number	Supply Voltage Range (V)	Quiescent Supply Current (mA) max (typ)	Switching Frequency (kHz)	Package Options*	Temp. Range**	Features	Price† 1000-up ($)
MAX620	4.5 to 16.5	0.5 (0.070)	70	DIP, SO	C, E	Quad high-side driver, V_{CC}+11V output	3.91
MAX621	4.5 to 16.5	0.5 (0.070)	70	DIP	C, E	Quad high-side driver, V_{CC}+11V output, internal capacitors	5.82
MAX625	4.5 to 16.5	0.5 (0.070)	70	DIP	C, E	Quad high-side switch, 4 internal 0.2Ω N-channel MOSFETs, internal capacitors	9.98

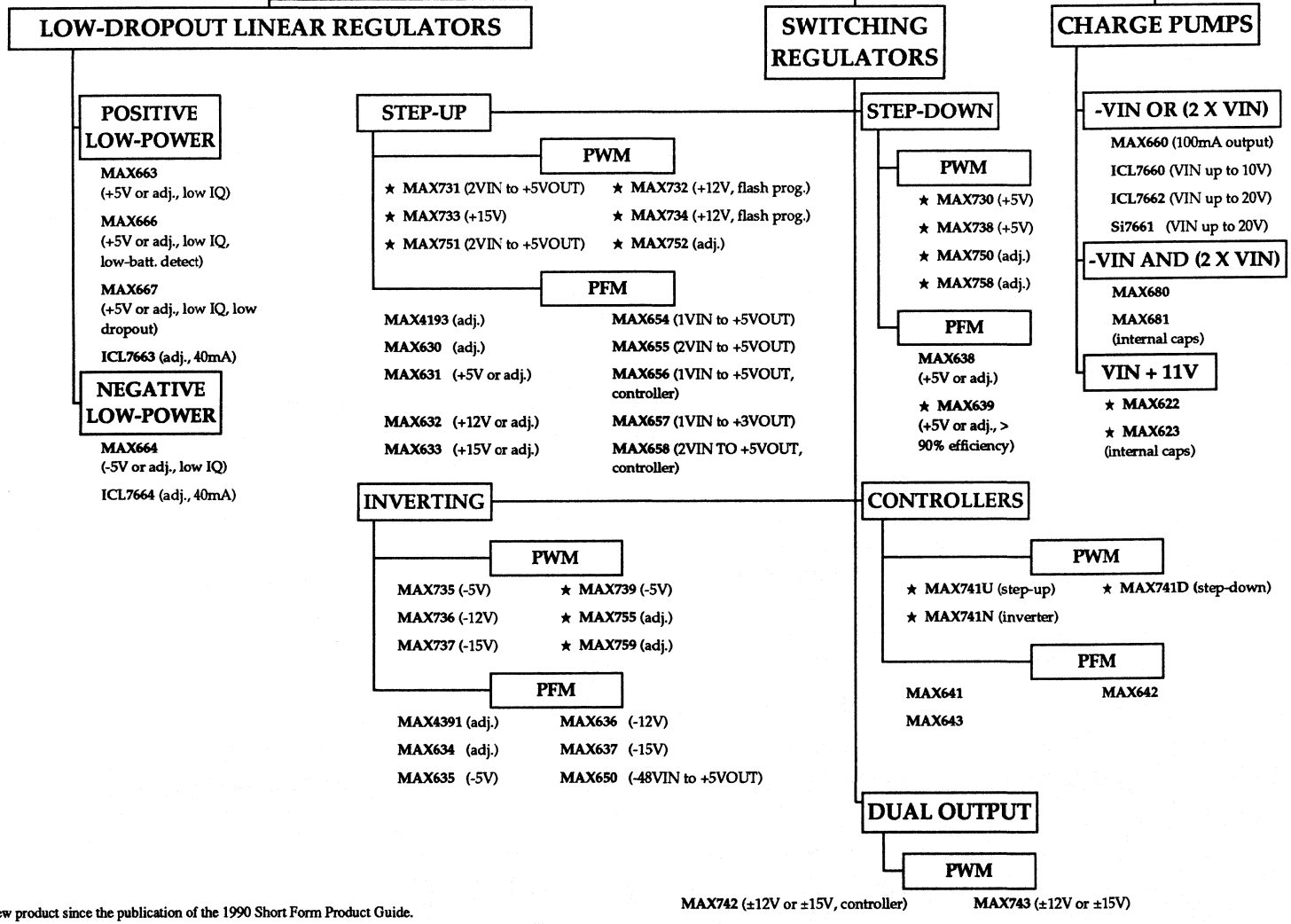
* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, TO-99 = Can
** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product - contact factory for pricing and availability.

Linear Voltage Regulators

Part Number	Input Voltage Range (V)	Output Voltage (V)	Dropout Voltage	Quiescent Current (µA) max (typ)	Output-Voltage Accuracy	Shutdown	Package Options*	Temp. Range**	Price† 1000-up ($)
AC-DC REGULATORS									
MAX610	110/240VAC	Fixed +5 or +1.3 to +9	N/A	150 (70)	±4%	No	DIP	C	2.58
MAX611	110/240VAC	Fixed +5	N/A	150 (70)	±4%	No	DIP	C	2.58
MAX612	110/220VAC	Fixed +5 or +1.3 to +9	N/A	150 (70)	±4%	No	DIP	C	2.58
DC LINEAR REGULATORS - POSITIVE OUTPUT									
MAX663	+2 to +16.5	Fixed +5 or +1.3 to +15	0.9V at 40mA	12 (6)	±5%	Yes	DIP, SO	C, E, M	1.91
MAX666	+2 to +16.5	Fixed +5 or +1.3 to +15	0.9V at 40mA	12 (6)	±5%	Yes	DIP, SO	C, E, M	2.22
MAX667	+3.5 to +16.5	Fixed +5 or +1.3 to +15	0.15V at 200mA	25 (12)	±5%	Yes	DIP, SO	C, E, M	2.35
ICL7663	+1.5 to +16	+1.3 to +15	0.9V at 40mA	10 (4)	±8%	Yes	DIP, SO, TO-99	C, E, I, M	1.81
ICL7663A	+2.0 to +16	+1.3 to +15	0.9V at 40mA	10 (4)	±1%	Yes	DIP, SO, TO-99	C, E, I, M	1.99
ICL7663B	+1.5 to +16	+1.3 to +15	0.9V at 40mA	10 (4)	±8%	Yes	DIP, SO, TO-99	C, E, I, M	1.81
DC LINEAR REGULATORS - NEGATIVE OUTPUT									
MAX664	-2 to -16.5	Fixed -5 or -1.3 to -15	0.5V at 40mA	12 (6)	±5%	Yes	DIP, SO	C, E, M	2.33
ICL7664	-2 to -16	-1.3 to -15	0.4V at 30mA	10 (3.5)	±5%	Yes	DIP, SO, TO-99	C, I, M	2.21
ICL7664A	-2 to -16	-1.3 to -15	0.4V at 30mA	10 (3.5)	±1%	Yes	DIP, SO, TO-99	C, I, M	2.65

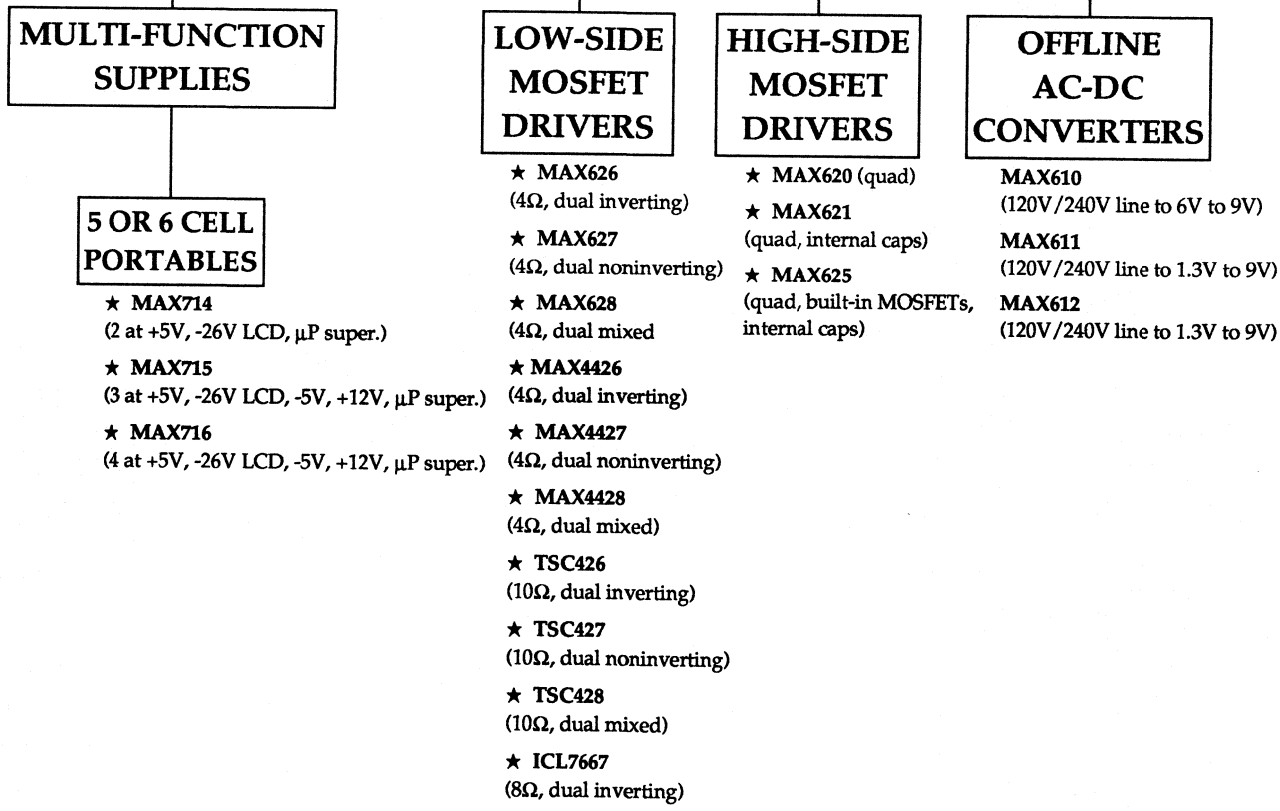
* Package Options: DIP = Dual-In-Line Package, SO = Small Outline, TO-99 = Can
** Temperature Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product - contact factory for pricing and availability.

DC-DC CONVERTERS



★ New product since the publication of the 1990 Short Form Product Guide.

POWER MANAGEMENT



★ New product since the publication of the 1990 Short Form Product Guide.

19-4454, Rev. 0; 8/91

MAXIM

Quad, High-Side Power Switch

General Description

The MAX625 is a quad, high-side power switch that switches 1A steady-state loads with 4A peak currents. The switch resistances are typically 0.2Ω, and internal clamp diodes allow inductive load switching. The MAX625 is completely self-contained in a 24-pin, 0.300" narrow plastic DIP package and requires no external components for normal operation.

The +4.5V to +16.5V input supply range and a typical quiescent current of only 70μA make the MAX625 ideal for a wide range of line- and battery-powered switching and control applications that require high efficiency and small size.

An internal quad latch accepts four TTL/CMOS logic signals that control the four switches. The MAX625 eliminates expensive logic MOSFETs in +5V-only and other low-voltage switching circuits. It also replaces costly, bulky, less efficient P-channel MOSFETs or PNP transistors.

Applications

Portable Computer Battery-Load Management
High-Side Power, N-Channel MOSFET Switching
Low-Side Switching from Low Supply Voltages
Solid-State Relay
Quad-Latching Level Translators
H-Bridge Motor Drivers
Stepper Motor Drivers

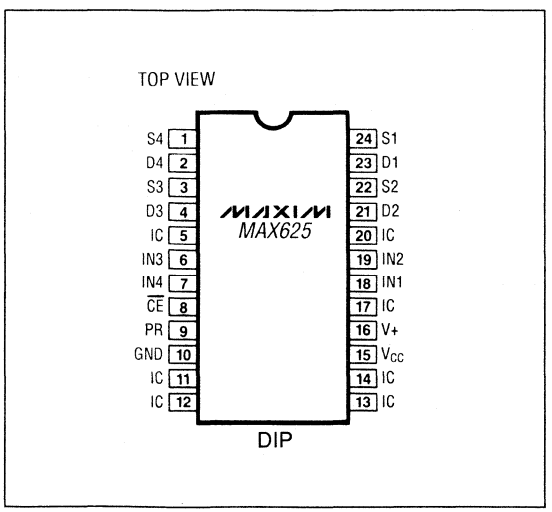
Features

- ♦ **0.2Ω Max Switch Resistance**
- ♦ **+4.5V to +16.5V Operating Supply Voltage Range**
- ♦ **Output Voltage Regulated to V_{CC} + 11V (Typ) Available at V+**
- ♦ **70μA Quiescent Current (Typ)**
- ♦ **Quad Latched TTL/CMOS Inputs**
- ♦ **Power-Ready Output**
- ♦ **Undervoltage Lockout**

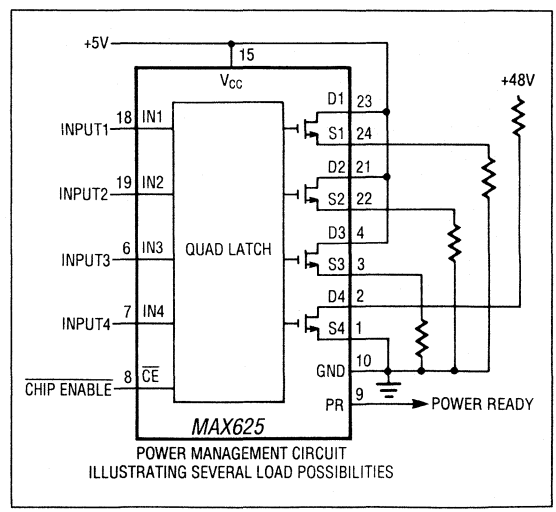
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX625CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX625ENG	-40°C to +85°C	24 Narrow Plastic DIP

Pin Configuration



Typical Operating Circuit



POWER MANAGEMENT CIRCUIT
ILLUSTRATING SEVERAL LOAD POSSIBILITIES

Quad, High-Side Power Switch

ABSOLUTE MAXIMUM RATINGS

V_{CC} 17V
V+ to GND 30V
IN1–IN4, $\overline{CE}$ ..... (GND – 0.3V) to (V+ + 0.3V)
Power Ready (PR) Output ... (GND – 0.3V) to (V_{CC} + 0.3V)
V+ Output Current 25mA
Drain-to-Source Breakdown Voltage 60V
Continuous Drain to Source Current
  Single MOSFET 5A
  All four MOSFETs 1.2A

Continuous Total Power Dissipation
  to +70°C 1067mW
  derate above +70°C ..... 13.33mW/°C
Operating Temperature Ranges:
  MAX625CNG ..... 0°C to +70°C
  MAX625ENG ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage (Note 1)	V_{CC}			4.5		16.5	V
Internal MOSFET ON Resistance (Note 2)	$R_{DS(ON)}$	T_A = +25°C V_{CC} = 4.5V to 16.5V (High-side)			150	200	mΩ
		T_A = +25°C V_{CC} = 4.5V to 8V (Low-side)			140	200	
		T_A = T_{MIN} to T_{MAX} V_{CC} = 4.5V to 16.5V (High-side)				260	
		T_A = T_{MIN} to T_{MAX} V_{CC} = 4.5V to 8V (Low-side)				260	
Off Leakage Current	$I_{DS(OFF)}$	V_{DS} = 55V			0.05	1.0	μA
High-Side Voltage (Note 3)	V+	I_{OUT} = 0, V_{CC} = +4.5V		14.5	15.5	17.5	V
		I_{OUT} = 0, V_{CC} = 16.5V		26.5	27.5	29.5	
		I_{OUT} = 250μA, V_{CC} = 5V		15	16	18	
		I_{OUT} = 500μA, V_{CC} = 16.5V		26.5	27.5	29.5	
Power-Ready Threshold	PRT	I_{OUT} = 0 (Note 4)		12	13.5	14.5	V
Power-Ready Output High	PR_{OH}	I_{SOURCE} = 100μA		3.8	4.7	5	V
Power-Ready Output Low	PR_{OL}	I_{SINK} = 1mA			0.1	0.4	V
Switching Frequency	f_O	I_{OUT} = 0, T_A = +25°C			70		kHz
Quiescent Supply Current	I_Q	T_A = +25°C, I_{OUT} = 0	V_{CC} = 16.5V		50	350	μA
			V_{CC} = 5V		70	500	

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V, T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic Inputs						
Input Threshold Low	V_{TL}				0.8	V
Input Threshold High	V_{TH}		2.4			V
Input Bias Current	I_B	0V < V_{IN} < 5V	-100		+100	nA
Chip Enable Threshold Low	CE_{LO}				0.8	V
Chip Enable Threshold High	CE_{HI}		2.4			V
Minimum $\overline{CE}$ Pulse Duration	t_{CE}		100	50		ns
Pull-Down Current	I_{CE}			10		µA
Data Hold Time	t_{DH}			-10	+10	ns
Data Set-Up Time	t_{SU}			50	100	ns
Data Delay Time	t_{OD}	V_{CE} = 0V		150		ns

Note 1: To avoid exceeding the maximum V_{GS} rating of the internal N-channel MOSFET switches, V_{CC} must not exceed +8V in low-side switching applications.

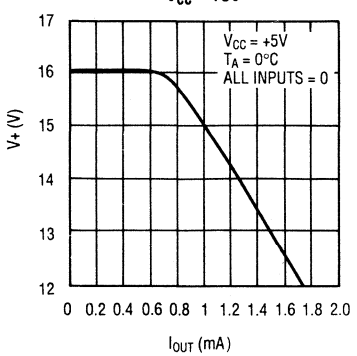
Note 2: A "low-side" switch connects between the load and ground.
A "high-side" switch connects between the voltage source and load.

Note 3: The High-Side Voltage (V+) is measured with respect to ground.

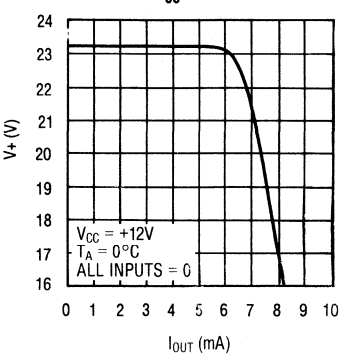
Note 4: Power Ready Threshold is the voltage measured with respect to ground at V+ when PR switches high (PR HIGH = V_{CC}).

Typical Operating Characteristics

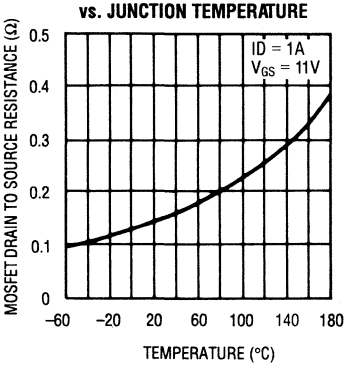
V+ vs. I_{OUT}
V_{CC} = +5V



V+ vs. I_{OUT}
V_{CC} = +12V



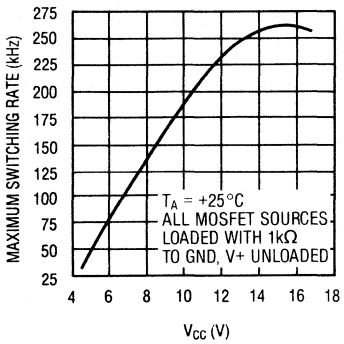
INTERNAL MOSFET DRAIN TO SOURCE RESISTANCE vs. JUNCTION TEMPERATURE



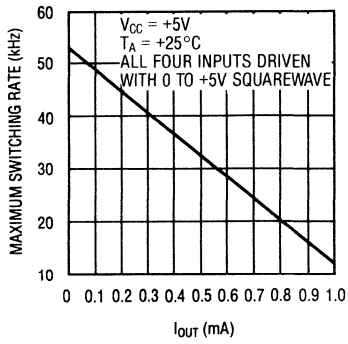
Quad, High-Side Power Switch

Typical Operating Characteristics (continued)

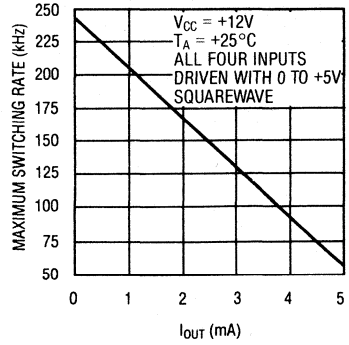
MAXIMUM SWITCHING RATE vs. V_{CC} SYNCHRONOUSLY DRIVING ALL FOUR INPUTS



MAXIMUM SWITCHING RATE vs. ADDITIONAL V+ LOAD CURRENT (I_{OUT}) VCC = +5V

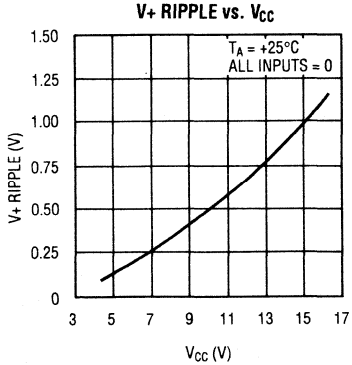


MAXIMUM SWITCHING RATE vs. ADDITIONAL V+ LOAD CURRENT (I_{OUT}) VCC = +12V

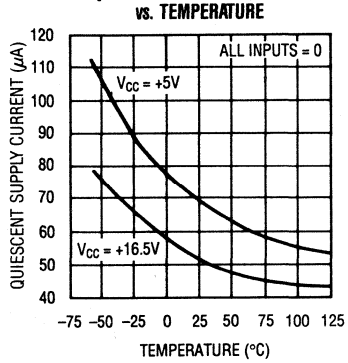


NOTE: THE MAXIMUM SWITCHING RATE OCCURS JUST BELOW THE POINT WHERE DRIVER OUTPUT AND V+ LOADING PULLS V+ TO PRT (PRT = V_{CC} + 8.5V).

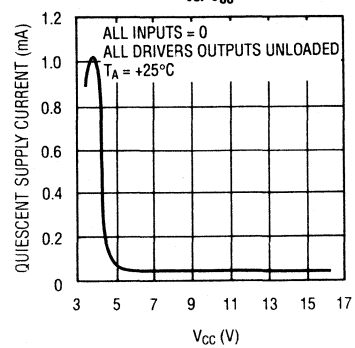
V+ RIPPLE vs. V_{CC}



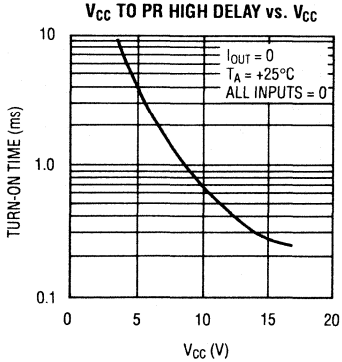
QUIESCENT SUPPLY CURRENT vs. TEMPERATURE



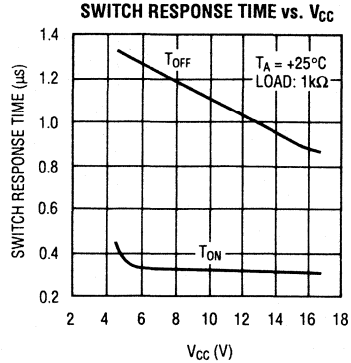
QUIESCENT SUPPLY CURRENT vs. V_{CC}



V_{CC} TO PR HIGH DELAY vs. V_{CC}



SWITCH RESPONSE TIME vs. V_{CC}



NOTE: MEASURED FROM THE DRIVER INPUT EDGE TO THE POINT WHERE THE SWITCH IS FULLY ON OR OFF

Pin Description

PIN	NAME	FUNCTION
1	S4	MOSFET Source 4.
2	D4	MOSFET Drain 4.
3	S3	MOSFET Source 3.
4	D3	MOSFET Drain 3.
5	IC	Internal Connection. Make no connection to this pin.
6	IN3	TTL/CMOS Compatible Input to Switch 3. Connect to GND if unused.
7	IN4	TTL/CMOS Compatible Input to Switch 4. Connect to GND if unused.
8	$\overline{CE}$	Chip Enable. Logic high inhibits input data. Logic low transfers data to switches. $\overline{CE}$ pulse must be at least 100ns. Connect to GND for direct data transfer.
9	PR	Power-Ready Output is a logic high equal to V_{CC} when $V+ \geq V_{CC} + 8.5V$.
10	GND	Ground.
11	IC	Internal Connection. Make no connection to this pin.
12	IC	Internal Connection. Make no connection to this pin.
13	IC	Internal Connection. Make no connection to this pin.
14	IC	Internal Connection. Make no connection to this pin.
15	V_{CC}	Supply Voltage. Connect to positive supply.
16	V+	High-side voltage out. Typically equal to V_{CC} + 11V.
17	IC	Internal Connection. Make no connection to this pin.
18	IN1	TTL/CMOS Compatible input to switch 1. Connect to GND if unused.
19	IN2	TTL/CMOS Compatible input to switch 2. Connect to GND if unused.
20	IC	Internal Connection. Make no connection to this pin.
21	D2	MOSFET Drain 2.
22	S2	MOSFET Source 2.
23	D1	MOSFET Drain 1.
24	S1	MOSFET Source 1.

Detailed Description

Figure 1 shows the MAX625 functional block diagram. A regulated multistage charge pump supplies four MOSFET drivers with V_{CC} + 11V for driving the internal MOSFETs (Figure 2). Logic inputs to the four drivers are stored in a quad latch. Data is latched by pulling $\overline{CE}$ high. An undervoltage lockout prevents the internal MOSFETs from turning on until V+ reaches the Power Ready Threshold (PRT) voltage (V_{CC} + 8.5V) and V_{CC} is greater than +3V.

The Dual-Charge Pump

A high-side voltage of approximately V_{CC} + 11V is generated by a multistage charge pump (Figure 2). Although the charge pump is capable of multiplying V_{CC} by up to four times, the output is regulated to V_{CC} + 11V by an internal feedback circuit. The charge pump typically operates at 70kHz, but regulates by pulse-skipping. When V+ exceeds V_{CC} + 11V, the charge pump shuts off. As V+ falls below V_{CC} + 11V, the charge pump turns on.

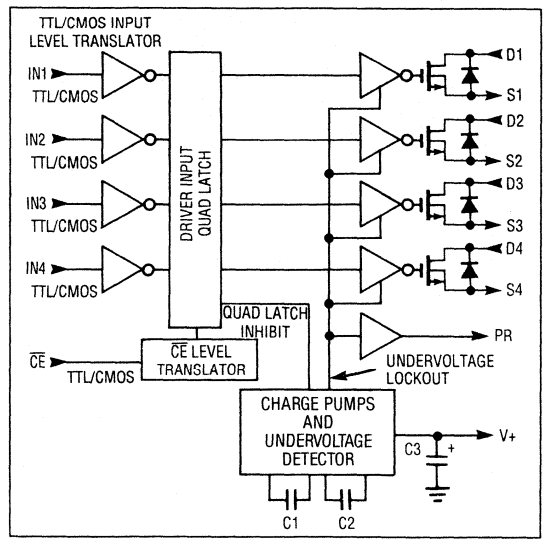


Figure 1. MAX625 Functional Diagram

Quad, High-Side Power Switch

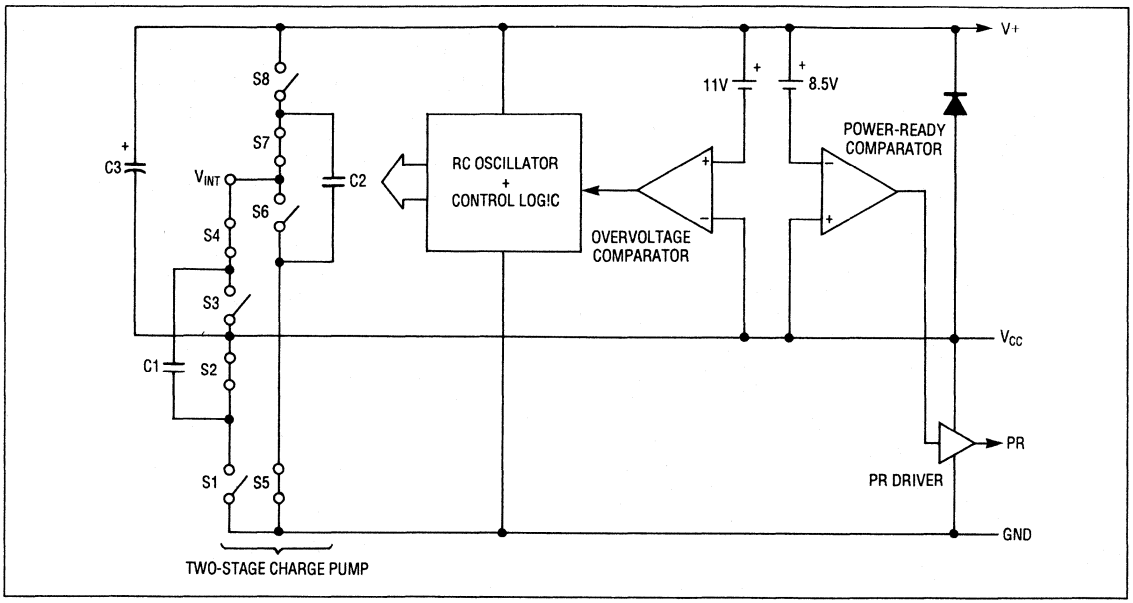


Figure 2. MAX625 Charge-Pump Diagram

MOSFET Drivers

Four MOSFET drivers level shift TTL/CMOS input signals, without an inversion, to levels that switch between ground and V_{CC} + 11V. These outputs drive the internal N-channel power MOSFETs in either high-side or low-side switching applications (a bridge arrangement would contain two high-side and two low-side N-channel MOSFET switches).

Internal MOSFETs

Each internal MOSFET will handle 4A current peaks. When all four MOSFETs are on, the steady-state $I_{DS(ON)}$ is limited to 1A due to power dissipation limitations.

A body diode connects from source-to-drain on each MOSFET, making them suitable for driving inductive loads. However, the body diode prohibits applications where two different voltages are being switched to the same load. For example, if one MOSFET drain connects to a +12V supply, the other to a +5V supply, and both sources connect to the same load: when the +12V MOSFET turns on, the body diode in the +5V MOSFET forward biases, shorting the two supplies together.

Data Input Latch

Driver outputs are buffered from data inputs by a quad latch. When $\overline{CE}$ is pulled low, the latch is transparent, and data transfers directly to driver outputs. When $\overline{CE}$ goes high, the latch enters hold mode, and new input data is ignored. Input data must be valid 100ns before the rising edge of $\overline{CE}$ and held 10ns (max over temp). The minimum $\overline{CE}$ pulse width is 100ns (Figure 3). If latched operation is not required, connect $\overline{CE}$ to GND.

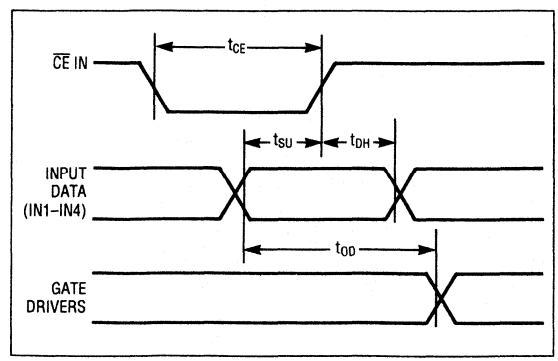


Figure 3. Digital Interface Timing Diagram

Undervoltage Latch Inhibit

If V_{CC} falls below +3V due to power failure, or while powering down, or V+ falls below V_{CC} + 8.5V, the quad latch immediately resets, forcing the driver outputs low. The quad latch remains reset until V_{CC} rises above +3V and V+ exceeds V_{CC} + 8.5V. This prevents the latch from being corrupted with errorneous data during a momentary power failure.

Undervoltage Detector

The MAX625 contains an undervoltage detector which forces all driver outputs low when the high-side voltage (V+) is less than the Power Ready Threshold (PRT = V_{CC} + 8.5V) or when V_{CC} is less than +3V. This ensures that the internal N-channel MOSFETs have sufficient gate drive to operate without dissipating excess power. On power up, the quad latch remains reset until the charge pump boosts the high-side voltage to the PRT. As soon as V+ reaches the PRT, the undervoltage lockout disables, the quad latch is enabled, and Power Ready (PR) goes high. The undervoltage lockout feature also forces the driver outputs low if V+ is pulled below the PRT, e.g. if the driver output(s) or V+ are overloaded.

Power Ready Output

The MAX625's PR output is a direct extension of the undervoltage lockout feature. When power is applied, PR remains a logic low until V+ reaches the PRT and V_{CC} exceeds +3V. The PR output high level is V_{CC}.

Sourcing Current from V+

A small amount of current may be sourced from V+ (pin 16) to drive other circuitry. The amount of current is a function of V_{CC}, and the driver switching rate. (See "Maximum Switching Rate vs. Additional V+ Load Current", *Typical Operating Characteristics*).

The MAX625 V+ output is not internally short-circuit protected. In applications where V+ is susceptible to short circuit, external output short-circuit protection must be provided. To accomplish this, connect a resistor between V+ and the load to limit the V+ current to less than 25mA. The resistor value is determined by the following formula:

$$R_{CL} \geq \frac{V_{CC}}{25mA}$$

Application Information

Data Input Transition Time

The MAX625 is microprocessor-compatible and easy to interface. However, the driver input voltage must not remain between V_{IL} and V_{IH} for more than 500ns. In clocked databus systems, this is most easily accomplished by setting the data on the driver input lines before clocking $\overline{CE}$ low. However, most CMOS and TTL gates easily meet the 500ns transition speed requirement. Connect unused inputs to ground.

Maximum Driver Switching Rate

The maximum driver switching rate is the rate at which loading causes V+ to fall to the PRT (V_{CC} + 8.5V) and the MOSFETs turn off. It is a function of the maximum charge-pump output current available to the drivers at a given supply voltage. For example, with V_{CC} = +5V and no external load on V+, the maximum switching rate while driving all four inputs is 52kHz. (See "Maximum Switching Rate vs. V_{CC}", *Typical Operating Characteristics*).

Typical Application Circuits

For typical application circuits, see the MAX620/621 datasheet.

19-4505; Rev. 0; 12/91

EVALUATION KIT AVAILABLE

MAXIM

High-Efficiency, +5V Adjustable Step-Down Switching Regulator

General Description

The MAX639 high-efficiency step-down switching regulator converts battery voltages between +5.5V and +11.5V to +5V, and supplies 100mA of output current over the entire input voltage range. 10µA quiescent current, greater than 90% efficiency, and 0.5V dropout (0.12V dropout at 25mA output current) extend battery life in portable applications. Additional features include a logic-level shutdown control and low-battery detection circuitry.

The MAX639 requires only four external components: a small low-cost inductor, a diode, an input bypass capacitor, and an output filter capacitor. No compensation components are needed. Voltages other than +5V can be generated by adding two resistors.

The MAX639 is pin compatible with the MAX638, except for the addition of the SHUTDOWN input, and is available in 8-pin DIP and SO packages.

Applications

High-Efficiency DC-DC Step Down Regulation

Linear Voltage Regulator Replacement

+9V to +5V Conversion

Battery-Life Extension

Portable Instruments

Features

- **High Efficiency**
  94% at I_{OUT} = 25mA
  91% at I_{OUT} = 100mA
- **Ultra Low 20µA (Max) Quiescent Current**
- **Output Currents Up to 225mA**
- **Preset +5V or Adjustable Output Voltage**
- **Only 4 External Components**
- **TTL/CMOS Compatible Shutdown Control**
- **Low-Battery Detector**
- **500mV (Typ) Dropout Voltage (100mA Load)**
- **8-Pin SO and Plastic DIP Packages**

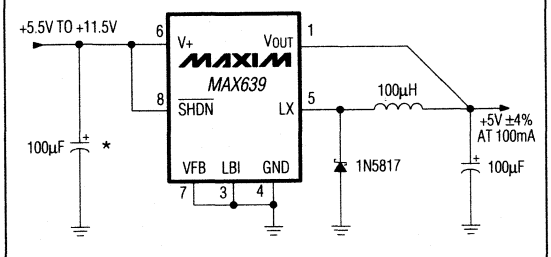
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX639CPA	0°C to +70°C	8 Plastic DIP
MAX639CSA	0°C to +70°C	8 SO
MAX639C/D	0°C to +70°C	Dice*
MAX639EPA	-40°C to +85°C	8 Plastic DIP
MAX639ESA	-40°C to +85°C	8 SO
MAX639MJA	-55°C to +125°C	8 CERDIP

Contact factory for dice specifications.

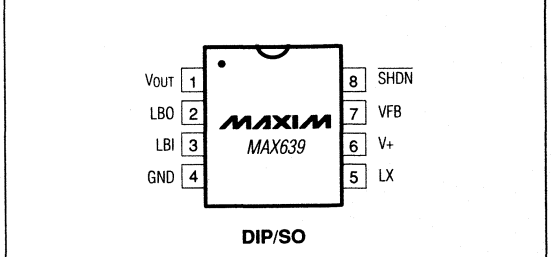
4

Typical Operating Circuit



* An input bypass capacitor must be less than 1cm from the V+ pin (pin 6). If the main bypass capacitor is too distant, then a high-frequency 0.1µF ceramic capacitor must be placed within 1cm of the V+ pin.

Pin Configuration



High-Efficiency, +5V Adjustable Step-Down Switching Regulator

ABSOLUTE MAXIMUM RATINGS

V+ 12V
LX . . . . . (V+ - 12V) to (V+ + 0.3V)
LBI, LBO, VFB, $\overline{SHDN}$, V_{OUT} . . . . . -0.3V to (V+ + 0.3V)
LX Output Current 1A
LBO Output Current 10mA
Continuous Power Dissipation
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX639C_ _ . . . . . 0°C to +70°C
MAX639E_ _ . . . . . -40°C to +85°C
MAX639MJA . . . . . -55°C to +125°C
Storage Temperature Range . . . . . -65°C to +160°C
Lead Temperature (soldering , 10 sec) . . . . . +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 9V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

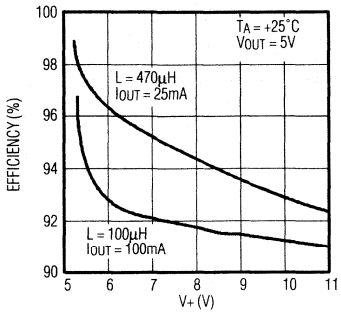
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		4.0		11.5	V
Supply Current	$\overline{SHDN}$ = V+, No load		10	20	µA
V_{OUT} (Note 1)	V+ = 6.0V to 11.5V, 0mA < I_{OUT} < 100mA	4.80	5.00	5.20	V
Dropout Voltage	I_{OUT} = 100mA, L = 100µH		0.5		V
Efficiency	I_{OUT} = 100mA, L = 100µH		91		%
	I_{OUT} = 25mA, L = 470µH		94		
t_{ON}	V+ = 9V, V_{OUT} = 5V	11.0	12.5	14.0	µs
	V+ = 6V, V_{OUT} = 3V	14.2	16.7	19.2	
t_{OFF}	V+ = 9V, V_{OUT} = 5V	8.5	10.0	11.5	µs
	V+ = 6V, V_{OUT} = 3V	14.2	16.7	19.2	
LX Peak Current				600	mA
LX Switch r_{ON}	V+ = 9V, T_A = +25°C		0.8	1.5	Ω
	V+ = 6V			2.5	
LX Switch Leakage	V+ = 12V, V_{LX} = 0V, T_A = +25°C		0.003	1.0	µA
	V+ = 12V, V_{LX} = 0V			30	
VFB I_{BIAS}	VFB = 2V		4	15	nA
VFB Dual Mode Trip Point			50		mV
VFB Threshold	MAX639C	1.26	1.28	1.30	V
	MAX639E, M	1.24	1.28	1.32	
LBI I_{BIAS}	V_{LBI} = 2V		2	10	nA
LBI Threshold	MAX639C	1.26	1.28	1.30	V
	MAX639E, M	1.24	1.28	1.32	
LBO Sink Current	V_{LBO} = 0.4V	0.80	2.50		mA
LBO Leakage Current	V_{LBO} = 12V		0.001	0.1	µA
LBO Delay	50mV Overdrive		25		µs
$\overline{SHDN}$ Threshold		0.80	1.15	2.00	V
$\overline{SHDN}$ Pull-Up Current	$V_{\overline{SHDN}}$ = 0V	0.10	0.20	0.40	µA

Note 1. Load regulation guaranteed by correlation to DC pulse measurements.

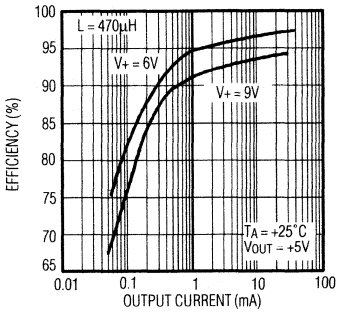
High-Efficiency, +5V Adjustable Step-Down Switching Regulator

Typical Operating Characteristics

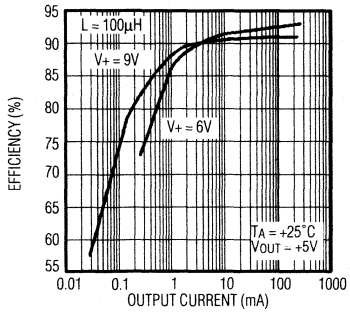
EFFICIENCY vs. INPUT VOLTAGE



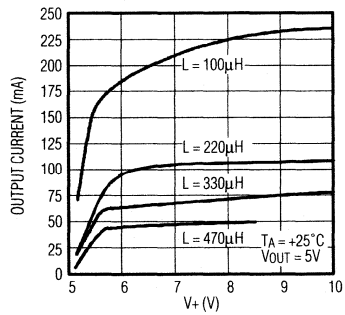
EFFICIENCY vs. OUTPUT CURRENT



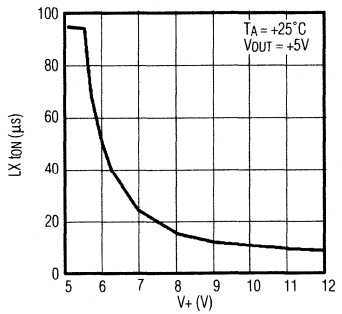
EFFICIENCY vs. OUTPUT CURRENT



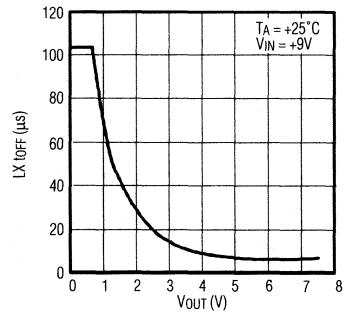
OUTPUT CURRENT vs. INPUT VOLTAGE



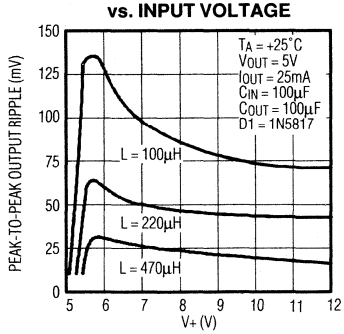
OSCILLATOR PULSE ON TIME vs. INPUT VOLTAGE



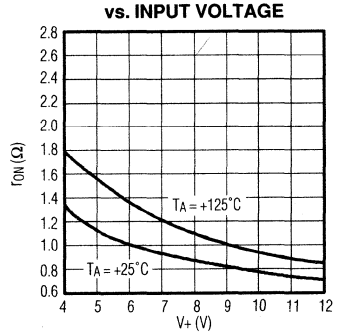
OSCILLATOR PULSE OFF TIME vs. OUTPUT VOLTAGE



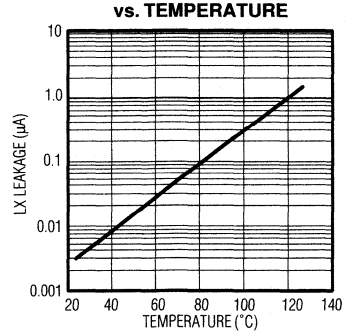
OUTPUT RIPPLE vs. INPUT VOLTAGE



LX ON RESISTANCE vs. INPUT VOLTAGE



LX LEAKAGE CURRENT vs. TEMPERATURE



4

High-Efficiency, +5V Adjustable Step-Down Switching Regulator

Pin Description

PIN	NAME	FUNCTION
1	VOUT	Sense pin for fixed +5V output operation. Internally connected to an on-chip voltage divider. VOUT also connects to the variable duty cycle on demand oscillator, and so must be connected to the regulator output even if the output is adjusted externally.
2	LBO	Low-Battery Output. An open drain N-channel MOSFET sinks current when the voltage at LBI drops below +1.28V.
3	LBI	Low-Battery Input. When the voltage on LBI drops below +1.28V, LBO sinks current.
4	GND	Ground
5	LX	Drain of a PMOS power switch that has its source connected to V+. LX drives the external inductor which provides current to the load.
6	V+	Positive Supply Voltage Input. Should not exceed 11.5V.
7	VFB	Dual-Mode Feedback pin. When VFB is grounded, the internal voltage divider sets the output to +5V. For adjustable operation, connect VFB to an external voltage divider.
8	$\overline{SHDN}$	Shutdown input — active low. When pulled below 0.8V, the LX power switch stays off, shutting down the regulator. When the shutdown input is above 2V, the regulator stays on. Tie $\overline{SHDN}$ to V+ if shutdown mode is not used.

Getting Started

Designing power supplies with the MAX639 is easy. The few required external components are readily available off-the-shelf. The most general application uses the following components:

Capacitors: The values of the input and output filter capacitors are not critical. As a start, they can be electrolytics in the range of 100µF. Low-ESR capacitors are preferable.

Diode: The diode should be the popular 1N5817 Schottky or equivalent.

Inductor: Choose a 100µH inductor with an incremental saturation current rating of at least 600mA. This inductor will provide the highest output current. To optimize the selection of the inductor to obtain the highest efficiencies and smallest size, refer to the *Inductor Selection* section under *Application Information*.

The following sections provide more detailed descriptions of the MAX639 and how to select its components. These sections are intended to assist you in fine-tuning your designs, and to explain the operation of the MAX639 in more detail.

Detailed Description

Figure 1 shows a simplified step-down DC-DC converter. When the switch is closed, a voltage equal to V+ minus VOUT is applied to the inductor. The current through the inductor ramps up, storing energy in the inductor's magnetic field. This same current also flows into the output filter capacitor and load. When the switch opens, the current continues to flow through the inductor in the same direction, but since the switch is now open, the current must flow through the diode. When the switch is open, the inductor alone supplies current to the load. This current decays to zero as the energy stored in the inductor's magnetic field is transferred to the output filter capacitor and the load.

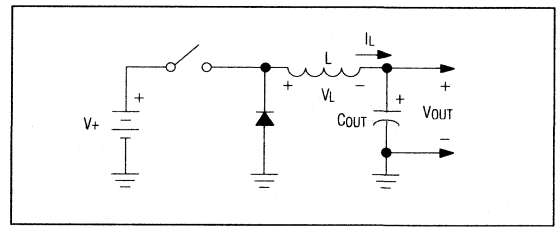


Figure 1. Simplified Step-Down Converter

Figure 2 shows what happens to the ideal circuit of Figure 1 if the switch turns on with a 66% duty cycle and VIN = 3/2 VOUT. The inductor current rises more slowly than it falls since the magnitude of the voltage applied during tON is less than that applied during tOFF. Varying the duty cycle and switching frequency keeps the peak current constant as input voltage varies. The MAX639 controls

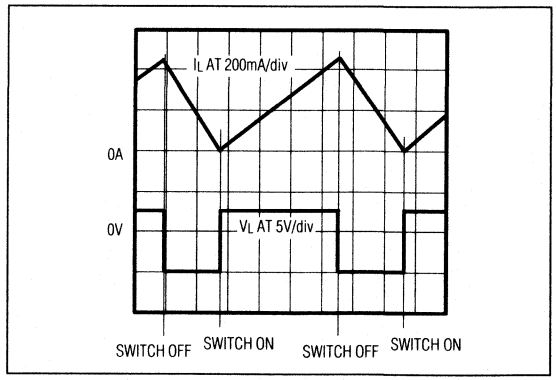


Figure 2. Simplified Step-Down Converter Operation

High-Efficiency, +5V Adjustable Step-Down Switching Regulator

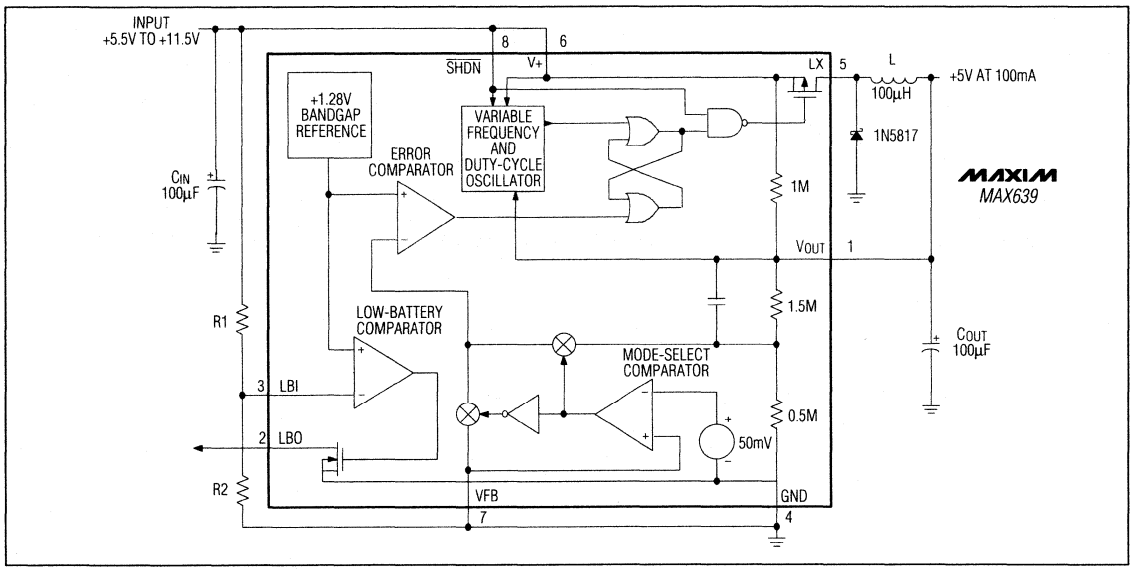


Figure 3. MAX639 Block Diagram

the switch (t_{ON} and t_{OFF}) according to the following formula:

Equation 1. $(V+ - V_{OUT}) \times t_{ON} = 50\mu sV$

Equation 2. $V_{OUT} \times t_{OFF} = 50\mu sV$

Equation 3. $I_{PEAK} = \frac{50\mu sV}{L}$

If we ignore the voltage drop across the diode (D1) and the resistive losses in the switch and inductor, the above formulation ensures constant peak currents across all input voltages for a given inductor value. The variable duty cycle also ensures that the current through the inductor discharges to zero at the end of each pulse.

Figure 3 shows the MAX639 block diagram and a typical connection in which +9V is converted to +5V. When the output drops below +5V, the error comparator switches high. This starts the internal oscillator (15µs start-up time) and connects it to the gate of the LX output driver. LX turns on and off according to t_{ON} and t_{OFF}, charging and discharging the inductor and supplying current to the output as described above. When the output reaches +5V, the comparator switches low, LX turns off, and the oscillator shuts down to save power.

Fixed or Adjustable Output

For operation at the preset +5V output voltage, VFB is connected to GND and no external resistors are required.

For other output voltages, an external voltage divider is connected to VFB as shown in Figure 4. The output is set by R3 and R4 as follows. Let R4 be any resistance in the 10kΩ to 1MΩ range, typically 100kΩ, then:

$$R3 = R4\left(\frac{V_{OUT}}{1.28} - 1\right)$$

Low-Battery Detector

The low-battery detector compares the voltage on the LBI input with the internal 1.28V reference. LBO goes low whenever the input voltage at LBI is less than 1.28V. The low battery detection voltage is set by resistors R1 and R2 (Figure 3). Let R2 be any resistance in the 10kΩ to 1MΩ range, typically 100kΩ, then:

$$R1 = R2\left(\frac{V_{LB}}{1.28} - 1\right)$$

where V_{LB} = desired low-battery detection voltage.

Application Information

Inductor Selection

When selecting an inductor, consider these four factors: peak current rating, inductance value, series resistance, and size. It is important not to exceed the inductor's peak current rating. A saturated inductor will pull excessive currents through the MAX639's switch and may cause

High-Efficiency, +5V Adjustable Step-Down Switching Regulator

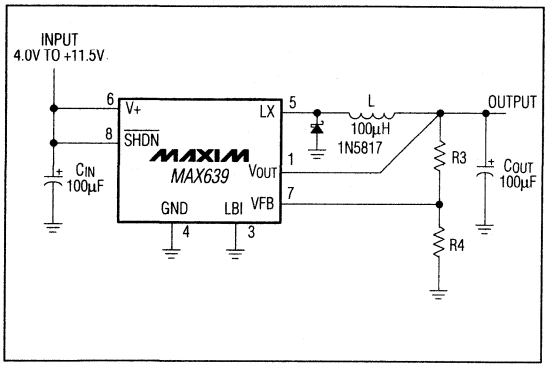


Figure 4. Adjustable Output Operation

damage. Avoid using RF chokes or air-core inductors since they have very low peak-current ratings. Electromagnetic interference must not upset nearby circuitry or the regular IC. Ferrite bobbin types work well for most digital circuits; toroids or pot cores work well for EMI-sensitive analog circuits.

Recall that the inductance value determines I_{PEAK} for all input voltages (Equation 3). If there are no resistive losses and the diode is ideal, the maximum current that can be drawn from the MAX639 will be one-half I_{PEAK}. With the real losses in the switch, inductor, and diode taken into account, the real maximum output current typically varies from 90% to 50% of the ideal. The following steps describe a conservative way to pick an appropriate inductor.

Step 1: Decide what the maximum output current will be in amps; I_{OUTMAX}.

Step 2: Let $I_{PEAK} = 4 \times I_{OUTMAX}$.

Step 3: Pick $L = 50 / I_{PEAK}$. L will be in µH. Do not use an inductor that is less than 100µH.

Step 4: Make sure that I_{PEAK} does not exceed 0.6A or the inductor's maximum current rating, whichever is lower.

Inductor series resistance affects both efficiency and dropout voltage. A high series resistance severely limits the maximum current available at lower input voltages. Output currents up to 225mA are possible if the inductor has low series resistance. Inductor and series switch resistance form an LR circuit during t_{ON}. If the L/R time constant is less than the oscillator t_{ON}, the inductor's peak current will fall short of the desired I_{PEAK}.

Choose the highest value inductor that will provide the required output current over the whole range of your input voltage. Choosing the highest workable inductor value

Table 1. Component Suppliers

Inductors — Through Hole

P/N	Size	Value (µH)	I_{MAX} (A)	Series-R (Ω)
MAXL001*	0.65 x 0.33" dia.	100	1.75	0.2
7300-13**	0.63 x 0.26" dia.	100	0.89	0.27
7300-15**	"	150	0.72	0.36
7300-17**	"	220	0.58	0.45
7300-19**	"	330	0.47	0.58
7300-21**	"	470	0.39	0.86
7300-25**	"	1000	0.27	2.00

*Maxim Integrated Products

**Caddell-Burns
258 East Second Street
Mineola, NY 11501-3508
(516) 746-2310

Inductors — Surface Mount

P/N	Size	Value (µH)	I_{MAX} (A)	Series-R (Ω)
CD54	5.2 x 5.8 x 4.5mm	100	0.52	0.63
CD54	"	220	0.35	1.50
CDR74	7.1 x 7.7 x 4.5mm	100	0.52	0.51
CDR74	"	220	0.35	0.98
CDR105	9.2 x 10.0 x 5.0mm	100	0.80	0.35
CDR105	"	220	0.54	0.69

Sumida Electric (USA)
637 East Golf Road
Arlington Heights, IL 60005
(708) 956-0666

Capacitors — Low ESR

P/N	Size	Value (µF)	ESR (Ω)	V_{MAX} (V)
MAXC001*	0.49 x 0.394" dia.	150	0.2	35
267 Series**	D SM packages	47	0.2	10
267 Series**	E SM packages	100	0.2	6.3

*Maxim Integrated Products

**Matsuo Electronics
2134 Main Street
Huntington Beach, CA 92648
(714) 969-2491

Schottky Diodes — Surface Mount

P/N	Size	V_F(V)	I_{MAX} (A)
SE014	SOT89	0.55	1
SE024	SOT89	0.55	0.95

Collmer Semiconductor
14368 Proton Road
Dallas, TX 75244
(214) 233-1589

NOTE: This list does not constitute an endorsement by Maxim Integrated Products and is not intended to be a comprehensive list of all manufacturers of these components.

High-Efficiency, +5V Adjustable Step-Down Switching Regulator

will provide the highest efficiencies (see *Typical Operating Characteristics*). Inductors with peak currents in the 600mA range do not need to be very large. They are about the size of a 1W resistor, with surface-mount versions approaching the size of a pea. Table 1 lists companies that supply suitable inductors for use with the MAX639.

Output Filter Capacitor

The MAX639's output ripple has two components. One component results from the change in stored charged on the filter capacitor with each LX pulse. The other is the product of the current into the capacitor and the capacitor's equivalent series resistance (ESR).

The amount of charge delivered in each oscillator pulse is determined by the inductor value and input voltage. The amount of charge per pulse decreases with increasing inductor size, but increases with decreasing input voltage. As a general rule, the smaller the amount of charge delivered in each pulse, the less the output ripple will be.

With low-cost aluminum electrolytic capacitors, the ESR-induced ripple can be larger than that caused by the change in charge. Consequently, high-quality aluminum electrolytic or tantalum filter capacitors will minimize output ripple. Best results at a reasonable cost are typically achieved with an aluminum electrolytic capacitor in the 100µF range, in parallel with a 0.1µF ceramic capacitor (see Table 1).

External Diode

In most MAX639 circuits, the current in the external diode (D1, Figure 3) changes abruptly from zero to its peak value each time LX switches off. To avoid excessive losses, the diode must have a fast turn-on time. For low-power circuits with peak currents less than 100mA, signal diodes such as the 1N4148 perform well. For higher-power circuits, or for maximum efficiency at low power, the 1N5817 series of Schottky diodes are recommended. 1N5817 equivalent diodes are also available in surface-mount packages (see Table 1). Although the 1N4001 and other general-purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-on time results in excessive losses.

Minimum Load

Under no-load conditions, because of the leakage of the PMOS power switch (see *Typical Operating Characteristics, LX Leakage Current vs. Temperature*) and the internal 1MΩ resistor from V+ to VOUT, leakage current may be supplied to the output capacitor even when the switch is off. Typically, for a 5V output at room temperature, this will not be a problem, since the reverse leakage current of the diode and the current drawn by the feedback resistors drain the excess current. However, if the diode leakage is very low (which can occur at low temperatures and/or small output voltages), charge may build up on the output capacitor, making VOUT rise above its set point. If this happens, simply add a small load resistor (typically 1MΩ) to the output to pull a few extra microamps of current from the output capacitor.

Layout

The MAX639 operates by switching the inductor current at high speed, so proper input bypassing is important. An input bypass capacitor must be less than 1cm from the V+ pin (pin 6). If the main bypass capacitor is too distant, then a high-frequency 0.1µF ceramic capacitor must be placed within 1cm of the V+ pin.

Several of the external components in a MAX639 circuit experience peak currents up to 600mA. Wherever one of these components connects to ground, the potential for ground bounce exists. Ground bounce occurs when high currents flow through the parasitic resistance of PC board traces. What one component sees as ground can be several millivolts different from the MAX639's ground. This may affect the MAX639's ripple performance, since the error comparator (which is referenced to ground) will generate extra switching pulses when they are not needed, increasing the output ripple. It is essential that the ground lead of the input filter capacitor, the MAX639 GND pin, the diode's anode and the ground lead of the output filter capacitor be as close together as possible. Figure 5 shows a suggested through-hole printed circuit layout that minimizes ground bounce.

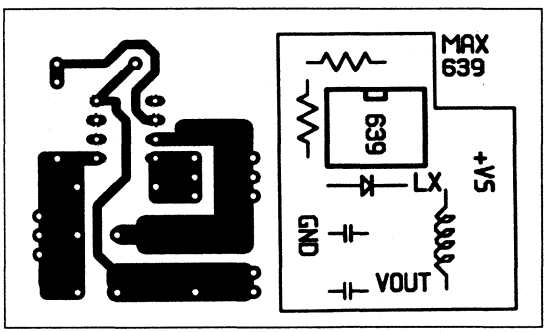


Figure 5. Through Hole PC Layout and Component Placement Diagram for Standard Step-Down Application (Top-Side View)

Inverter Configuration

Figure 6 shows the MAX639 in a floating ground configuration. By tying what would normally be the +5V output to the supply voltage ground, the GND pin of the MAX639 is forced to a regulated -5V. Avoid exceeding

High-Efficiency, +5V Adjustable Step-Down Switching Regulator

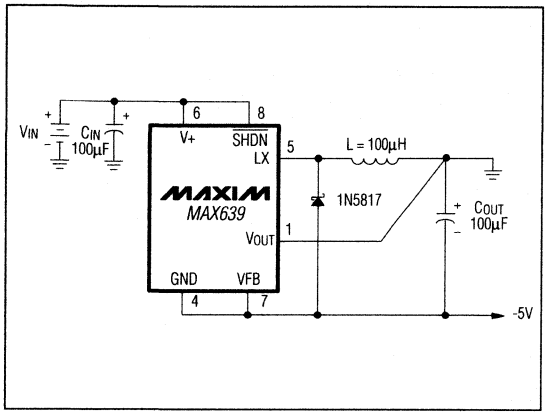


Figure 6. Inverting Configuration

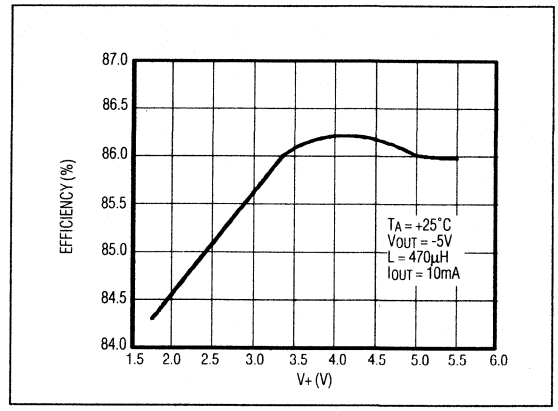


Figure 8. Effficiency of Figure 6 Circuit

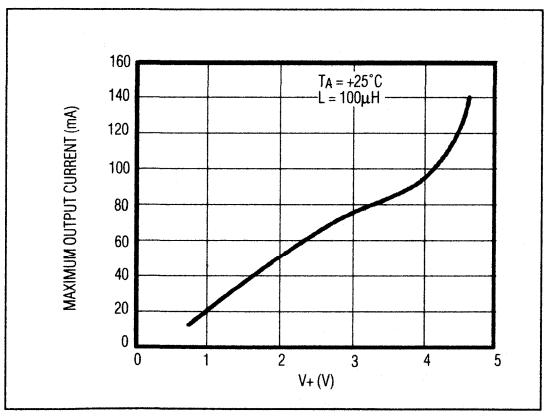


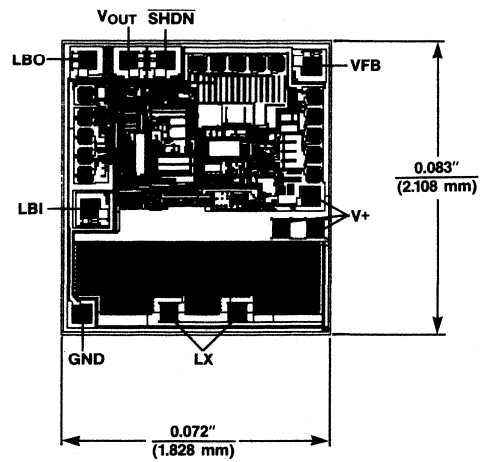
Figure 7. Maximum Current Capability of Figure 6 Circuit

the maximum differential voltage of 11.5V from V_{IN} to V_{OUT}. Other negative voltages can be generated by placing a voltage divider across C_{OUT} and connecting the tap point to VFB in the same manner as the normal step-down configuration.

Two AA Batteries to 5V Configuration

For battery-powered applications, where the signal ground does not have to correspond to the power supply ground, the circuit in Figure 6 generates 5V from a pair of AA batteries. Connect the V_{IN} ground point to the +5V input of your system and connect the -5V output to the ground input of your system. This configuration has the added advantage that the internal power FET of the MAX639 has V_{IN} plus 5V of gate drive, thus reducing on resistance (see Figures 7 and 8).

Chip Topography



TRANSISTOR COUNT: 221

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

+12V, 25mA Flash Memory Programming Supply

General Description

The MAX661 is a regulated +12V, 25mA-output, charge-pump DC-DC voltage converter. It provides the necessary +12V ±5% output to program byte-wide flash memories, and requires no inductors to deliver a guaranteed 25mA output from inputs as low as 4.75V. It fits into less than 0.2in^2 of board space.

The MAX661 is the first charge-pump boost converter to provide a regulated +12V output without using inductors. It requires only a few inexpensive, miniature capacitors, and the entire circuit is completely surface-mountable.

A logic-controlled shutdown pin that interfaces directly with microprocessors cuts supply current to only 1µA. This device comes in 14-pin narrow SO and plastic DIP packages.

For higher-current flash memory programming solutions, refer to the MAX734 and MAX732 PWM switch-mode DC-DC converter data sheets. They have guaranteed output currents of 120mA and 200mA, respectively. Also refer to the MAX717-MAX721 data sheet for dual-output power-supply chips that integrate both main V_{CC} (3V/3.3V/or 5V) and auxiliary +12V flash memory power supplies on a single device and operate from 2V minimum inputs.

Applications

+12V Flash Memory Programming Supplies

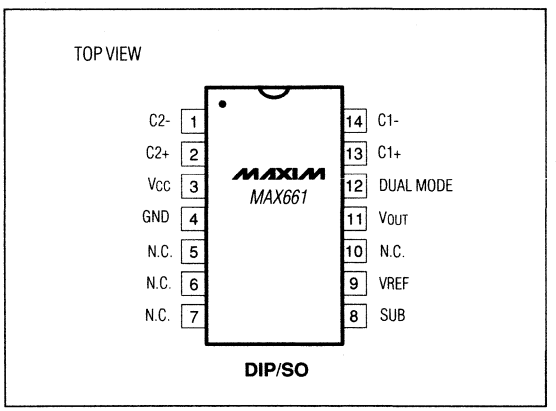
Compact +12V Op-Amp Supplies

Switching MOSFETs in Low-Voltage Systems

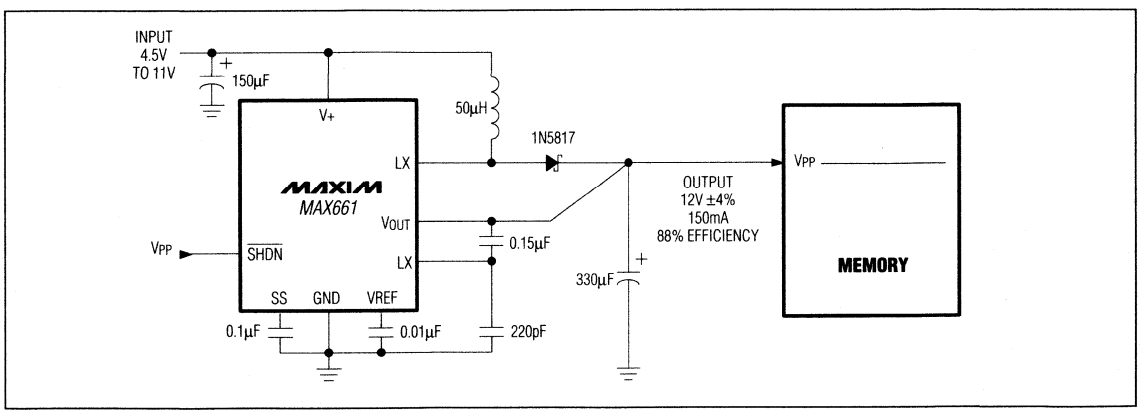
Features

- **Regulated +12V ±5% Output**
- **Fits in 0.2in^2**
- **Guaranteed 25mA Output Current**
- **No Inductors - Uses Only Capacitors**
- **200mA Quiescent Supply Current**
- **Logic-Controlled 10µA Shutdown**
- **14-Pin Narrow SO and Plastic DIP Packages**

Pin Configuration



Typical Operating Circuit



19-0011; Rev. 0; 6/92

MAXIM

8V CMOS Switched-Capacitor Voltage Converter

General Description

The MAX665 charge-pump voltage inverter converts a +1.5V to +8V input to a corresponding -1.5V to -8V output. Using only two low-cost capacitors to produce 100mA, the MAX665 replaces switching regulators, eliminating inductors and their associated cost, size, and EMI. Greater than 90% efficiency over most of its load-current range combined with a 200µA typical operating current provides ideal performance for both battery-powered and board-level voltage conversion applications. The MAX665 can also double the output voltage of an input power supply or battery, providing +9.35V at 100mA from a +5V input.

A Frequency Control (FC) pin selects either 10kHz or 45kHz operation to optimize capacitor size and quiescent current. The oscillator frequency can also be adjusted with an external capacitor or driven with an external clock. The MAX665 is a pin-compatible high-current upgrade of the ICL7660. For an 8-pin SO version with a 5.5V maximum input voltage, refer to the MAX660 data sheet.

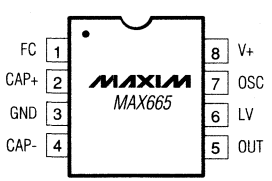
The MAX665 is available in both 8-pin DIP and 16-pin wide SO packages in commercial, extended, and military temperature ranges.

Applications

Laptop Computers
Medical Instruments
Interface Power Supplies
Handheld Instruments
Op-Amp Power Supplies
GaAs Power-Amp Bias Supplies

Pin Configurations

TOP VIEW



DIP

Wide SO on last page

Features

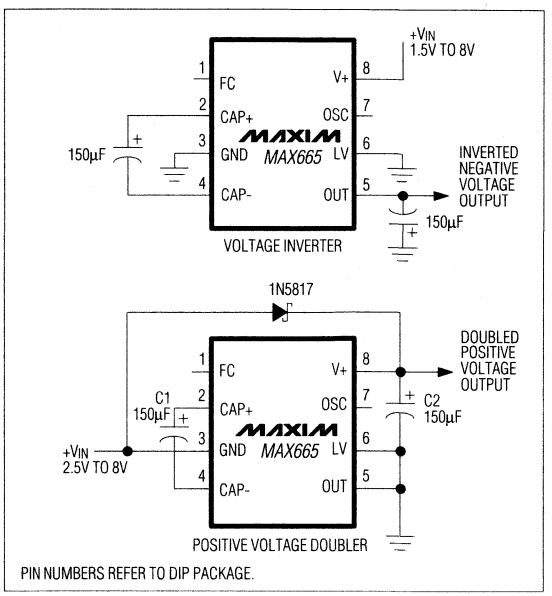
- **0.65V Loss at 100mA Load**
- **6.5Ω Output Impedance**
- **Pin-Compatible High-Current ICL7660 Upgrade**
- **Inverts or Doubles Input Supply Voltage**
- **Selectable Oscillator Frequency: 10kHz/45kHz**
- **88% Conversion Efficiency at 100mA (I_L to GND)**
- **200µA Operating Current**
- **+1.5V to +8V Supply**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX665CPA	0°C to +70°C	8 Plastic DIP
MAX665CWE	0°C to +70°C	16 Wide SO
MAX665C/D	0°C to +70°C	Dice*
MAX665EPA	-40°C to +85°C	8 Plastic DIP
MAX665EWE	-40°C to +85°C	16 Wide SO
MAX665MJA	-55°C to +125°C	8 CERDIP

** Dice are tested at +25°C only.*

Typical Operating Circuits



PIN NUMBERS REFER TO DIP PACKAGE.

8V CMOS Switched-Capacitor Voltage Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND, or GND to OUT) ..... +8.5V
LV Input Voltage ..... (OUT - 0.3V) to (V+ + 0.3V)
FC and OSC Input Voltages ..... The Least Negative of (OUT - 0.3V) or (V+ - 6V) to (V+ + 0.3V)
OUT and V+ Continuous Output Current 120mA
Output Short-Circuit Duration to GND (Note 1) ..... 1 sec
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) . 727mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX665C _ _ ..... 0°C to +70°C
MAX665E _ _ ..... -40°C to +85°C
MAX665MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: OUT may be shorted to GND for 1 sec without damage, but shorting OUT to V+ may damage the device.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, C1, C2 = 150µF, test circuit of Figure 1, FC = open, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Voltage	R_L = 1kΩ	Inverter, LV = open	3		8	V
		Inverter, LV = GND	1.5		8	
		Doubler, LV = OUT	2.5		8	
Supply Current	No load	FC = open		0.2	0.5	mA
		FC = V+		1	3	
Output Current	$T_A \leq$ +85°C, OUT more negative than -4V		100			mA
	$T_A >$ +85°C, OUT more negative than -3.8V		100			
Output Resistance (Note 3)	I_L = 100mA	$T_A \leq$ +85°C		6.5	10	Ω
		$T_A >$ +85°C			12	
Oscillator Frequency	FC = open			10		kHz
	FC = V+			45		
OSC Input Current	FC = open			±1.1		µA
	FC = V+			±5		
Power Efficiency	R_L = 1kΩ connected between V+ and OUT		96	98		%
	R_L = 500Ω connected between OUT and GND		92	96		
	I_L = 100mA to GND			88		
Voltage Conversion Efficiency	No load		99	99.96		%

Note 2: In the test circuit, capacitors C1 and C2 are 150µF, 0.2Ω maximum ESR, aluminum electrolytics (Maxim part # MAXC001). Capacitors with higher ESR may reduce output voltage and efficiency.
Note 3: Specified output resistance is a combination of internal switch resistance and capacitor ESR. See *Capacitor Selection* section.

8V CMOS Switched-Capacitor Voltage Converter

Typical Operating Characteristics

All curves are generated using the test circuit of Figure 1 with V+ = 5V, LV = GND, FC = open, and T_A = +25°C, unless otherwise noted. The charge-pump frequency is one-half the oscillator frequency. Test results are also valid for doubler mode with GND = +5V, LV = OUT, and OUT = 0V, unless otherwise noted; however, the input voltage is restricted to +2.5V to +8V.

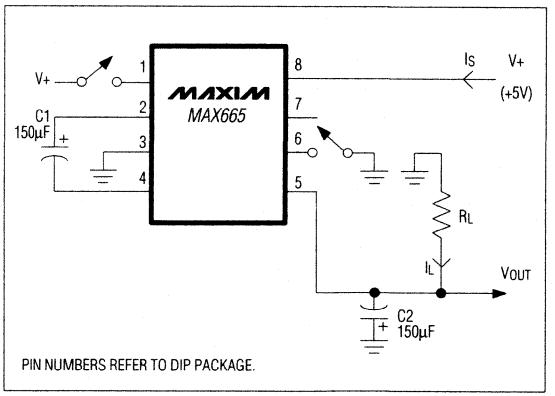
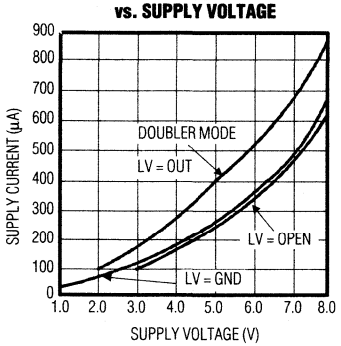
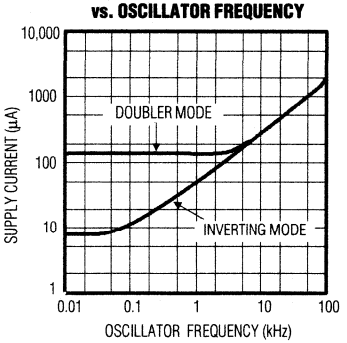


Figure 1. MAX665 Test Circuit

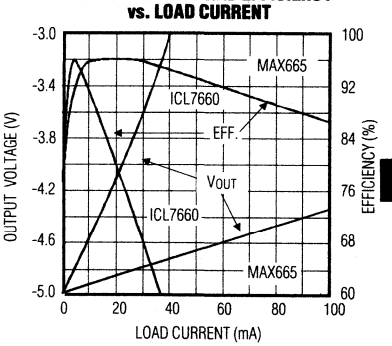
SUPPLY CURRENT vs. SUPPLY VOLTAGE



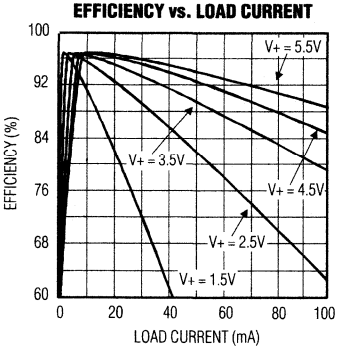
SUPPLY CURRENT vs. OSCILLATOR FREQUENCY



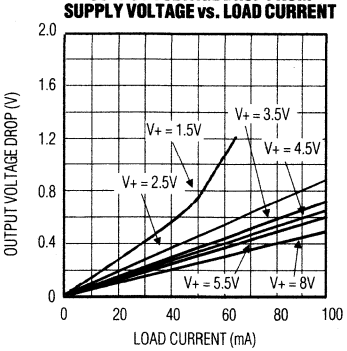
OUTPUT VOLTAGE AND EFFICIENCY vs. LOAD CURRENT



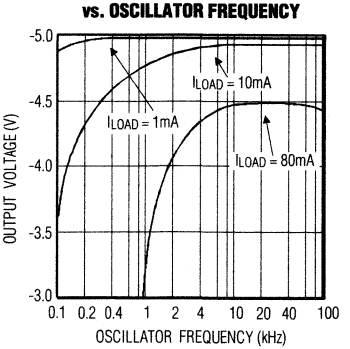
EFFICIENCY vs. LOAD CURRENT



OUTPUT VOLTAGE DROP FROM SUPPLY VOLTAGE vs. LOAD CURRENT



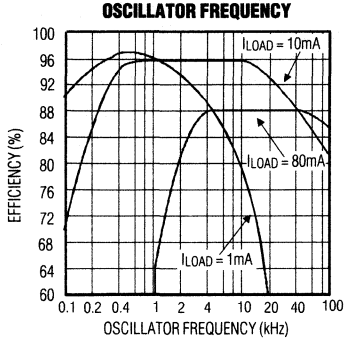
OUTPUT VOLTAGE vs. OSCILLATOR FREQUENCY



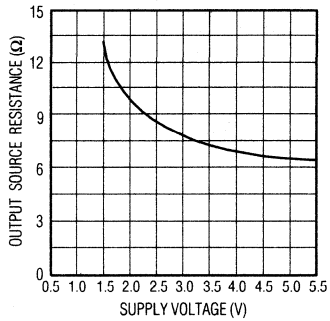
8V CMOS Switched-Capacitor Voltage Converter

Typical Operating Characteristics (continued)

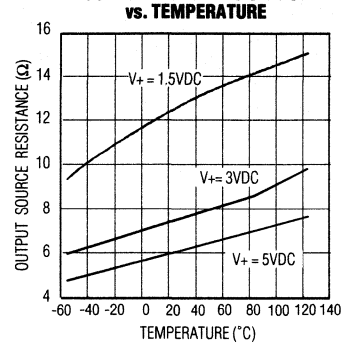
EFFICIENCY vs. OSCILLATOR FREQUENCY



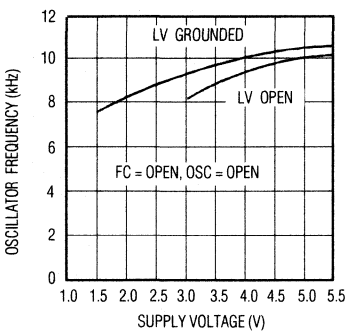
OUTPUT SOURCE RESISTANCE vs. SUPPLY VOLTAGE



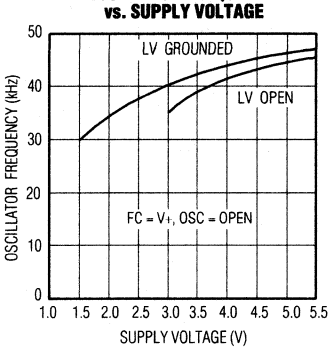
OUTPUT SOURCE RESISTANCE vs. TEMPERATURE



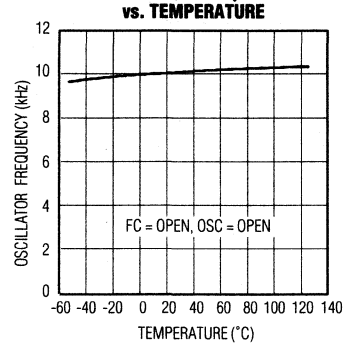
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



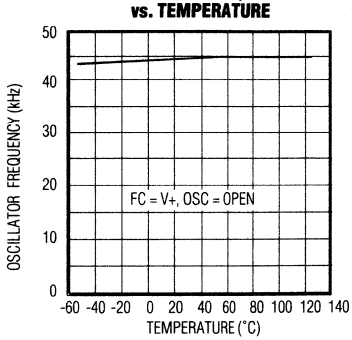
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



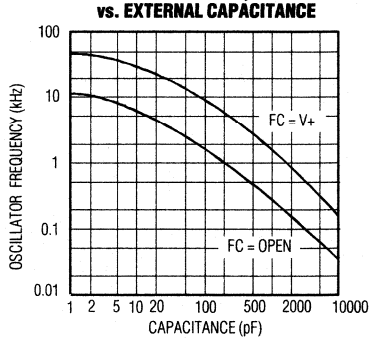
OSCILLATOR FREQUENCY vs. TEMPERATURE



OSCILLATOR FREQUENCY vs. TEMPERATURE



OSCILLATOR FREQUENCY vs. EXTERNAL CAPACITANCE



8V CMOS Switched-Capacitor Voltage Converter

Pin Description

PIN		NAME	FUNCTION	
DIP	WIDE SO		INVERTER	DOUBLER
1	2	FC	Frequency Control for internal oscillator. FC = open, f_{OSC} = 10kHz typ; FC = V+, f_{OSC} = 45kHz typ; FC has no effect when OSC pin is driven externally.	Same as inverter
2	4	CAP+	Positive Charge-Pump Capacitor Terminal	Same as inverter
3	6	GND	Power-Supply Ground Input	Power-Supply Positive Voltage Input
4	8	CAP-	Negative Charge-Pump Capacitor Terminal	Same as inverter
5	9	OUT	Output, Negative Voltage	Power-Supply Ground Input
6	11	LV	Low-Voltage Operation Input. Tie LV to GND when input voltage is less than 3V. Above 3V, LV may be connected to GND or left open; when overdriving OSC, LV must be connected to GND.	LV must be tied to OUT for all input voltages.
7	13	OSC	Oscillator Control Input. OSC is connected to an internal 15pF capacitor. An external capacitor can be added to slow the oscillator. Care must be taken to minimize stray capacitance. An external oscillator may also be connected to overdrive OSC.	Same as inverter; however, do not overdrive OSC in voltage doubler mode.
8	16	V+	Power-Supply Positive Voltage Input	Positive Voltage Output
—	1, 3, 5, 7, 10, 12, 14, 15	N.C.	No Connect - not internally connected	No Connect

Detailed Description

The MAX665 capacitive charge-pump circuit either inverts or doubles the input voltage. Two external capacitors are needed in the voltage inverting mode, while two capacitors and one diode are needed for the voltage doubling mode (see *Typical Operating Circuits*). For highest performance, use low effective series resistance (ESR) capacitors. See *Capacitor Selection* section for more details.

When using the inverting mode with a supply voltage less than 3V, LV must be connected to GND. This bypasses the internal regulator circuitry and provides best performance in low-voltage applications. When using the inverter mode with a supply voltage above 3V, LV may be connected to GND or left open. The part is typically operated with LV grounded, but since LV may be left open, the substitution of the MAX665 for the ICL7660 is simplified. LV must be grounded when overdriving OSC (see *Changing Oscillator Frequency* section). Connect LV to OUT (for any supply voltage) when using the doubler mode.

Applications Information

Negative Voltage Converter

The most common application of the MAX665 is as a charge-pump voltage inverter. The operating circuit uses only two external capacitors, C1 and C2 (see *Typical Operating Circuits*). In most applications these are low-cost, low-ESR, 150µF electrolytic capacitors (refer to *Capacitor Selection* section).

Even though its output is not actively regulated, the MAX665 is very insensitive to load current changes. A typical output source resistance of 6.5Ω means that with an input of +5V the output voltage is -5V under light load, and decreases to only -4.35V with a 100mA load. Output source resistance vs. temperature and supply voltage are shown in the *Typical Operating Characteristics* graphs.

Output ripple voltage is calculated by noting that the output current supplied is solely from capacitor C2 during one-half of the charge-pump cycle. This introduces a peak-to-peak ripple of:

$$V_{RIPPLE} = \frac{I_{OUT}}{2(f_{PUMP})(C2)} + I_{OUT}(ESR_{C2})$$

For a nominal f_{PUMP} of 5kHz (one-half the nominal 10kHz oscillator frequency) where C2 = 150µF with an ESR of 0.2Ω, ripple is approximately 90mV with a 100mA load current. If C2 is raised to 390µF, the ripple drops to 45mV.

8V CMOS Switched-Capacitor Voltage Converter

Positive Voltage Doubler

The MAX665 operates in the voltage-doubling mode as shown in the *Typical Operating Circuit*. The external Schottky (1N5817) diode is for start-up only. The no-load output is 2 x V_{IN} and is not reduced by the diode forward drop.

Changing Oscillator Frequency

Four modes control the MAX665's clock frequency, as listed below:

FC	OSC	Oscillator Frequency
Open	Open	10kHz
FC = V+	Open	45kHz
Open or FC = V+	External capacitor	See *Typical Operating Characteristics*
Open	External clock	External clock frequency

When FC and OSC are unconnected (open), the oscillator runs at 10kHz typically. When FC is connected to V+, the charge and discharge current at OSC changes from 1.1µA to 5µA, thus increasing the oscillator frequency 4.5 times. In the third mode, the oscillator frequency is lowered by connecting a capacitor between OSC and GND. FC can still multiply the frequency by 4.5 times in this mode.

In the inverter mode, OSC may also be overdriven by an external clock source that swings within 100mV of V+ and GND. Any standard CMOS logic output is suitable for driving OSC. When OSC is overdriven, FC has no effect. Also, LV must be grounded when overdriving OSC. Do not overdrive the OSC pin in the voltage doubler mode.

Note: In all modes, the frequency of the signal appearing at CAP+ and CAP- is one-half that of the oscillator. Also, an undesirable effect of lowering the oscillator frequency is the charge pump's effective output resistance. Compensate for this by increasing the value of the charge-pump capacitors (see *Capacitor Selection* section and *Typical Operating Characteristics*).

In some applications, the 5kHz output ripple frequency may be low enough to interfere with other circuitry. If desired, the oscillator frequency can then be increased by using the FC pin or an external oscillator as described above. The output ripple frequency is one-half the selected oscillator frequency. Increasing the clock frequency increases the MAX665's quiescent current, but also allows smaller capacitance values to be used for C1 and C2.

Capacitor Selection

Three factors (in addition to load current) affect the MAX665 output voltage drop from its ideal value:

1) MAX665 output resistance,

2) Pump (C1) and reservoir (C2) capacitor ESRs,

3) C1 and C2 capacitance.

The voltage drop caused by MAX665 output resistance is the load current times the output resistance. Similarly, the loss in C2 is the load current times C2's ESR. The loss in C1, however, is larger because it handles currents that are greater than the load current during charge-pump operation. The voltage drop due to C1 is therefore about four times C1's ESR times the load current. Consequently, a low (or high) ESR capacitor has much greater impact on performance for C1 than for C2.

Generally, as the MAX665's pump frequency increases, the capacitance values required to maintain comparable ripple and output resistance diminish proportionately. Figure 2 shows the total circuit output resistance for various capacitor values (the pump and reservoir capacitors' values are equal) and oscillator frequencies. These curves assume 0.25Ω capacitor ESRs and a 5.25Ω MAX665 output resistance, which is why the flat portion of the curve shows a 6.5Ω (R_O MAX665 + 4(ESR_{C1}) + ESR_{C2}) effective output resistance. Note: R_O = 5.25Ω is used, rather than the typical 6.5Ω, because the typical specification includes the effect of the capacitors' ESRs in the test circuit.

To reduce output ripple caused by the charge pump, increase reservoir capacitor C2 and/or reduce its ESR. Also, the reservoir capacitor must have low ESR if filtering high-frequency noise at the output is important.

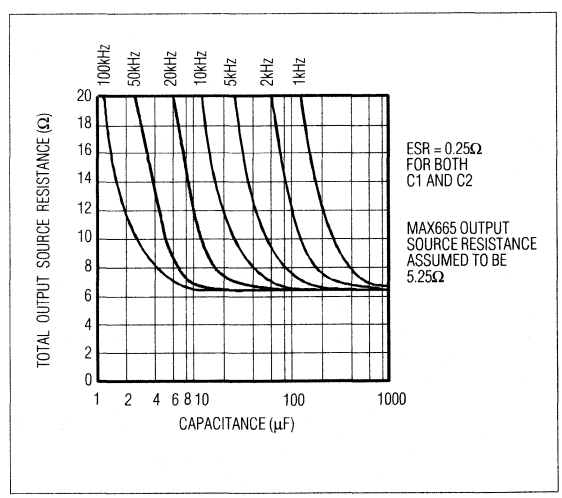


Figure 2. Total Output Source Resistance vs. C1 and C2 Capacitance (C1 = C2)

Not all manufacturers guarantee the capacitor ESR range required by the MAX665. In general, capacitor ESR is inversely proportional to physical size, so larger capacitance values and higher voltage ratings tend to reduce ESR. The capacitors used when testing the MAX665 are MAXC001 150µF aluminum electrolytics available from Maxim. They combine low cost, a guaranteed maximum ESR of 0.2Ω at room temperature, and a low-temperature operating limit of -25°C. If operation at lower temperatures is required, certain tantalum capacitors provide good low-temperature ESR, but at added expense.

Manufacturers who provide low-ESR electrolytic capacitors include:

MANUFACTURER	CAPACITOR	CAPACITOR TYPE
Illinois Capacitor	RZS	Aluminum electrolytic
Mallory Capacitor	TDC & TDL	Tantalum
Nichicon	PF & PL	Aluminum electrolytic
Sprague Electric	672D, 673D, 674D, 678D	Aluminum electrolytic
Sprague Electric	135D, 173D, 199D	Tantalum
United Chemi-Con	LXF & SXF	Aluminum electrolytic

Illinois Capacitor	(708) 675-1760	FAX (708) 673-2850
Mallory Capacitor	(317) 856-3731	FAX (317) 856-2500
Nichicon	(708) 843-7500	FAX (708) 843-2798
Sprague Electric	(508) 339-8900	FAX (508) 339-5063
United Chemi-Con	(708) 696-2000	FAX (708) 640-6341

Cascading Devices

To produce larger negative multiplication of the inititial supply voltage, the MAX665 may be cascaded as shown in Figure 3. The resulting output resistance is approximately equal to the sum of the individual MAX665 ROUT values. The output voltage, where n is an integer representing the number of devices cascaded, is defined by VOUT = -n (VIN).

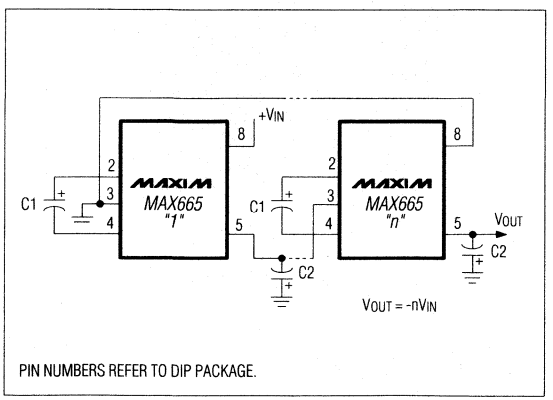


Figure 3. Cascading MAX665s to Increase Output Voltage

Paralleling Devices

Paralleling multiple MAX665s reduces the output resistance. As illustrated in Figure 4, each device requires its own pump capacitor C1, but the reservoir capacitor C2 serves all devices. C2's value should be increased by a factor of n, where n is the number of devices. Figure 4 shows the equation for calculating output resistance.

Combined Positive Supply Multiplication and Negative Voltage Conversion

This dual function is illustrated in Figure 5. In this circuit, capacitors C1 and C3 are pump and reservoir, respectively, for generating the negative voltage. Capacitors C2 and C4 are pump and reservoir for the multiplied positive voltage. This circuit configuration, however, leads to higher source impedances of the generated supplies. This is due to the common charge-pump driver's finite impedance.

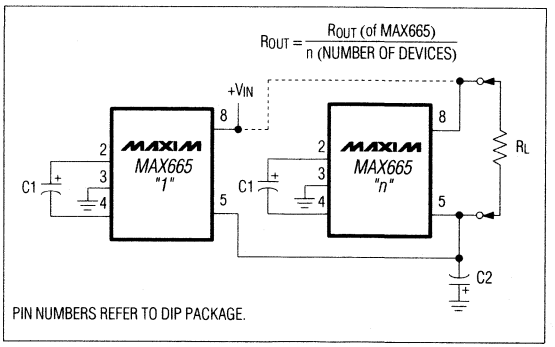


Figure 4. Paralleling MAX665s to Reduce Output Resistance

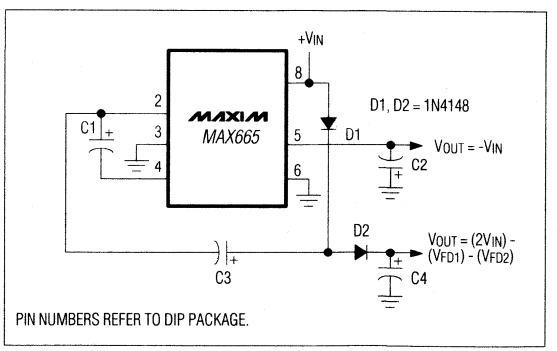


Figure 5. Combined Positive Multiplier and Negative Converter

8V CMOS Switched-Capacitor Voltage Converter

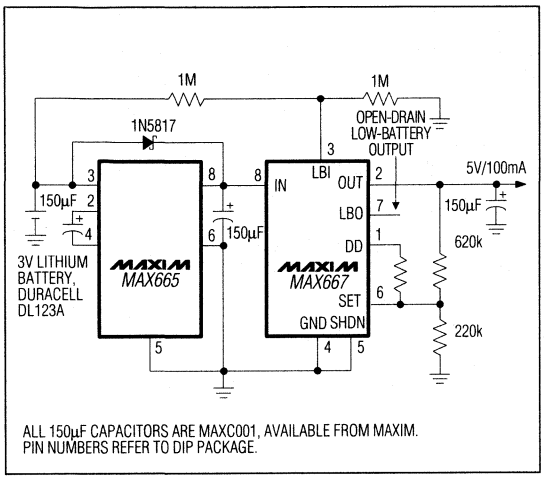
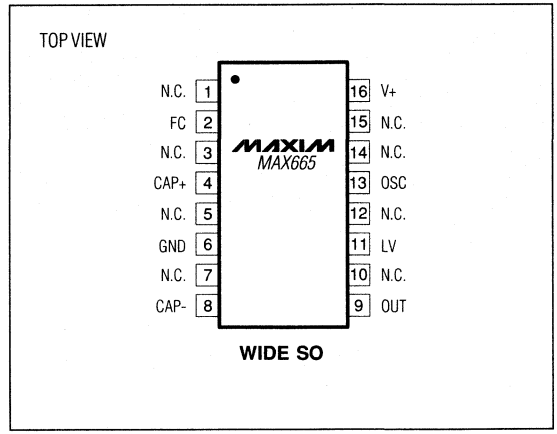
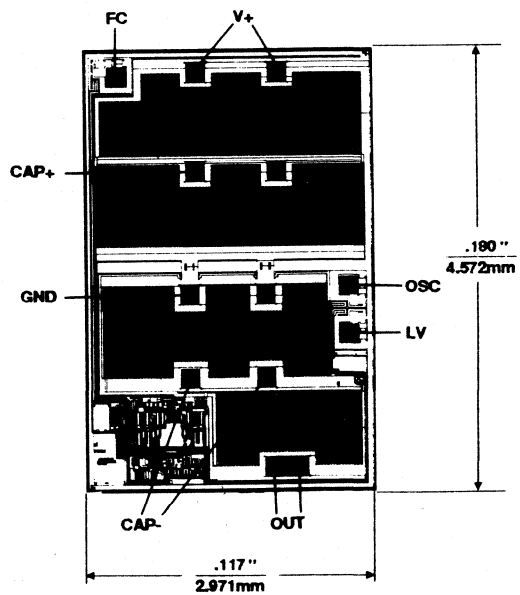


Figure 6. The MAX665 generates a +5V regulated output from a 3V lithium battery and operates for 16 hours with a 40mA load.

Pin Configurations (continued)



Chip Topography



SUBSTRATE CONNECTED TO V+;
TRANSISTOR COUNT: 89.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

NiCad/NiMH Battery Fast-Charge Controllers

General Description

The MAX712 and MAX713 fast charge nickel metal hydride and nickel cadmium batteries from a DC source at least 1V higher than the maximum battery voltage. These devices can charge 1 to 16 series cells at rates up to 4C. A voltage-slope detecting analog-to-digital converter, a timer, and a temperature window comparator determine charge completion. The MAX712/MAX713 are powered by an on-board +5V shunt regulator off the DC source and draw only 5µA maximum from the battery when not charging. A low-side, current-sense resistor allows the battery-charge current to be regulated while still supplying power to the battery's load.

The MAX712 charges NiMH batteries by detecting zero-voltage slope, while the MAX713 uses a negative voltage-slope detection scheme for NiCad batteries. Both parts come in 16-pin DIP and narrow SO packages. An external power PNP, a blocking diode, three resistors and three capacitors are the only external components needed. Optional temperature sensing adds only two low-cost thermistors, three resistors, and a capacitor.

For higher-power charging, the MAX712/MAX713 can easily interface with an ICM7556 and a power MOSFET to form a switch-mode battery charger that minimizes power dissipation.

Applications

Battery-Powered Equipment
- Laptop, Notebook and Palmtop Computers
- Handi-Terminals
- Cellular Telephones

Portable Consumer Products

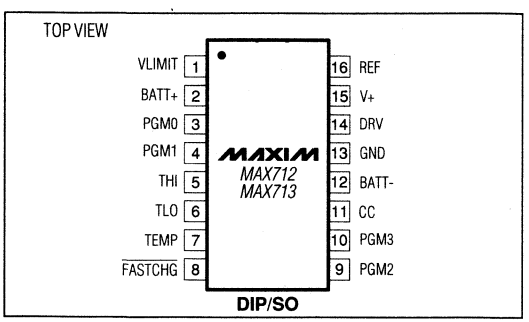
Portable Stereos

Cordless Telephones

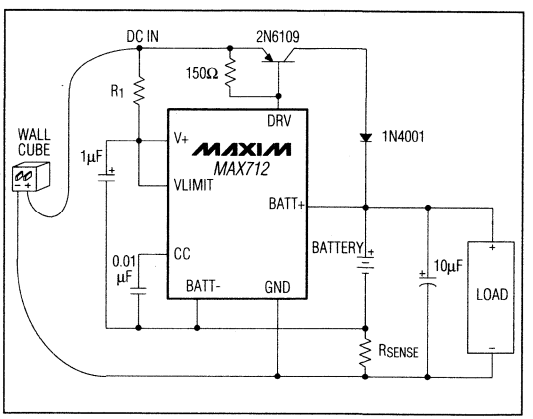
Features

- ♦ **Fast-Charge NiMH (MAX712) or NiCad (MAX713) Batteries**
- ♦ **Charge 1 to 16 Series Cells**
- ♦ **Fast Charge from C/4 to 4C Rate**
- ♦ **C/16 Trickle Charge Rate**
- ♦ **Automatically Switch from Fast to Trickle Charge**
- ♦ **Shorted or Reversed-Battery Protection**
- ♦ **-ΔV, Temperature, and Timer Fast-Charge Cutoff**
- ♦ **5µA Max Drain on Battery When Not Charging**
- ♦ **+5V Shunt Regulator Powers External Logic**
- ♦ **Supplies Load while Charging Battery**
- ♦ **16-Pin Narrow SO and DIP Packages**

Pin Configuration



Typical Operating Circuit



19-4507; Rev. 1; 3/92

EVALUATION KIT AVAILABLE

MAXIM

Battery-Powered Supply Systems

General Description

The MAX714/715/716 battery-powered supply systems combine multiple regulated voltage outputs with microprocessor supervisory functions that are optimized for battery-powered supplies. High-level integration and low-power CMOS simplify high-efficiency power-supply design in portable and battery-operated instruments.

The MAX716 combines circuitry for four low-dropout linear regulators, three DC-DC switching regulators, and power-supervisory functions on a single IC. All but one regulator output is logic controlled so that loads may be shut down to extend battery life. Linear-regulator outputs are pre-trimmed to +5V and operate with only 0.1V input-output differential. In addition, three DC-DC switching regulators generate a fixed negative output (-5V, -12V, or -15V), a software-adjustable negative output (-5V to -26V) to power LCD displays, and a positive boosted output voltage (+12 or +15). Other functions include backup-battery switchover, low-voltage warning, and power-fail reset.

The MAX716 is supplied in 28-pin plastic DIP and wide SO packages. The MAX715, in 24-pin narrow plastic DIP and CERDIP packages, eliminates one linear-regulator output. The MAX714, in 16-pin packages, includes two linear regulators and the LCD display DC-DC converter.

Applications

Portable Computers

Battery-Powered, Microprocessor-Based Systems

Handheld Instruments, Terminals

Bar-Code Readers

Remote Data-Acquisition Systems

Features

- ♦ **Four Logic-Controlled +5V Regulators**
- ♦ **Three Switching Regulators**
- ♦ **35µA Quiescent Current in Standby Mode**
- ♦ **100mV Dropout on Linear Regulators**
- ♦ **CMOS RAM Battery-Switchover Circuit**
- ♦ **Microprocessor Reset and Interrupt Outputs**
- ♦ **Hardware-On Signal**
- ♦ **Evaluation Kit Available – MAX716EVKIT**

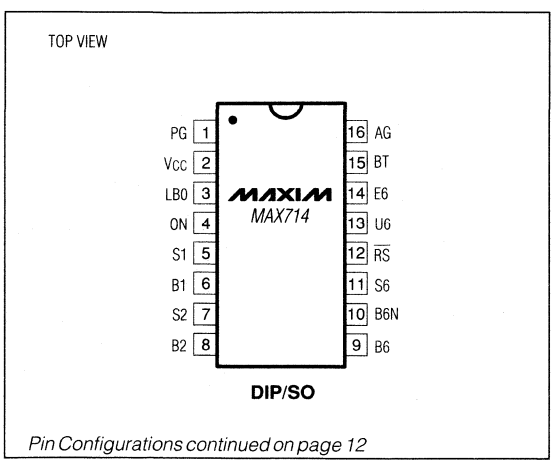
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX714CPE	0°C to +70°C	16 Plastic DIP
MAX714CWE	0°C to +70°C	16 Wide SO
MAX714C/D	0°C to +70°C	Dice*
MAX714EPE	-40°C to +85°C	16 Plastic DIP
MAX714EWE	-40°C to +85°C	16 Wide SO
MAX714MJE	-55°C to +125°C	16 CERDIP
MAX715CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX715CWG	0°C to +70°C	24 Wide SO
MAX715C/D	0°C to +70°C	Dice*
MAX715ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX715EWG	-40°C to +85°C	24 Wide SO
MAX715MRG	-55°C to +125°C	24 Narrow CERDIP

Ordering Information continued on page 12.

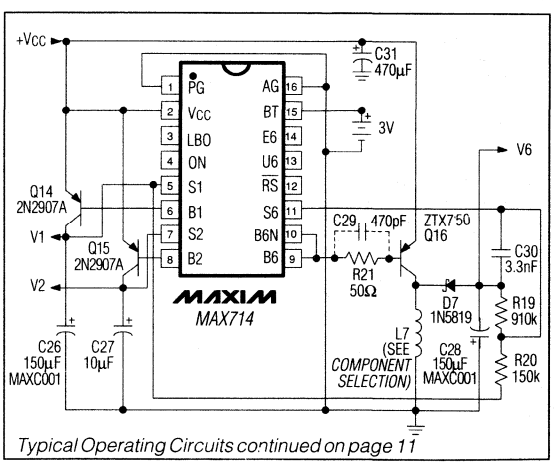
**Contact factory for dice specifications.*

Pin Configurations



Pin Configurations continued on page 12

Typical Operating Circuits



Typical Operating Circuits continued on page 11

Battery-Powered Supply Systems

ABSOLUTE MAXIMUM RATINGS

Input Supply Voltages
- V_{CC}, BT ..... -0.3V to +12V
- S1-S7, B1-B7, ON, E3-E7, U6 ..... -0.3V to the higher of V_{CC}+0.3V or BT+0.3
- LBO, $\overline{RS}$ ..... -0.3V to V1+0.3V

Maximum $\Delta V/\Delta T$ on V_{CC} 1V/µs
Maximum $\Delta V/\Delta T$ on BT ..... Infinite
Continuous Power Dissipation
- Plastic DIP
  - 16-Pin (derate 7.41mW/°C above +70°C) 593mW
  - 24-Pin Narrow (derate 8.7mW/°C above +70°C) .. 696mW
  - 28-Pin (derate 9.09mW/°C above +70°C) 727mW
- Wide SO
  - 16-Pin (derate 9.52mW/°C above +70°C) 762mW
  - 24-Pin (derate 11.76mW/°C above +70°C) 941mW
  - 28-Pin (derate 12.50mW/°C above +70°C) 1000mW
- CERDIP
  - 16-Pin (derate 10mW/°C above +70°C) 800mW
  - 24-Pin Narrow (derate 12.5mW/°C above +70°C) ... 1000mW
  - 28-Pin (derate 16.67mW/°C above +70°C) 1333mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AG = PG = 0V, V_{CC} = +5.05V to +11V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	Regulated output	5.05		11.00	V
Low Battery Indicator Threshold (Note 1)	LBO	MAX71_C_ _	5.05	5.16	5.27	V
Shutdown Voltage Range		MAX71_C_ _	4.81	4.92	5.05	V
Delta Between LB0 and $\overline{RS}$ (Note 1)		MAX71_C_ _	0.19	0.24	0.29	V
Low Battery Indicator Threshold (Note 1)	LBO	MAX71_E/M_ _	4.94	5.16	5.27	V
Shutdown Voltage Range		MAX71_E/M_ _	4.70	4.92	5.05	V
Delta Between LBO and $\overline{RS}$ (Note 1)		MAX71_E/M_ _	0.17	0.24	0.31	V
Battery Input	BT		2.3		4.0	V
Supply Current in Backup State		V_{CC} = 0V, BT = 3V, MAX71_C_ _		7	15	µA
		V_{CC} = 0V, BT = 3V, MAX71_E/M_ _		7	20	
Supply Current in Standby State (ON = 0V)		V_{CC} = 11V, BT = 3V		35	55	µA
Supply Current in Operating State (ON = V1)		V_{CC} = 11V, BT = 3V, V1 and V2 on only, I_{OUT} = 0µA		300	500	µA
$\overline{RS}$ Pulse Width			160	230	350	ms
V_{CC} to BT Power-Supply Switchover (Note 2)			-200		-50	mV
BT to V_{CC} Power-Supply Switchover (Note 2)			50		200	
BT Input Current (Note 3)		BT = 3V, V_{CC} = 5.05-11V	-1.00	0.01	1.00	µA
Digital Input Levels; ON, E3-E7, U6	V_{IH}		V1*0.7			V
	V_{IL}				V1*0.3	
	I_{IH}	Digital input current			5	µA
Digital Outputs; $\overline{RS}$, LB0	V_{OH}	I_{OUT} = -500µA	V1-0.5			V
	V_{OL}	I_{OUT} = 500µA			0.5	

ELECTRICAL CHARACTERISTICS (continued)

(AG = PG = 0V, V_{CC} = +5.05V to +11V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

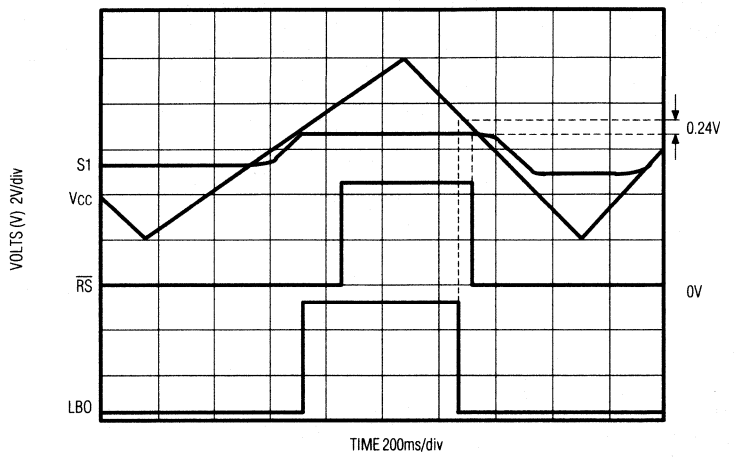
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LINEAR REGULATORS V1 - V4							
Output Voltage (Note 4)	V_{OUT}	5.05 < V_{CC} < 11		4.75		5.25	V
		V_{CC} = 5.05, I_{OUT} = 100mA		4.75		5.25	
Load Regulation (Note 4)		I_{OUT} = 1mA to 100mA, V_{CC} = 9V			35	100	mV
Line Regulation (Note 4)		V_{CC} = 5.05V to 11V, I_{OUT} = 1mA			20	100	mV
Additional Operating Supply Current when each V3, V4 Input is Enabled		V_{CC} = 11V			100	200	µA
Output Voltage Tracking Maximum Difference Between V1, V2, V3, V4		V_{CC} = 5.05V to 11V, I_{OUT} ≤ 100mA		-300		300	mV
B1-B4 Maximum Sink Capability		V_{CC} = 9V, B1-B4 = 5V		10	50	85	mA
B1 Sink Capability		During standby mode			100		µA
DC-DC CONVERTERS V5 - V7							
Additional Operating Supply Current when each V5, V6, V7 Input is Enabled		V_{CC} = 11V			125	200	µA
Extra Operating Supply Current when RC Oscillator Enabled (Note 5)		V_{CC} = 11V			225	300	µA
Oscillator Timing High Period Low Period	T_{ON} (Note 6)	V_{CC} = 5.5V, MAX71_C_ _		10.22	11.36	12.45	µs
		V_{CC} = 11V, MAX71_C_ _		4.56	5.70	6.84	
	T_{OFF}	V_{CC} = 5.5V to 11V, MAX71_C_ _		11.25	12.50	13.75	
Oscillator Timing High Period Low Period	T_{ON} (Note 6)	V_{CC} = 5.5V, MAX71_E/M_ _		9.09	11.36	13.63	µs
		V_{CC} = 11V, MAX71_E/M_ _		4.56	5.70	6.84	
	T_{OFF}	V_{CC} = 5.05V to 11V, MAX71_E/M_ _		10	12.50	15	
Input Leakage Current S5-S7		V_{CC} = 11V, S5-S7 = 1V		-1		1	µA
S5 Voltage		E5 = V1		-30		30	mV
S6 Voltage		E6 = V1, controlled by DAC	Code = 00000	-70		70	mV
			Code = 11111	1.18		1.32	V
S7 Voltage		E7 = V1		1.18	1.25	1.32	V
B5, B6, B7 Drive Voltages	V_{OL}	V_{CC} = 5.5V, I_{SINK} = 10mA			0.5	1.0	V
	V_{OH}	V_{CC} = 5.5V, I_{SOURCE} = 10mA		4.0	4.5		
Efficiency					85 (Note 7)		%

Note 1: Typical ramp rate 1V/ms.
Note 2: Tested with less than 1V/ms on V_{CC} and BT separately.
Note 3: To minimize test time, a larger max spec was chosen. The typical value indicates the mean value.
Note 4: A Motorola 2N2907A PNP was used as the output transistor in Figure 1.
Note 5: RC oscillator is enabled whenever any one of the DC-DC convertors is enabled.
Note 6: T_{ON} varies proportionally to 1/V_{CC}.
Note 7: The efficiency depends on external components and can be increased or decreased from this typical value.

Battery-Powered Supply Systems

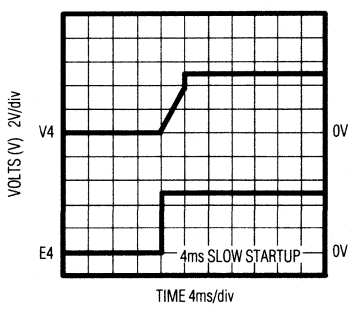
Typical Operating Characteristics

BACKUP-BATTERY SWITCHING AND WARNING FLAGS



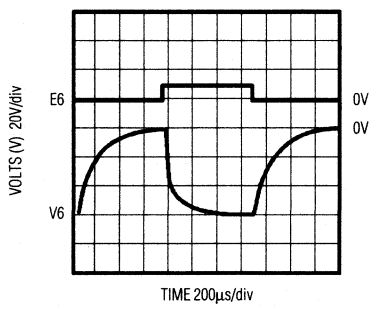
NOTE: THE BACKUP BATTERY IS AT 3V

REGULATOR 4 TURN-ON TIME



REGULATOR 4 V_{OUT} 0V TO +5V
WITH LOAD OF 390Ω AND 150µF

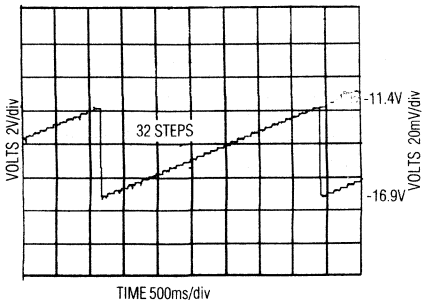
REGULATOR 7 TURN-ON TIME



REGULATOR V_{OUT} 0V TO -30V
I_{OUT} 0mA TO -30mA 10V/div

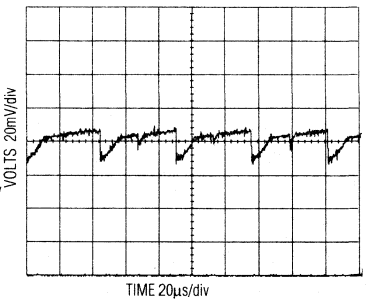
Typical Operating Characteristics (continued)

REGULATOR 7 V_{OUT} STEPPING



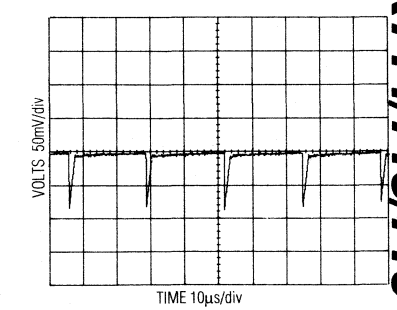
REGULATOR 7 V_{OUT} -11.4 TO -16.9 V WITH 10kΩ LOAD

REGULATOR 6 OUTPUT RIPPLE UNFILTERED



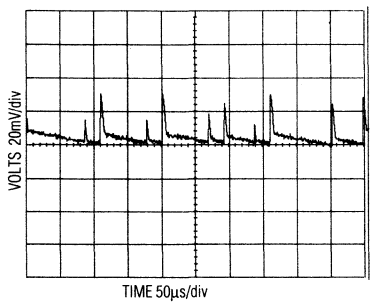
REGULATOR 6 V_{OUT} = -5V WITH 250Ω LOAD

REGULATOR 7 OUTPUT RIPPLE UNFILTERED



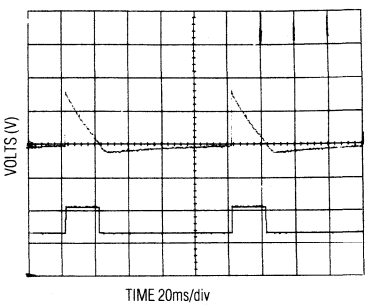
REGULATOR 7 V_{OUT} = -30V WITH 150kΩ LOAD

REGULATOR 8 OUTPUT RIPPLE UNFILTERED



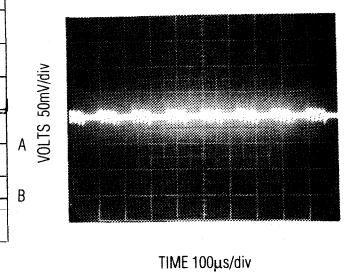
REGULATOR 8 V_{OUT} = +15V WITH 1.5kΩ LOAD

V2 LINE TRANSIENT RESPONSE



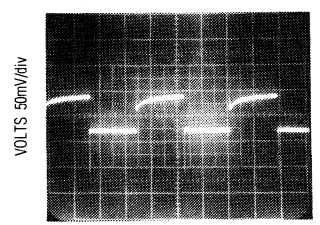
A = V2 VOLTAGE OUT .2V/div
B = LINE TRANSIENT SWITCH 5V/div

V5 LOAD-TRANSIENT RESPONSE



0mA TO -40mA LOAD
V_{CC} = +9V, V_{OUT} = -5V
ZTX749 OUTPUT TRANSISTOR

V4 LOAD-TRANSIENT/DROPOUT RESPONSE



0mA TO 100mA LOAD
V_{CC} = +9V, V_{OUT} = -5V
2N2907 OUTPUT TRANSISTOR

Battery-Powered Supply Systems

Pin Description

MAX714 PIN	MAX715 PIN	MAX716 PIN	NAME	FUNCTION
15	1	1	BT	Backup-Battery Input
16	2	2	AG	Analog Ground
1	3	3	PG	High-Power Ground
2	4	4	V_{CC}	Main Supply Input: +5.05V to +11V
3	5	5	LBO	Low Battery Warning Output. High when V_{CC} > 5.16V.
4	6	6	ON	Hardware-On Input. Logic-high level activates V2-V7. V1 is always on.
–	–	7	S4	V4, Feedback-Sense Input
–	–	8	B4	V4, Base drive for linear regulator output transistor
5	7	9	S1	V1, Feedback-Sense Input
6	8	10	B1	V1, Base drive for linear regulator output transistor
7	9	11	S2	V2, Feedback-Sense Input
8	10	12	B2	V2, Base drive for linear regulator output transistor
–	11	13	B3	V3, Base drive for linear regulator output transistor
–	12	14	S3	V3, Feedback-Sense Input
–	13	15	B5	V5, Base drive for the inverting output transistor
–	14	16	S5	V5, Feedback-Sense Input
9	15	17	B6	V6, Base drive for LCD inverting output transistor (MAX714 - B6P)
10	–	–	B6N	V6, MAX714 only
11	16	18	S6	V6, Feedback-Sense Input – for adjustable (LCD) switching regulator
–	17	19	B7	V7, Base-/Gate-Drive Output – step-up switching transistor/MOSFET
–	18	20	S7	V7, Feedback-Sense Input – step-up switching regulator
12	19	21	$\overline{RS}$	$\overline{Reset}$ Output – low during power-up, battery-backup, and standby states
–	20	22	E3	V3, Enable Input
–	–	23	N.C.	No Connect
–	–	24	E4	V4, Enable Input
13	21	25	U6	Pulsing this input increments V6 negative output
–	22	26	E5	V5, Enable Input
14	23	27	E6	V6, Enable Input
–	24	28	E7	V7, Enable Input

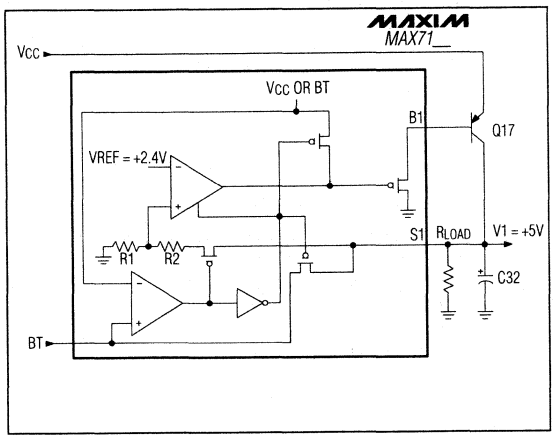


Figure 1. Functional Diagram and Circuit for Linear Regulator V1

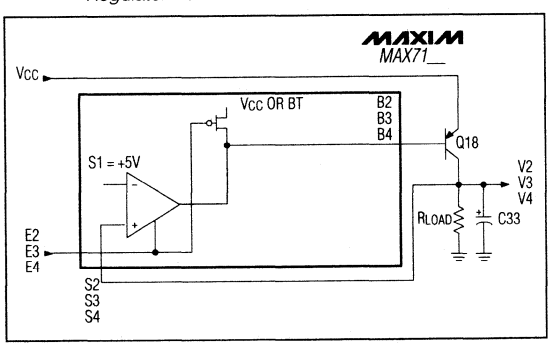


Figure 2. Functional Diagram and Circuit for Linear Regulators V2-V4

Detailed Description

External PNP pass transistors provide low-dropout linear outputs while minimizing regulator interaction and maximizing line and load rejection. The switching regulators employ external switching transisitors to maximize efficiency at low input voltages.

DC-DC convertor output current is primarily determined by the selected inductors and transistors. Inductors and transistors for several voltage and current outputs are listed in Table 1.

A "speed-up" capacitor (C29) (see *Typical Operating Characteristics*, page 1) appears in dotted lines across the base resistor of the DC-DC converter's output transistor. This capacitor reduces switching time and increases efficiency by about 2%. It may be omitted if efficiency improvement is not needed. Linear-regulator (V1-V4) output current is determined by the current capability of the selected output PNP pass transistors. The 2N2907A transistors in Figure 1 can provide load currents up to approximately 600mA.

TABLE 1: COMPONENT SELECTION

REGULATOR	TRANSISTOR	INDUCTOR*	V_{OUT} (V)	I_{OUT} (mA)
V5	2N2907A	470µH CB 7070-33	-5	-30
V5	2N2907A	390µH CB 7070-32	-5	-36
V5	ZTX750	100µH CB 7070-25	-5	-100
V6	2N2907A	220µH CB 7070-29	-18	-17
V6	ZTX750	82µH CB 7070-24	-26	-30
V6	ZTX750	100µH CTX100-3	-26	-28
V7	2N2222A	470µH CB 7070-33	15	14
V7	2N2222A	220µH CB 7070-29	15	30

* CB = Caddell-Burns, CTX = Coiltronics, ZTX = Zetex

The Caddell-Burns (CB) inductors are ferrite-bobbin cylindrical coils and the Coiltronics (CTX) is a surface-mount toroidal inductor.

Linear Regulators

Linear-regulator output current is a function of the selected PNP pass transistors. As the input voltage rises, power dissipation in the transistor limits the safe output current. Very little power is dissipated in the MAX714/715/716 devices, but each transistor must dissipate (V_{CC}-V_{OUT}) x I_{OUT}. Consult the pass-transistor data sheets for power-dissipation and thermal-resistance limits.

To maintain stability, 10µF output capacitors are required at the V2-V4 linear regulator outputs. 150µF is recommended at V1, as it serves as the V2-V4 reference, and V1 output ripple may feed through to other regulator outputs.

For V2-V4, use these minimum capacitor values:

I_{LOAD} 500mA – 100µF
I_{LOAD} 50mA – 10µF

Outputs B1-B4 drive the bases of external PNP pass transistors and sink a minimum of 10mA. The output voltage at the collector of the external PNP transistor is sensed at S1-S4 to maintain regulation. When an output is turned off, the base-drive output rises to V_{CC} (or BT whichever is higher), turning off the pass transistor.

Short-circuit current limiting and thermal shutdown are not implemented in the regulator outputs. Consequently,

Battery-Powered Supply Systems

short-circuit current is limited only by the maximum B1-B4 sink current (85mA) and the transistor current gain (beta).

During standby, when the ON input is low or V_{CC} < 4.95V, B1 is limited to 100µA to reduce power consumption during dropout (dropout occurs when V_{CC} falls below 5V). During start-up, V2-V4 base currents limit at approximately 0.5mA for about 4ms to prevent large load-current transients. The external PNP transistors should have betas above 100 and f_t above 200MHz. Typical transistors are 2N2907A and 2N3905.

All 5V outputs have a tolerance of ±5% over the specified V_{CC} input voltage, output current, and temperature ranges. V1 serves as the reference for all other 5V outputs to maintain optimum tracking between outputs.

Switching Regulators

Inverters

Figures 3 and 4 show typical operating circuits for the V5 and V6 inverting regulators. V5's feedback input (S5) is kept at 0V in regulator 5. In regulator 6, S6 is digitally adjusted from 0V to +1.25V, providing a variable negative supply for LCD power.

When V5 (Figure 3) becomes less negative than the level set by the R23 and R24 resistor dividers, B5 toggles at the oscillator frequency (f_{OSC} varies with V_{CC}; see *Electrical Characteristics*), turning on Q19 when B5 is low. When Q19 turns on, current increases in the L8 inductor, storing energy in its magnetic field. When Q19 is off, current flows through L8 in the same direction, flowing from C35 through D8, making V5 more negative. As inductor energy is transferred to C35, the inductor current decays linearly to zero and its magnetic field collapses. V6 (Figure 4) operates similarly to V5, except its output is varied by a digital input signal at V6.

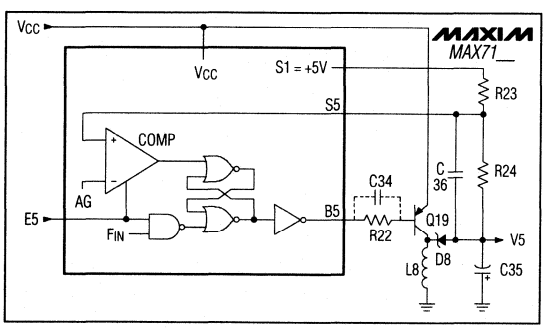


Figure 3. Functional Diagram and Circuit for DC-DC Converter V5

The B5 and B6 outputs are suitable for driving external PNP or logic-level P-channel MOSFET switching transistors (such as the Siliconix SMD10PO5L); however, PNP transistors are less expensive for input voltages below 7V. Likewise, the B7 output can drive a logic-level N-channel MOSFET such as the Siliconix Si9956DY.

The output voltages of V5 and V6 are set by these equations:

$$R24 = -V5 \times (R23/5)$$
$$R27 = -R26 \times (V6\text{-}V_{TH})/(5\text{-}V_{TH}),\ V_{TH} = 0V \text{ to } +1.25V$$

The V6 output (Figure 4) is generated in the same fashion as V5, except that the S6 threshold can be varied from 0V to +1.25V with an internal 5-bit (32 step) DAC. The DAC is incremented by pulsing U6 and can only be incremented in one direction (more negative). To reduce the voltage (less negative), the DAC must loop completely around; to decrement by one step, U6 must be clocked 31 times. The DAC is set to 0V during standby and whenever V6 is turned off.

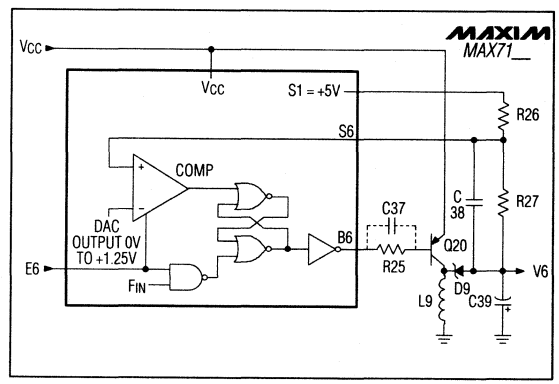


Figure 4. Functional Diagram and Circuit for DC-DC Converter V6

V6's output voltage range is set by an external resistor divider connected between V1 (used as a reference) and V6 (see Table 2). A good typical value for R26 is 150kΩ. The ratio of the resistors to each other sets the voltage ranges as follows. Choose the high value to be within the absolute maximum of the display.

TABLE 2: V6 (LCD POWER) VOLTAGE RANGE

R27/R26 RATIO	V6 OUTPUT VOLTAGE RANGE (V)
6:1	-30 to -21.3
5:1	-25 to -17.5
4:1	-20 to -13.8
3:1	-15 to -10
2:1	-10 to -6.3
1:1	-5 to -2.5

Step-Up Converter

Regulator V7 operates similiarly to V5, except that it steps up rather than inverts. In Figure 5, the feedback input (S7) is kept at 1.25V. B7 swings from 0V to V_{CC}, and can drive either the gate of an N-channel power MOSFET or the base of an NPN transistor. When V7 is at the desired voltage, B7 remains low, keeping Q21 off. When V7 falls below the preset level, B7 switches Q21 on and off at the clock frequency. When Q21 turns off, inductor current flows through D10 into C41, and V_{OUT} rises. R30 is set by:

$$R30 = R29 \times 1.25/(V7-1.25)$$

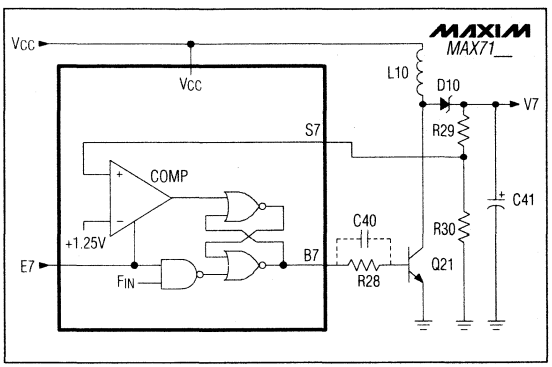


Figure 5. Functional Diagram and Circuit for DC-DC Converter V7

Switching Frequency and Soft Start

The switching frequency is set by an internal oscillator. The oscillator high period (switch-on time) is inversely proportional to V_{CC} and peak inductor current remains constant over variations in input voltage. The high period is typically 11.36µs with V_{CC} = 5.5V, and 5.7µs with V_{CC} = 11V. The low period (off time) is typically 12.5µs and is independent of V_{CC}.

A soft-start circuit limits the oscillator duty cycle at start-up by enabling the switch during every 8th oscillator cycle only. The soft-start duration is approximately 4ms. This prevents large current drain at turn-on.

Board Layout and Grounding

Since the V5-V7 DC-DC converters use feedback control circuitry, it is important to minimize the lengths of GND connections and feedback points. Minimize the size of the connections between S5, S6, S7, and the respective resistors, and place the transistors' output bases as close as possible to the respective B5, B6, and B7 base pins. The traces connecting the V_{CC} pins to the input capacitor (C28 or C31 in *Typical Operating Circuits*) must be separate from the high current traces of the linear switching circuits.

Switching-Regulator Components

Inductor Selection

The output power of each switching regulator depends on the selected inductor and switching transistor. Table 1 lists components for two ranges of output current (see *Typical Operating Characteristics*). Other inductor types may also be used, but be sure to observe their peak current ratings.

For the output power levels given in Table 1, Caddell-Burns 7070 inductors were used. However, smaller size inductors may be used in low output-current applications. In general, higher internal resistance and lower current ratings reduce efficiency and increase the chance of inductor saturation. Be sure to observe the manufacturer's ratings on substitute coils. Coiltronics produces surface-mount inductors that have relatively high-power capacity compared to their size. For alternate output voltage, current values, or coil selection, contact Maxim's applications department.

Coil saturation is the most likely cause of poor efficiency, overheating, and component damage in switching-regulator circuits. Test for saturation by applying the maximum load over the full input voltage range while monitoring the inductor current with a current probe. The normal inductor-current waveform is a sawtooth with a linear increase and decrease of current. Saturation creates a nonlinear current waveform where current slope increases as the current level rises.

Capacitor Selection

The V5-V7 output ripple contains two elements. One is the result of change in the stored charge on the filter capacitor with each current pulse. The other element is the effect of the capacitor's charge/discharge current and its equivalent series resistance (ESR). With low-cost aluminum electrolytic capacitors, ESR-produced ripple may sometimes be greater than that caused by the change in charge. Consequently, high-quality aluminum or tantalum filter capacitors minimize output ripple, even when smaller capacitance values are used. Best results at reasonable cost are achieved with a high-quality aluminum electrolytic capacitor in parallel with a 0.1µF ceramic capacitor. For V5-V7, the MAXC001 or equivalent capacitor is recommended for an output filter.

The Typical Operating Circuit on page 11 shows capacitors C8-C10 as dashed lines connected in parallel with the base resistors of transistors Q5-Q7. These capacitors improve efficiency by about 2% by reducing switching time, but can be omitted if component count is critical.

Battery-Powered Supply Systems

Rectifier Selection

Since the current in the external rectifiers switches abruptly, they must have a fast turn-on time to minimize losses. For low-power circuits with peak inductor currents less than 100mA, signal diodes such as 1N4148s perform well. In higher-power applications, or for maximum efficiency at low power, Schottky rectifiers are recommended. Although 1N4001s and other general-purpose rectifiers are rated for high currents, they are unacceptable because their slow turn-on times result in excessive losses. Since Schottky rectifiers tend to have limited breakdown voltage, be careful to observe this limit, especially in the V6 and V7 inverting regulators. When the switch turns on, the voltage at the inductor-diode junction is pulled to V_{CC}. When the switch turns off, this junction "flies back" to the negative output. If the V7 output is -26V, the diode reverse voltage is +11V - (-26V), or +37V, which is why the higher rated (40V) 1N5819 is used.

System Operating Modes

There are three system operating modes:

Battery Backup
Standby
Operating

Battery-Backup Mode

In battery-backup mode, V1 provides a low current output to maintain CMOS RAM and/or a real-time clock. The input to V1 is supplied by the backup battery when V_{CC} is less than the backup-battery voltage. This will happen when the main battery is discharged, the line power switch is disconnected, or the main battery is being replaced. Battery-backup mode is entered whenever the voltage at BT is higher than V_{CC}. Supply current in this state is less than 15µA maximum with a 3V backup-battery voltage.

In battery-backup mode:

1) V1 connects to BT via an internal 500Ω switch.
2) All other outputs (V2-V7) turn off.
3) S2-S4 connect to GND via internal 5kΩ resistors.
4) ON and $\overline{RS}$ outputs are low.
5) All digital inputs are ignored. The allowed digital input range is 0V to V1.

Changing Batteries

The V1 regulator picks the higher of either V_{CC} or BT. Either the main battery (at V_{CC}) or the backup battery (but not both) may be removed without loss of backup power. The V_{CC} rate-of-rise must be limited to 1V/µs during power-up. The BT rate-of-rise need not be controlled.

The BT input must be connected to GND if a backup battery is not used. If BT is left unconnected, leakage currents may raise the BT-terminal voltage to a level that causes erroneous switchover to the battery backup. The BT input range is 2.3V to 4.0V. BT voltage above 4V may damage external transistors.

Standby Mode

Standby is entered from the operating mode when the ON input is low. The purpose of standby is to minimize power consumption between periods of normal operation. The MAX714/715/716 also enter standby if V_{CC} falls to approximately 4.95V (4.70V min). Operating circuitry must be shut down by the system processor before standby is entered; this prevents data loss that might result from power supplies turning off without warning. The low battery output provides early warning so that data can be saved.

In standby mode:

1) V1 = 5V (or V_{CC}, whichever is lower).
2) B1 output current is limited to 100µA typ.
3) V2-V7 are off.

Standby mode is also entered from the battery-backup mode whenever V_{CC} rises above BT.

The MAX714/715/716 power up in standby mode. The V1 output current is limited to 100µA times the beta of the pass transistor. If V1's load current is too high on power-up, there may be insufficient output current to regulate at 5V. For a transistor beta of 200, the load on V1 during power-up should be no more than 20mA.

Operating Mode

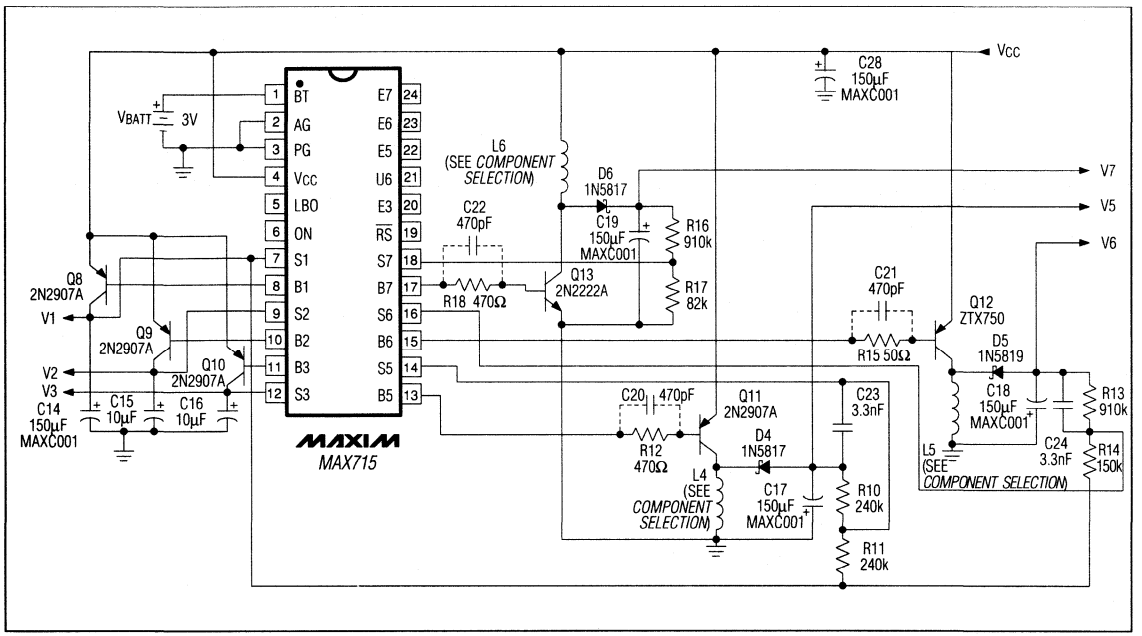
Operating mode is entered from standby by driving the ON input high. V_{CC} MUST be above the low battery warning threshold to enter the operating mode. V2 turns on, but the other regulators (V3-V7) are controlled by E3-E7 regulator enable inputs.

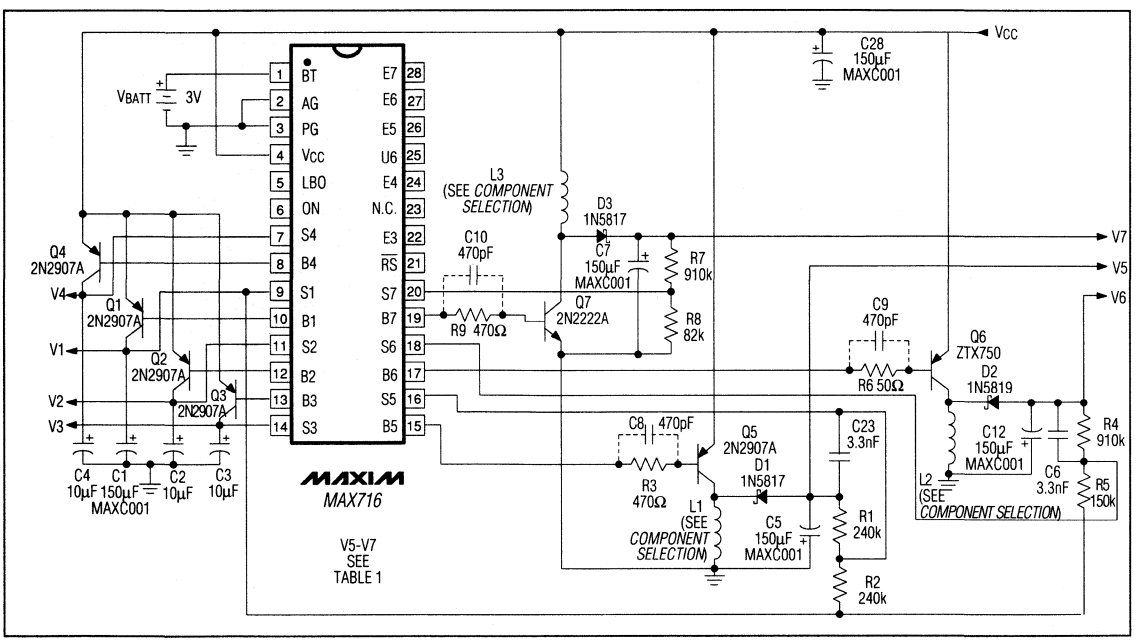
LBO Warning and $\overline{RS}$ Outputs

The low battery output (LBO) is normally a logic high (the V1 voltage). When V_{CC} falls to approximately 5.16V, LBO goes low. In a typical application, LBO drives the nonmaskable interrupt ($\overline{NMI}$) input of a microprocessor (µP). When LBO goes low, the µP should perform an orderly shutdown of the system, including turning off all MAX714/715/716 regulators. This shutdown should be completed before V_{CC} falls more than 240mV below the low-battery warning threshold. When V_{CC} falls to approximately 4.92V, standby mode begins whether or not standby has been commanded by the µP. All supplies except V1 are turned off.

$\overline{RS}$ goes low during battery-backup and standby modes. It remains low for approximately 230ms after the ON input rises, and V_{CC} is above the warning threshold.

Typical Operating Circuits (continued)

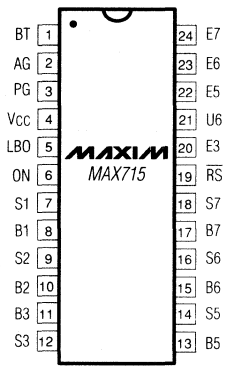




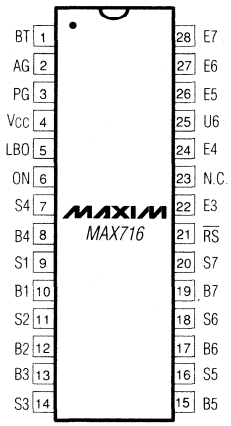
Battery-Powered Supply Systems

Pin Configurations (continued)

TOP VIEW



DIP/SO



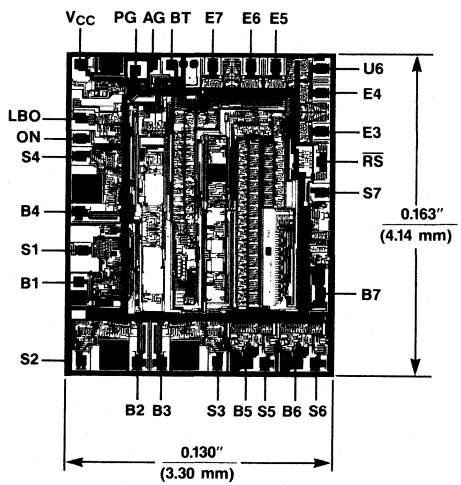
DIP/SO

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX716CPI	0°C to +70°C	28 Plastic DIP
MAX716CWI	0°C to +70°C	28 Wide SO
MAX716C/D	0°C to +70°C	Dice*
MAX716EPI	-40°C to +85°C	28 Plastic DIP
MAX716EWI	-40°C to +85°C	28 Wide SO
MAX716MJI	-55°C to +125°C	28 CERDIP
MAX716EVKIT	Evaluation Kit	

**Contact factory for dice specifications.*

Chip Topography



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

EVALUATION KIT AVAILABLE

MAXIM

Palmtop Computer and Flash Memory Power-Supply Regulators

General Description

The MAX717-MAX721 CMOS power-supply ICs create dual, regulated DC outputs for small, battery-operated microprocessor systems. Each device generates a main output (3V or 5V, selectable) and an auxiliary output for flash memory or PCMCIA (5V or 12V, selectable). Each device accepts up to three input voltages. Power can come from a main battery (two or three alkaline or NiCad), a lithium backup battery, or an unregulated DC source such as an AC-DC wall adapter.

The MAX717-MAX721 provide three improvements over prior-art devices. Physical size is reduced – the high switching frequencies (up to 0.5MHz) made possible by MOSFET power transistors allow for tiny (<5mm diameter) surface-mount magnetics. Efficiency is improved to 87% (10% better than with low-voltage regulators made in bipolar technology). And supply current is reduced to 60µA by CMOS construction and a unique constant-off-time pulse-frequency modulation (PFM) control scheme.

The MAX717-MAX721 differ only in shutdown and status functions and in the choice of a 3.0V or 3.3V main output (see *Device Options*).

For LCD-bias applications requiring an adjustable negative voltage, refer to the MAX722/MAX723 data sheet.

Applications

Palmtop Computers

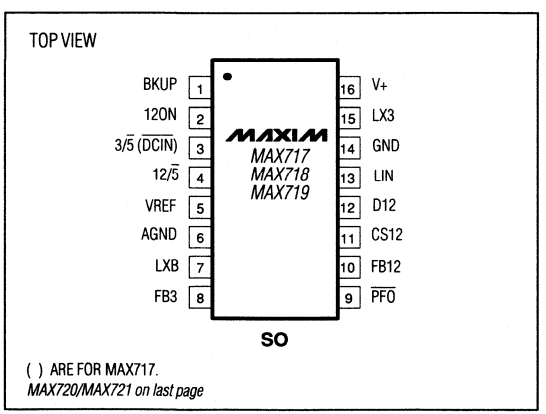
Flash-Memory/PCMCIA Power Supplies

Portable Data-Collection Equipment

Medical Instrumentation

Portable Data Communicators

Pin Configurations



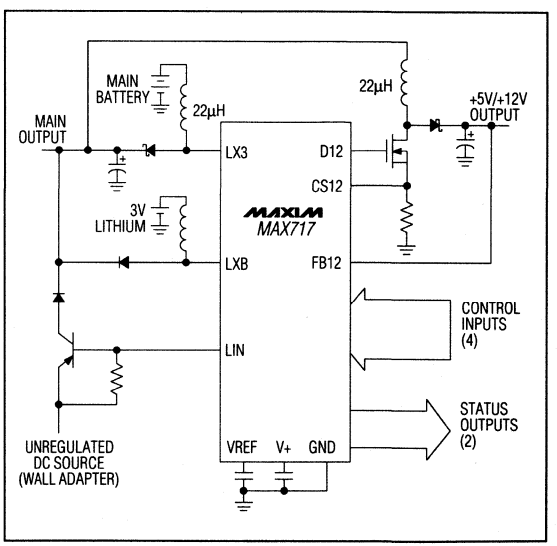
( ) ARE FOR MAX717.

MAX720/MAX721 on last page

Features

- ♦ **Low 0.9V to 5.5V Battery Operating Range**
- ♦ **Unregulated 7V to 20V DC Input Range**
- ♦ **Dual Regulated Outputs**
  Main Output: 3.3V/5V
  Auxiliary Output: 5V/12V
- ♦ **87% Efficiency at 200mA**
- ♦ **Efficiency PRAM Keep-Alive: 80% at 1mA**
- ♦ **8W/in^3 Power Density**
- ♦ **60µA Quiescent Current**
- ♦ **20µA Shutdown Mode with VREF Alive (MAX720/MAX721 only)**
- ♦ **500kHz Maximum Switching Frequency**
- ♦ **±1.5% VREF Tolerance Over Temp**
- ♦ **Detect Output Power Failures**
- ♦ **Detect Presence of AC Power**
- ♦ **16-Pin Narrow SO Packages**

Typical Operating Circuit



19-0040; Rev 0; 6/92

EV KIT MANUAL FOLLOWS DATA SHEET

MAXIM

Palmtop Computer and LCD Power-Supply Regulators

General Description

The MAX722 and MAX723 CMOS power-supply ICs create dual regulated DC outputs for small, battery-operated microprocessor systems. Each device generates a main output (3V or 5V, selectable) and a negative auxiliary output that is adjustable for LCDs. Each device accepts two input voltages. Power can come from a main battery (two or three alkaline or NiCad), or an unregulated DC source such as an AC-DC wall adapter.

The MAX722/MAX723 provide three improvements over prior-art devices. Physical size is reduced; the high switching frequencies (up to 0.5MHz), made possible by MOSFET power transistors, allow for tiny (<5mm diameter) surface-mount magnetics. Efficiency is also improved to 87% (10% better than with low-voltage regulators made in bipolar technology). And supply current is reduced to 60µA by CMOS construction and a unique constant-off-time pulse-frequency modulation (PFM) control scheme.

The MAX722 and MAX723 differ only in the lower fixed output voltage of the main regulator, with a 3.3V output for the MAX722 and a 3.0V output for the MAX723.

For flash memory or PCMCIA applications that require a +12V output voltage, refer to the MAX717-721 data sheet.

Applications

Palmtop Computers

LCD Contrast Control

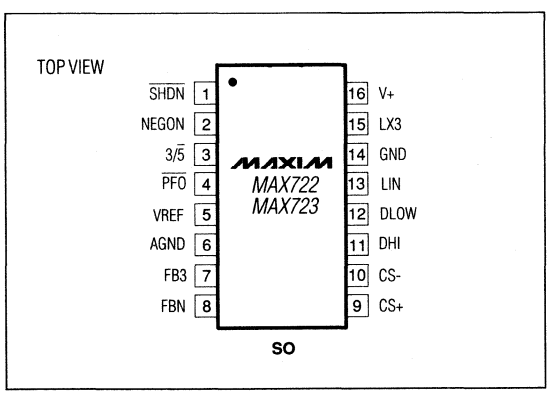
Portable Data-Collection Equipment

Portable Data Communicators

Medical Instrumentation

Bar-Code Scanners

Pin Configuration



Features

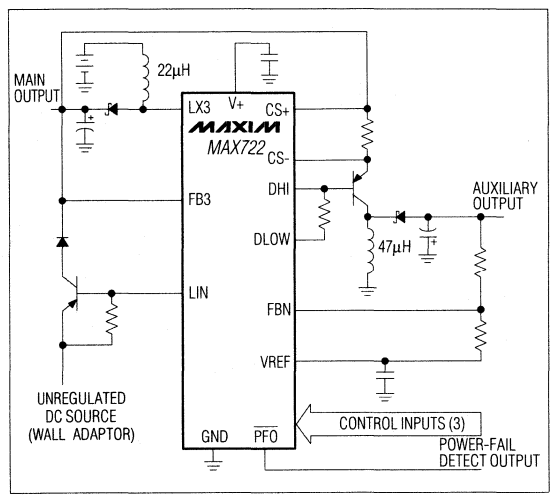
- ♦ **Low 0.9V to 5.5V Battery Input Range**
- ♦ **Unregulated 7V to 20V DC Input Range**
- ♦ **Dual Regulated Outputs**
  Main Output: 3.3V/5V
  Auxiliary Output: 0V to -100V
- ♦ **87% Efficiency at 200mA**
- ♦ **Efficient PRAM Keep-Alive: 80% at 1mA**
- ♦ **8W/in^3 Power Density**
- ♦ **60µA Quiescent Current**
- ♦ **20µA Shutdown Mode with VREF Alive**
- ♦ **500kHz Maximum Switching Frequency**
- ♦ **±1.5% VREF Tolerance (Over Temp.)**
- ♦ **Detect Output Power Failures**
- ♦ **16-Pin Narrow SO Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX722CSE	0°C to +70°C	16 Narrow SO
MAX722C/D	0°C to +70°C	Dice*
MAX722ESE	-40°C to +85°C	16 Narrow SO
MAX723CSE	0°C to +70°C	16 Narrow SO
MAX723C/D	0°C to +70°C	Dice*
MAX723ESE	-40°C to +85°C	16 Narrow SO
MAX722EVKIT-SO	0°C to +70°C	Evaluation Kit-Surface Mount

*Contact factory for dice specifications.

Typical Operating Circuit



Palmtop Computer and LCD Power-Supply Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND) ..... +7V, -0.3V
Switch Voltage (LX3 to GND) ..... +7V, -0.3V
Linear Regulator Voltage (LIN to GND) ..... +20V, -0.3V
Auxiliary Pin Voltages
(NEGON, FB3, 3/5, $\overline{SHDN}$, FBN, DHI, DLOW, VREF, PFO, CS+, CS- to GND) ..... -0.3V to (V+ + 0.3V)
Ground Voltage Difference (AGND to GND) ..... ±0.3V
Feedback Input Current (FBN) ..... ±10mA
Reference Current (I_{VREF}) 2.5mA

Continuous Power Dissipation (T_A = +70°C)
Narrow SO (derate 8.70mW/°C above +70°C) 696mW
Operating Temperature Ranges:
MAX72_C_ ..... 0°C to +70°C
MAX72_ESE ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, VBATT1 = VBATT2 = 2.5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Main Output Voltage – Main SMPS Mode	2V < VBATT1 < 3V, 0mA < I_{LOAD} < 200mA, DC SOURCE = 0V (Note 1)	3/$\overline{5}$ = 3V	MAX722	3.17	3.3	3.43	V
			MAX723	2.88	3.0	3.12	
		3/$\overline{5}$ = 0V		4.8	5.0	5.2	
Main Output Voltage – Linear-Regulator Mode	7V < DC SOURCE < 18V, 0mA < I_{LOAD} < 500mA	3/$\overline{5}$ = 3V	MAX722	3.17	3.3	3.43	V
			MAX723	2.88	3.0	3.12	
		3/$\overline{5}$ = 0V		4.8	5.0	5.2	
Auxiliary Output Voltage	2V < VBATT2 < 5V, VBATT1 = 2.5V, External Reference = 3V, R4 = 170k, R5 = 30k, 0mA < I_{LOAD} < 5mA			-18	-17	-16	V
FBN Input Offset Voltage	3/$\overline{5}$ = 0V or 3V				±2	±20	mV
FBN Input Bias Current	FBN forced to 0V				-5	±100	nA
Minimum Start-Up Supply Voltage (VBATT1)	I_{LOAD} = 0mA				0.85		V
Minimum Start-Up Supply Voltage (DCSOURCE)					7.3	7.6	V
Current-Sense Limit Threshold	Measured at CS+, CS-			170	200	230	mV
DHI Source Current	3/$\overline{5}$ = 3V				50		mA
DLOW On Resistance	3/$\overline{5}$ = 3V				5		Ω
Quiescent Supply Current from $3V_{OUT}$ (Note 2)	NEGON = 0V, 3/$\overline{5}$ = 3V, FB3 forced to 3.47V (MAX722) FB3 forced to 3.15V (MAX723)					60	µA
Battery Quiescent Current (VBATT1 + VBATT2)	NEGON = 0V, 3/$\overline{5}$ = 3V				60		µA
Shutdown Battery Current	NEGON = 0V, 3/$\overline{5}$ = 3V, $\overline{SHDN}$ = 0V				20	40	µA
Battery Quiescent Current – Linear-Regulator Mode	DC SOURCE = 7V, 3/$\overline{5}$ = 0V, measured at VBATT1			-10		10	µA
Linear-Regulator Output Sink Current	LIN = 6V, 3/$\overline{5}$ = 3V, measured at LIN			20	50		mA
Reference Voltage	No VREF load			1.23	1.25	1.27	V
Reference Load Regulation	3/$\overline{5}$ = 3V, -20µA < REF load < 250µA	T_A = +25°C			10	20	mV
		T_A = T_{MIN} to T_{MAX}				25	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, VBATT1 = VBATT2 = 2.5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Fail Threshold	3/$\overline{5}$ = 0V or 3V, falling edge, referred to no-load output voltage	-4	-6	-8	%
Power-Fail Hysteresis	3/$\overline{5}$ = 0V or 3V		2		%
$\overline{PFO}$ Output Voltage Low	I_{SINK} = 2mA, 3/$\overline{5}$ = NEGON = 0V			0.4	V
$\overline{PFO}$ Output Current High	$\overline{PFO}$ = 4.8V, 3/$\overline{5}$ = 0V			1	µA
Logic Input Voltage Low	Measured at NEGON, $\overline{SHDN}$, 3/$\overline{5}$			0.4	V
Logic Input Voltage High	Measured at NEGON, $\overline{SHDN}$, 3/$\overline{5}$	1.6			V
Logic Input Current				±100	nA

Note 1: The main SMPS output voltage at full load current is guaranteed by measuring LX3 switch on resistance and peak current limit threshold.

Note 2: Supply current from $3V_{OUT}$ is measured with an ammeter between the main output $3V_{OUT}$ and FB3. This current correlates directly with actual battery supply current, but is reduced in value according to the step-up ratio and efficiency.

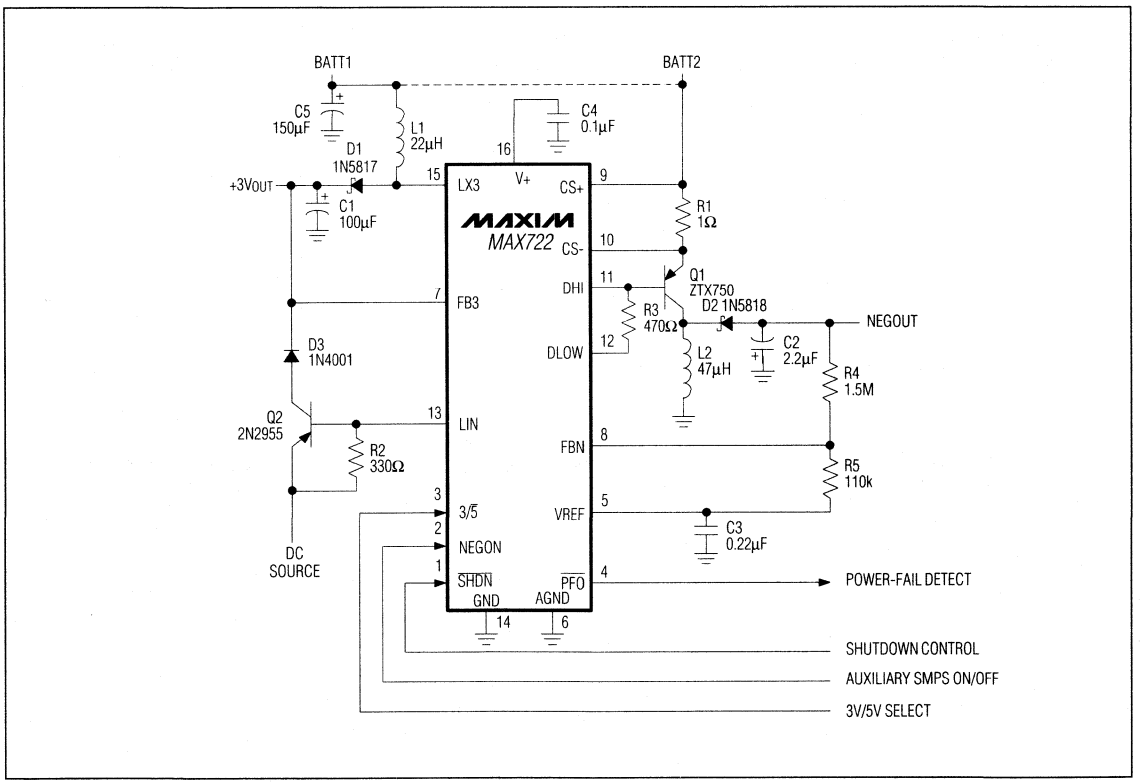
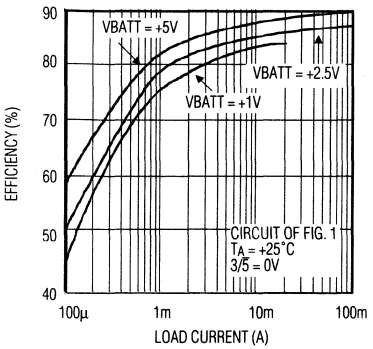


Figure 1. Standard Application Circuit

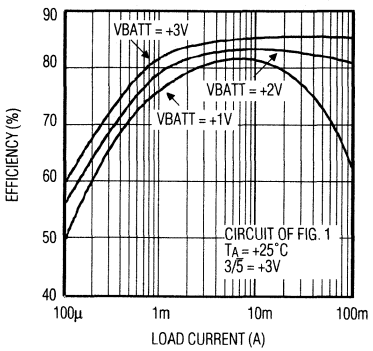
Palmtop Computer and LCD Power-Supply Regulators

Typical Operating Characteristics

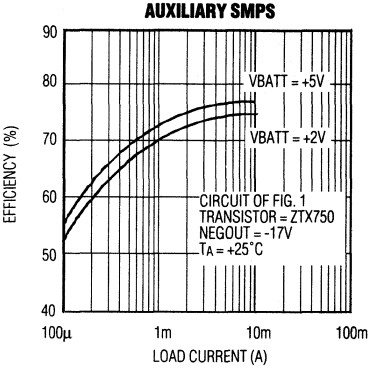
EFFICIENCY vs. LOAD CURRENT, MAIN SMPS IN 5V MODE



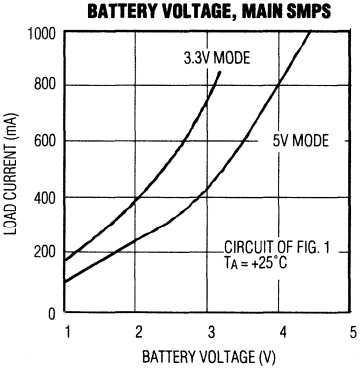
EFFICIENCY vs. LOAD CURRENT, MAIN SMPS IN 3.3V MODE



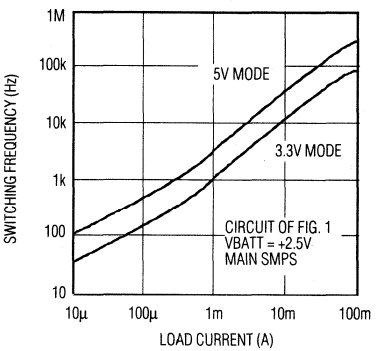
EFFICIENCY vs. LOAD CURRENT, AUXILIARY SMPS



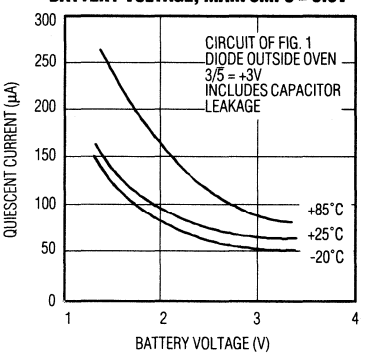
LOAD CURRENT CAPABILITY vs. BATTERY VOLTAGE, MAIN SMPS



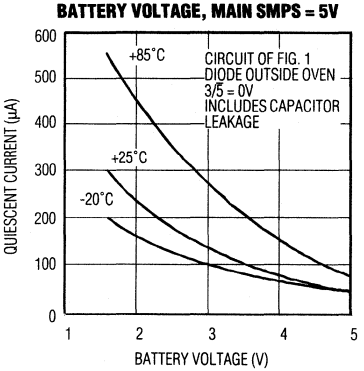
SWITCHING FREQUENCY vs. LOAD CURRENT



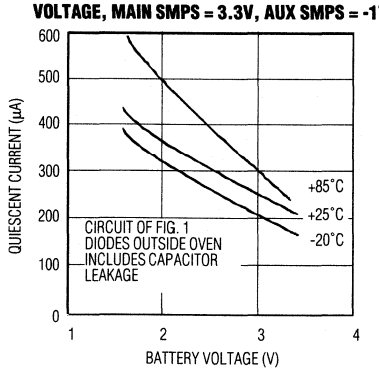
BATTERY QUIESCENT CURRENT vs. BATTERY VOLTAGE, MAIN SMPS = 3.3V



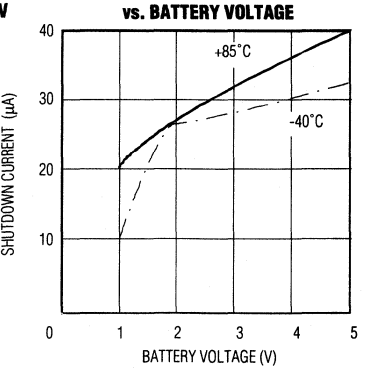
BATTERY QUIESCENT CURRENT vs. BATTERY VOLTAGE, MAIN SMPS = 5V



BATTERY QUIESCENT CURRENT vs. BATTERY VOLTAGE, MAIN SMPS = 3.3V, AUX SMPS = -17V

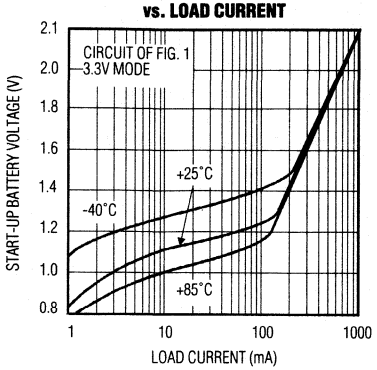


SHUTDOWN BATTERY CURRENT vs. BATTERY VOLTAGE

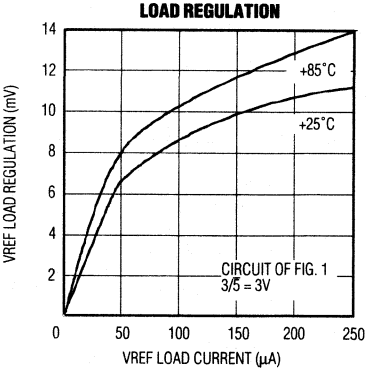


Typical Operating Characteristics (continued)

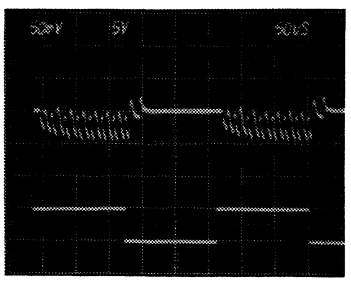
START-UP BATTERY VOLTAGE vs. LOAD CURRENT



REFERENCE VOLTAGE LOAD REGULATION



MAIN SMPS LOAD-TRANSTENT RESPONSE

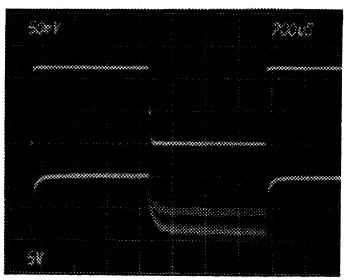


A = OUTPUT VOLTAGE, 50mV/div

B = LOAD CURRENT, 0mA TO 200mA

VBATT = 2.5V
HORIZONTAL = 50µs/div
3/5 = 0V

DC-SOURCE SWITCHOVER – SMPS TO LINEAR

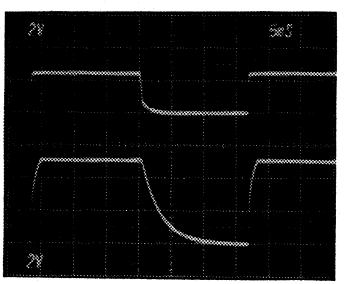


A = DC SOURCE, 0V to +12V

B = OUTPUT VOLTAGE, 50mV/div

I_{LOAD} = 200mA
HORIZONTAL = 200µs/div
3/5 = 0V

MAIN SMPS START-UP DELAY TIME



A = BATTERY VOLTAGE, 0V TO 2.5V

B = OUTPUT VOLTAGE, 2V/div

I_{LOAD} = 100mA
HORIZONTAL = 5ms/div
3/5 = 0V

Palmtop Computer and LCD Power-Supply Regulators

Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	Shutdown Input disables both SMPSs when low, but the reference remains alive. If the linear regulator is powered up, SHDN is overridden.
2	NEGON	Negative SMPS On/Off Control Input that enables the auxiliary negative SMPS when high.
3	3/$\overline{5}$	Selects the main output voltage setting – 5V when low.
4	$\overline{PFO}$	Power-Fail Output - an open-drain output that goes low to indicate that the main output is out of regulation by 6% or more.
5	VREF	1.250V Reference Voltage Output. Bypass with 0.22µF capacitor to AGND (0.1µF if there is no external reference load). Maximum load capability is 250µA source, 20µA sink.
6	AGND	Quiet Analog Ground
7	FB3	Feedback Input for the main SMPS
8	FBN	Feedback Input for the auxiliary negative SMPS
9	CS+	Positive Current-Sense Input for the auxiliary SMPS controller. 200mV corresponds with the maximum current limit threshold.
10	CS-	Negative Current-Sense Input
11	DHI	Driver for the auxiliary SMPS PNP. Open-drain P-channel output.
12	DLOW	Driver for the auxiliary SMPS PNP. Open-drain N-channel output. This output provides a controlled current sink to drive the PNP (set by an external limiting resistor).
13	LIN	Linear-Regulator Controller Output drives the external PNP pass transistor. Open-drain N-channel output. The main SMPS automatically shuts off when the voltage at LIN reaches 7.3V, and turns back on when LIN falls to 6.5V.
14	GND	Power Ground
15	LX3	1.2A, 0.4Ω N-channel power MOSFET drain for the main SMPS.

Detailed Description

Operating Principle

The MAX722/MAX723 combine two switch-mode power-supply (SMPS) regulators, a linear regulator, a precision voltage reference, and a power-fail detector (Figure 2). For maximum integration, the MAX722/MAX723 ICs contain internal N-channel power MOSFETs for the main low-voltage boost converter. This MOSFET is a "sense-FET" type for best efficiency, and has a very low gate-threshold voltage to guarantee start-up under low battery-voltage conditions (1.2V typ with 100mA load). The negative auxiliary controller exploits an external PNP transistor for the higher voltage requirement.

Pulse-Frequency Modulation

A unique minimum-off-time, current-limited, pulse-frequency modulation (PFM) control scheme is a key feature of both the main and auxiliary regulators (Figure 3). This PFM scheme combines the advantages of a pulse-width modulation scheme (PWM) (high output power and efficiency) with those of a traditional PFM pulse-skipper (ultra-low quiescent currents). There is no oscillator; switching is accomplished through a constant peak-current limit in the switch, which allows the inductor current to self-oscillate between this peak limit and some lesser value. Switching frequency is governed by a pair of one-shots that set a minimum off-time (1µs) and a maximum on-time (4µs). Under light loads, the inductor current rises to about one-half the current limit (for best light-load efficiency). Under heavy loads, the peak inductor current rises until it hits the current limit, whereupon the MOSFET switch turns off for the minumum off-time set by a one-shot. A switch to continuous-conduction mode results, which minimizes peak currents and component stresses for a given load. The only disadvantage of this architecture compared to full PWM operation is the variable-frequency switching noise. However, the noise does not exceed the current-limit times the filter capacitor equivalent series resistance (ESR), unlike conventional pulse-skippers.

Main 3V/5V Switch-Mode Regulator

The main output voltage can be selected to 3.3V or 5V with logic control, or it can be left in one mode or the other by tying 3/5 to ground or FB3. Efficiency varies depending on the battery and load, and is typically better than 80% over a 1mA to 200mA load range. The device is internally bootstrapped; power is derived from the output voltage (via FB3) or the battery (CS+ input), whichever is higher. When the output is set at 5V instead of 3.3V, the higher internal supply voltage results in lower switch transistor on-resistance and slightly greater output power. Bootstrapping allows the battery voltage to sag

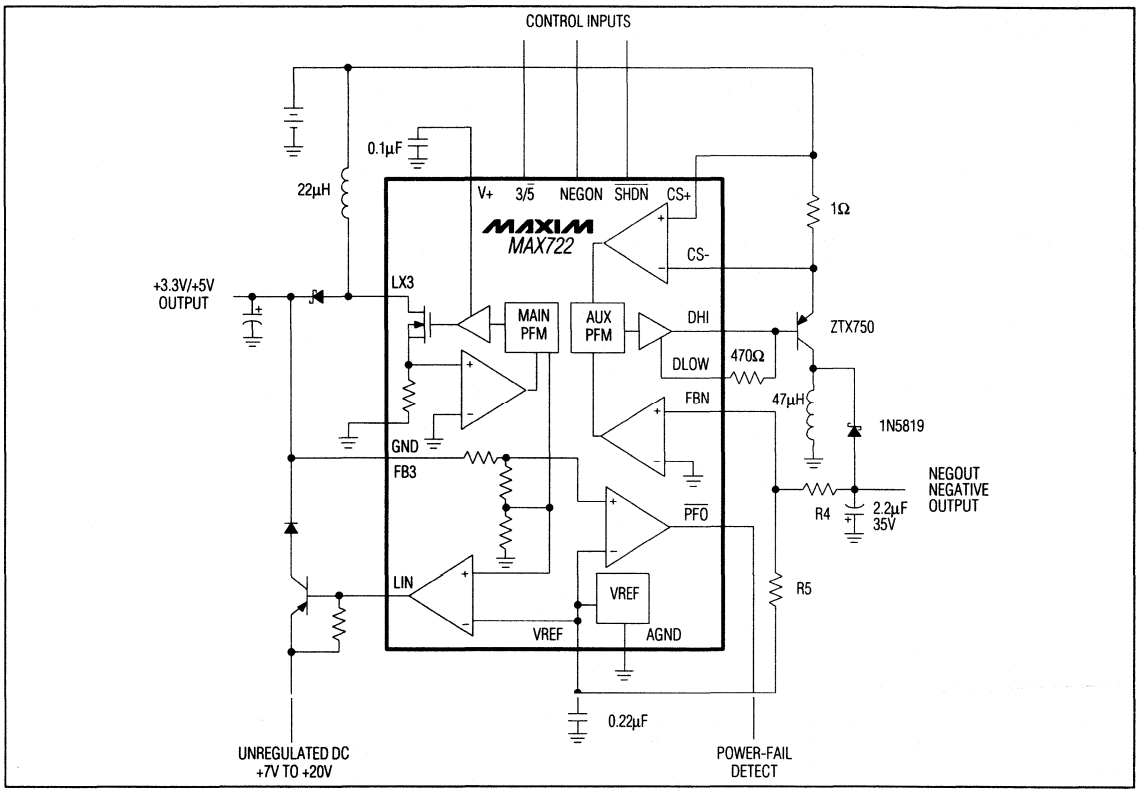


Figure 2. MAX722 Block Diagram

to less than 1V once the system is started. Therefore, the battery-voltage range is from V_{OUT} + V_{diode} to less than 1V (where V_{diode} is the forward drop of the Schottky rectifier). If the battery voltage exceeds the programmed output voltage, the output will follow the battery voltage. In many systems this is acceptable; however, the output voltage must not be forced above 7V.

The main regulator's peak current limit is internally fixed at 1A ±0.2A. The switching frequency depends on load and input voltage, and can range as high as 500kHz for the main SMPS.

Auxiliary Negative Switch-Mode Controller

The auxiliary controller operates similarly to the main regulator, except that the power transistor and sense resistor are external, and the maximum on-time is set at 8µs. Maximum possible output power is limited by the choice of external power transistor and sense resistor. A common 2N2907 works well as the switch transistor, but a high-gain fast PNP, such as the Zetex ZTX749 (preferred, but 25V BVCEO) or ZTX750 (40V BVCEO), provides typically 5% better efficiency.

The DHI and DLOW outputs provide a voltage source pull-up (DHI) and a current-sink pull-down (DLOW, set by the 470Ω resistor). This drive method is optimal for PNP transistors, so no external base speed-up capacitors are needed.

If the auxiliary regulator is always powered from a +5V source (such as the main output) or other relatively high-voltage input, a logic-level P-channel MOSFET in place of the PNP can provide typically > 80% efficiency (Figure 4).

The output voltage is set by R4 and R5 of Figure 1:

NEGOUT = -VREF(R4/R5)

NEGOUT can be made adjustable by making R4 a potentiometer, or by disconnecting VREF and driving R5 with a digital-to-analog converter or PWM signal.

Palmtop Computer and LCD Power-Supply Regulators

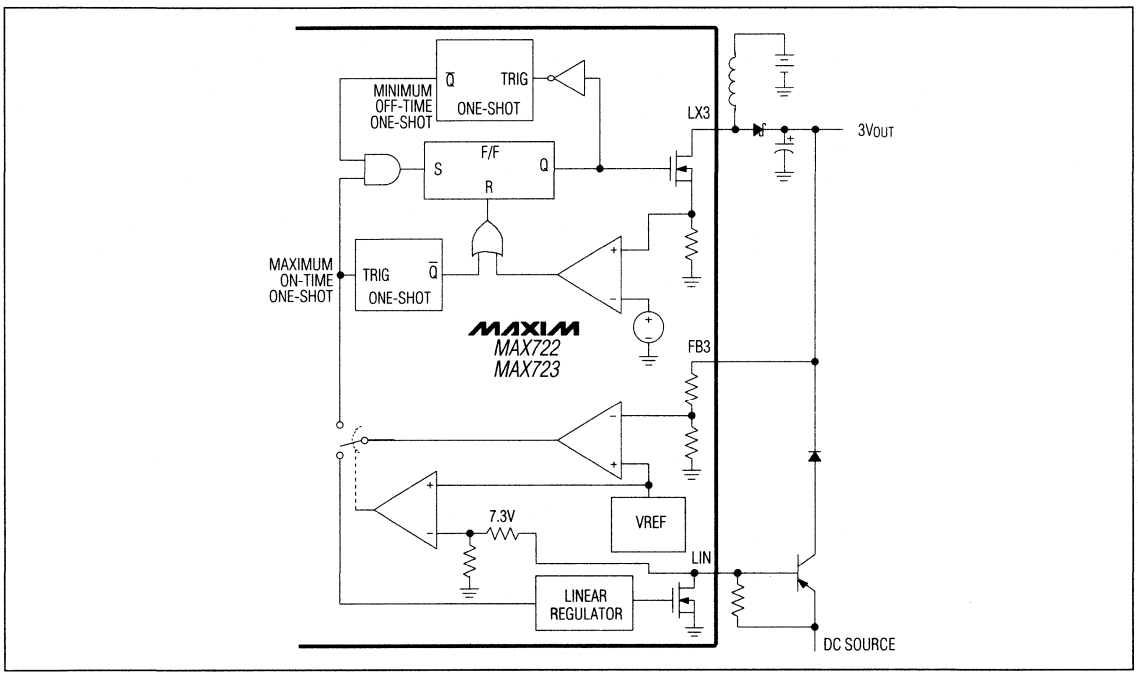


Figure 3. Main SMPS Block Diagram

The auxiliary SMPS peak current limit is set at 200mV/R1 (170mV worst-case low). The equations below calculate R1 based on design parameters. If the peak current limit is less than (NEGOUT) (1µsec/L), the circuit will operate in discontinuous-conduction mode. This is usually the case when low-voltage batteries and high LCD contrast voltages are employed. At low-output voltage settings, the circuit may enter continuous-conduction mode.

Discontinuous-conduction case:

$$I_{PEAK} = (2)\,(I_{LOAD})\left(1 + \frac{NEGOUT + VD}{VBATT - VSW}\right)$$

$$R1 = 200mV/I_{PEAK}$$

where VD is the forward voltage of the rectifier D2 and VSW is the average saturation voltage of the switch transistor Q1, including the drop across R1.

Discontinuous-mode example, -17V at 9mA from 2 AA batteries:

$$I_{PEAK} = (2)\,(9mA)\left(1 + \frac{17V + 0.5V}{2V - 0.3V}\right) = 203mA$$

$$R1 = 170mV/203mA = 0.83\Omega \text{ or less.}$$

Continuous-conduction case:

$$I_{PEAK} = (I_{LOAD})\left(\frac{NEGOUT + VD}{VBATT - VSW} + 1\right) + \left(\frac{NEGOUT + VD}{(2)\,(L)}\right)(1\mu s)$$

Continuous-mode example, -5V at 50mA from 3 AA batteries:

$$I_{PEAK} = 50mA\left(\frac{5V + 0.5V}{2.7V - 0.3V} + 1\right) + \left(\frac{5V + 0.5V}{(2)\,(47\mu H)}\right)(1\mu s) = 223mA$$

Powering the Auxiliary LCD Supply

The auxiliary output is not automatically powered from the linear regulator like the main output. The main battery will continue to drain if the auxiliary supply is not turned off when an external DC source is applied. There are several alternative solutions:

1. Power the LCD supply from the main output all the time. This leads to compounded efficiency losses, but is simple. These compounded losses are actually not crippling in many cases, especially if the main output is set

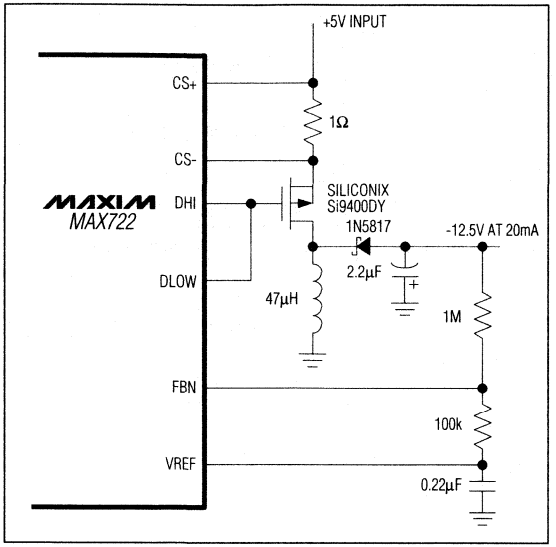


Figure 4. +5V-Powered LCD Supply with P-Channel MOSFET

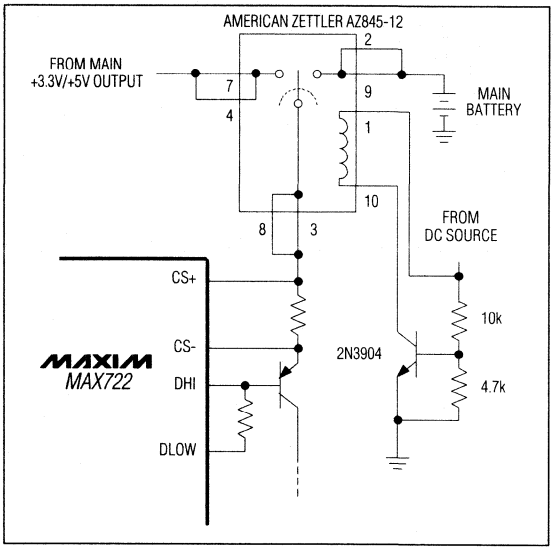


Figure 5. SMT Relay Powers Auxiliary LCD Supply

at 5V and the P-channel solution (Figure 4) is employed. For example, the overall efficiency for 2.5V to 5V at 50mA plus -17V at 5mA, when compounded by the P-channel circuit, is 81% vs. 84% for the non-compounded case (with PNP transistor).

2. Power the LCD supply from the main output in linear regulator mode, but power it from the battery when the DC source is absent. This provides the best overall efficiency, but requires a relay or MOSFET switch to make the switchover (Figure 5). In most applications, the battery voltage is too low to use P-channel devices for the switchover, but a high-side supply, such as the MAX623 charge-pump regulator (Figure 6) or the system +12V supply, works well with N-channel switches. Switchover can also be accomplished using special AC/DC adapter plugs and jacks with built-in mechanical switches.

3. Use a battery charger that can supply a load while it charges the battery, such as the MAX713. This approach also eliminates the PNP pass transistor for the linear regulator.

Linear Regulator

The linear regulator output drives the base of an external PNP pass transistor through an open-drain output. This design relies on a relatively slow PNP transistor for AC stability, so use a transistor with less than 10MHz f_t, or add a 1µF base-emitter capacitor. The base-emitter resistor should not be higher than 1kΩ unless a low-leakage PNP is used for the pass transistor.

When constructed with a 2N2955 PNP transistor, the typical output current capability is greater than 1A.

When the linear regulator operates, the main SMPS is disabled so as not to drain the battery. This mode cannot be programmed, but occurs automatically when LIN is pulled high by the external DC source.

Voltage Reference

The precision voltage reference is suitable for driving external loads such as a low-battery detection comparator or an analog-to-digital converter. It has guaranteed 250µA source- and 20µA sink-current capability. The reference is kept alive even in shutdown mode. If the reference drives an external load, bypass it with 0.22µF to ground. If the reference is unloaded, bypass it with a 0.1µF capacitor, minimum.

Power-Fail Status Output

The power-fail detector output ($\overline{PFO}$) is an active-low, open-drain type. Although a true open-drain type, which can be wire-OR'ed with external logic, $\overline{PFO}$ is protected against ESD damage by reverse-biased clamp diodes connecting to V+. If $\overline{PFO}$ is pulled up to external supply voltages above the main output voltage level, the pull-up resistor must limit the current through the ESD protection diode to 25µA or less to maintain regulation of the outputs.

The $\overline{PFO}$ comparator senses when the main output is more than 6% out of regulation, and has 2% hysteresis

Palmtop Computer and LCD Power-Supply Regulators

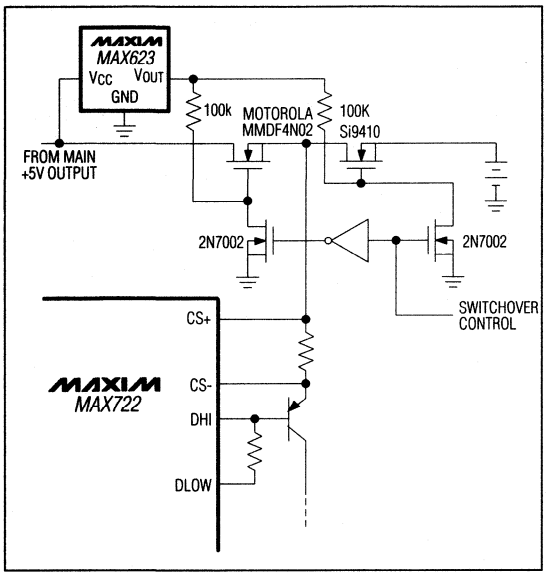


Figure 6. High-Side MOSFET Switch Powers Auxiliary LCD Supply

built in to prevent chatter. The $\overline{PFO}$ comparator is active in all modes except shutdown.

Control-Logic Inputs

The control inputs (3/$\overline{5}$, NEGON, and $\overline{SHDN}$) are high-impedance MOS gates protected against ESD damage by normally reverse-biased clamp diodes. If these inputs are driven from signal sources that exceed the main supply (FB3) voltage, the diode current should be limited to 25µA or less by a series resistor (1MΩ suggested). The logic input thresholds are the same (approximately 1V) in both 3V and 5V modes. Do not leave the control inputs floating.

Substrate Switchover Circuit

The substrate (V+, pin 16) is powered from either the battery (CS+ input) or from the main +3V output, whichever is higher. The substrate serves as the positive supply rail for most internal circuitry, including the reference and the PNP driver (DHI). Do not load V+. V+ must be bypassed to ground with at least 0.1µF.

Inductor Selection

The inductors must have a saturation (incremental) current rating equal to the peak switch current limit, which is 1.2A (worst-case) for the main output and user-adjustable for the auxiliary output. However, it's generally acceptable to bias the inductor deep into saturation by 20% or more.

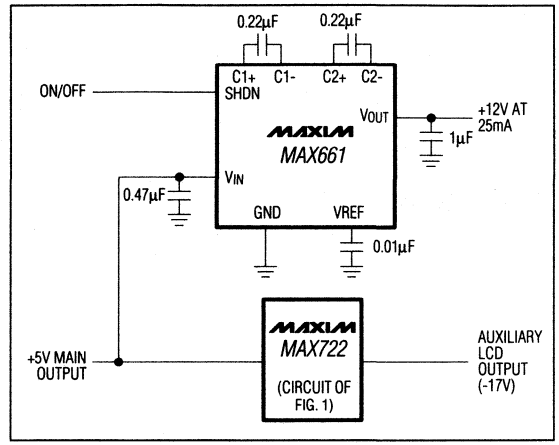


Figure 7. MAX722/MAX661 Triple-Output Supply with +12V for Flash Memory

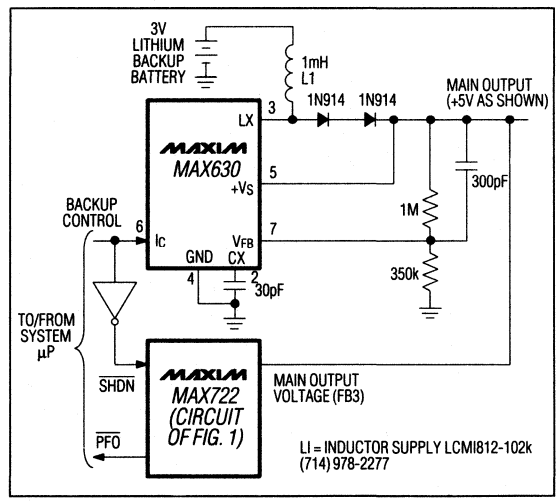


Figure 8. Lithium Backup-Battery Circuit

The inductor's DC resistance significantly affects efficiency. For highest efficiency, limit L1's DCR to 0.03Ω or less.

Capacitor Selection

A 100µF, 10V SMT tantalum capacitor typically maintains 50mV$_{p-p}$ output ripple when stepping up 2V to 5V at 200mA. Smaller capacitors, down to 10µF, are acceptable for light loads or in applications that tolerate higher output ripple.

For the auxiliary output, a 2.2µF, 25V SMT tantalum capacitor typically provides $100mV_{p-p}$ output ripple when inverting 3V to -17V at 5mA. Smaller capacitors down to 1µF are acceptable.

The ESR of both bypass and filter capacitors affects efficiency. Best performance is obtained by doubling up on the filter capacitors or using specialized low-ESR capacitors.

The smallest low-ESR SMT tantalum capacitors currently available are Sprague 595D series, which are about half the size of competing products. Sanyo OS-CON organic semiconductor through-hole capacitors also exhibit very low ESR.

Sprague: (603) 224-1961 or (207) 324-4140
Sanyo: (619) 661-6322

Applications Information

Lithium Backup-Battery Circuit

The MAX630 backup battery circuit of Figure 8 provides a low-current supply voltage of 3.3V or 5V to keep the system memory alive when the main battery pack is removed. When $\overline{PFO}$ goes low, the system must latch off the MAX722 and latch on the MAX630, periodically testing for the presence main battery's by going back to the original state after some interval. This method also extends the life of the expensive lithium battery by allowing a discharged main battery to "rest," allowing all of its energy to be used. The second rectifier diode allows this circuit to meet Underwriters Laboratories' requirements for preventing accidental charging of lithium batteries.

$\overline{PFO}$ remains active in shutdown mode.

PC Layout and Grounding

The MAX722's high peak currents and high-frequency operation make PC layout important for minimizing ground bounce and noise. Use the PC layout of Figures 9 and 10 as a rough guide for component placement and ground connections. The distance between the MAX722's GND and the ground leads of C1 and C5 must be kept to less than 0.2 inches (5mm). If possible, use a ground plane.

3-Cell Applications

Higher input voltages increase the energy transferred with each cycle, due to the reduced input/output differential. Excess ripple due to increased energy transfer is best minimized by reducing the inductor value (10µH suggested). Add extra filtering and recalculate the auxiliary regulator's current limit resistor value according to the equations under the *Auxiliary Negative Switch-Mode Controller* section.

Palmtop Computer and LCD Power-Supply Regulators

EV Kit General Description

The MAX722 evaluation kit (EV kit) is an assembled surface-mount demonstration board. The kit embodies the standard 2-cell application circuit of Figure 1, and adds a DIP switch and 3MΩ pull-up resistors for each control input. A MAX722 comes installed on the board, and it also accomodates a MAX723 footprint. To replace the MAX722 IC, first cut the leads free of the package, then carefully desolder the leads individually.

Operating Instructions

For best efficiency, connect heavy-gauge (18AWG) stranded wire from the battery terminals to a 2A adjustable supply or 2-cell battery pack.

Important: Connect BATT1 and BATT2 together with heavy wire to ensure both SMPS regulators work. If BATT1 is powered separately from BATT2, connect a new input bypass capacitor across BATT1 (not included). Otherwise, there is no filtering at BATT1 and efficiency will be poor.

Adjust the supply up to two or three volts. Load the outputs and observe the switching waveforms at LX3 and DHI.

EV Kit Component List

DESIGNATION	DESCRIPTION	SOURCE
C1	100µF, 10V E-size SMT tantalum capacitor	Matsuo 267M1002-107
C2	2.2µF, 35V C3-size SMT tantalum capacitor	Matsuo 267M2502-335
C3	0.22µF 1206-size ceramic capacitor	Murata-Erie GRM42-6X7R224K025V
C4	0.1µF 1206-size ceramic capacitor	Murata-Erie GRM42-6X7R104K025V
C5	150µF, 6.3V E-size SMT tantalum capacitor	Matsuo 267M6301-157
C6	Not used	
L1	22µH, 1A SMT inductor	Sumida CD54-220 or two CD43-220 in parallel
L2	47µH, 0.25A SMT inductor	Sumida CD54-470
R1	1Ω ±10% 1206-size chip resistor	Ohmtek L1206MR1R00LB
R2	330Ω ±5% 1206-size chip resistor	
R3	470Ω ±5% 1206-size chip resistor	
R4	1.5MΩ ±1% 1206-size chip resistor	
R5	110kΩ ±1% 1206-size chip resistor	
D1	1A SMT Schottky rectifier, 1N5817 equivalent	NIEC EC15QS02L
D2	1A SMT Schottky rectifier, 1N5818 equivalent	NIEC EC10QS03
D3	1A SMT silicon rectifiers, 1N4001 equivalent	NIEC EC10DS1
Q1	Fast, high-gain, low sat 30V PNP transistor	Zetex ZTX750SM
Q2	Power PNP transistor, D-PAK	Motorola MJD2955

Matsuo USA (714) 969-2491 FAX (714) 960-6492
Matsuo Japan (06) 332-0871
Motorola (602) 244-6900
Murata-Erie (404) 436-1300
NIEC (805) 867-2555
NIEC Japan (81) 3-3494-7411

Ohmtek (716) 283-4025
Siliconix 408) 988-8000
Sumida USA (708) 956-0666
Sumida Japan (03) 3607-5111 FAX (03) 3607-5428
Zetex (516) 543-7100

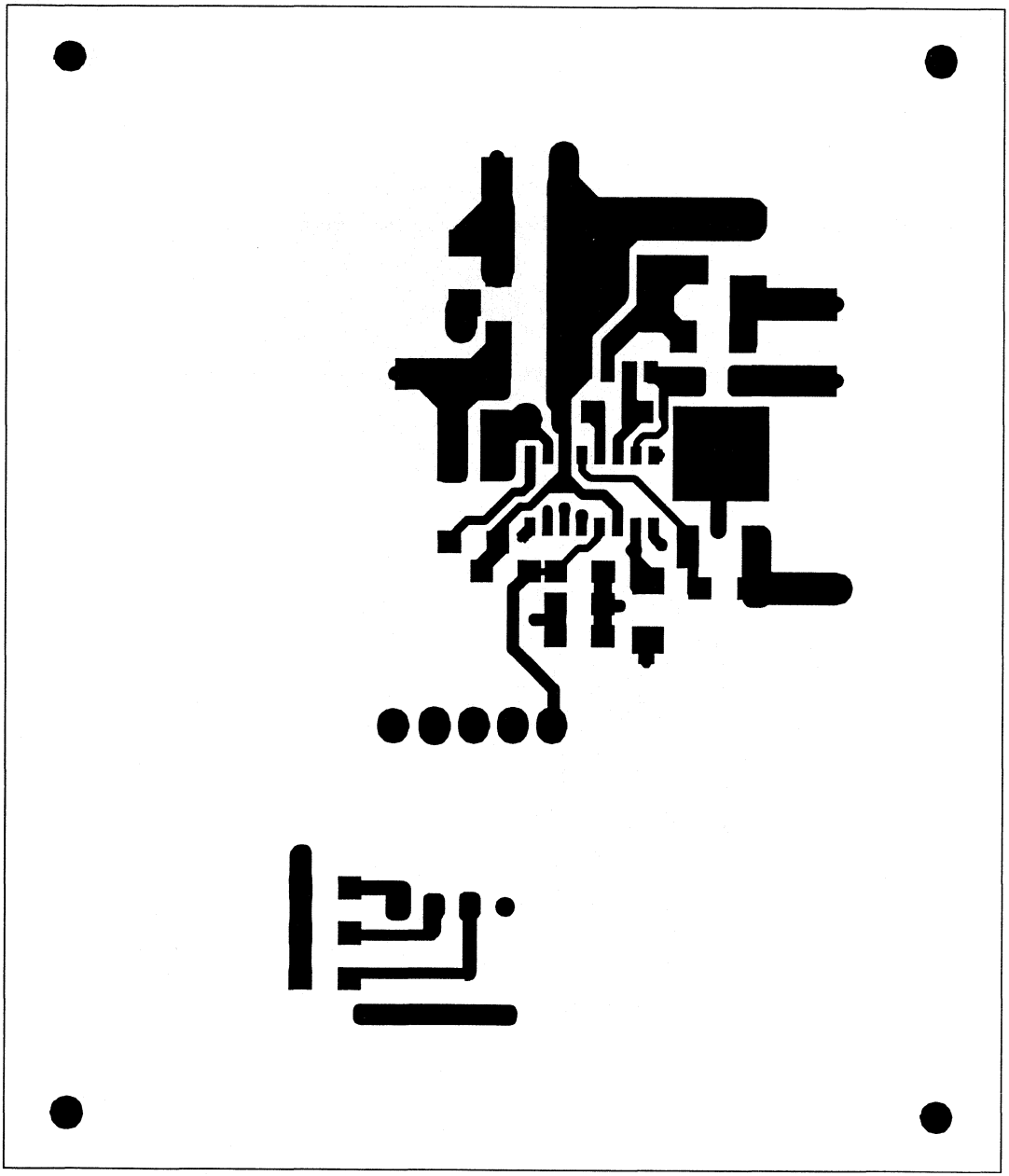


Figure 9. MAX722 EV Kit PC Layout (Component Layer, Component Side View, 2X Scale)

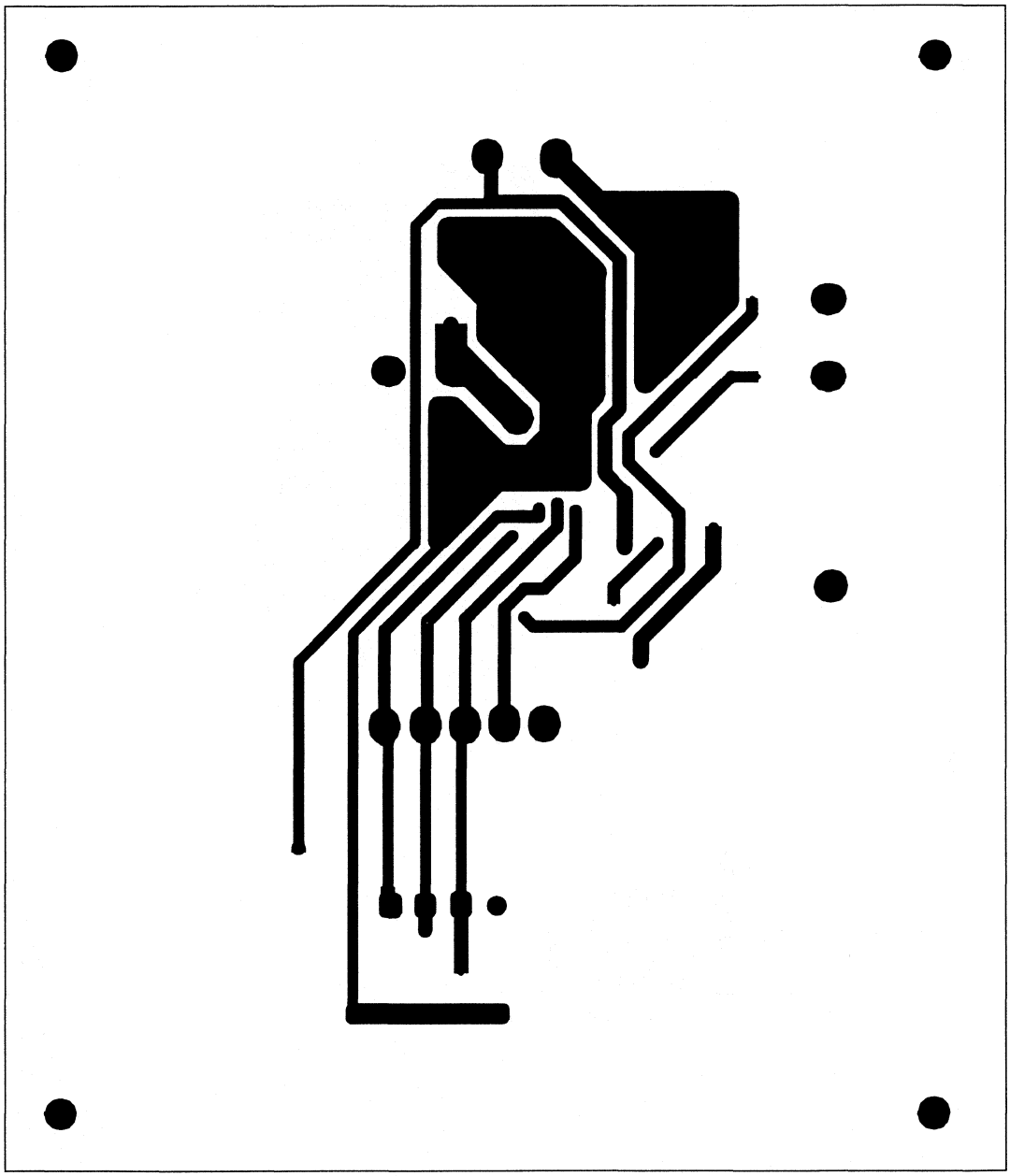


Figure 10. MAX722 EV Kit PC Layout (Bottom Layer, Component Side View, 2X Scale)

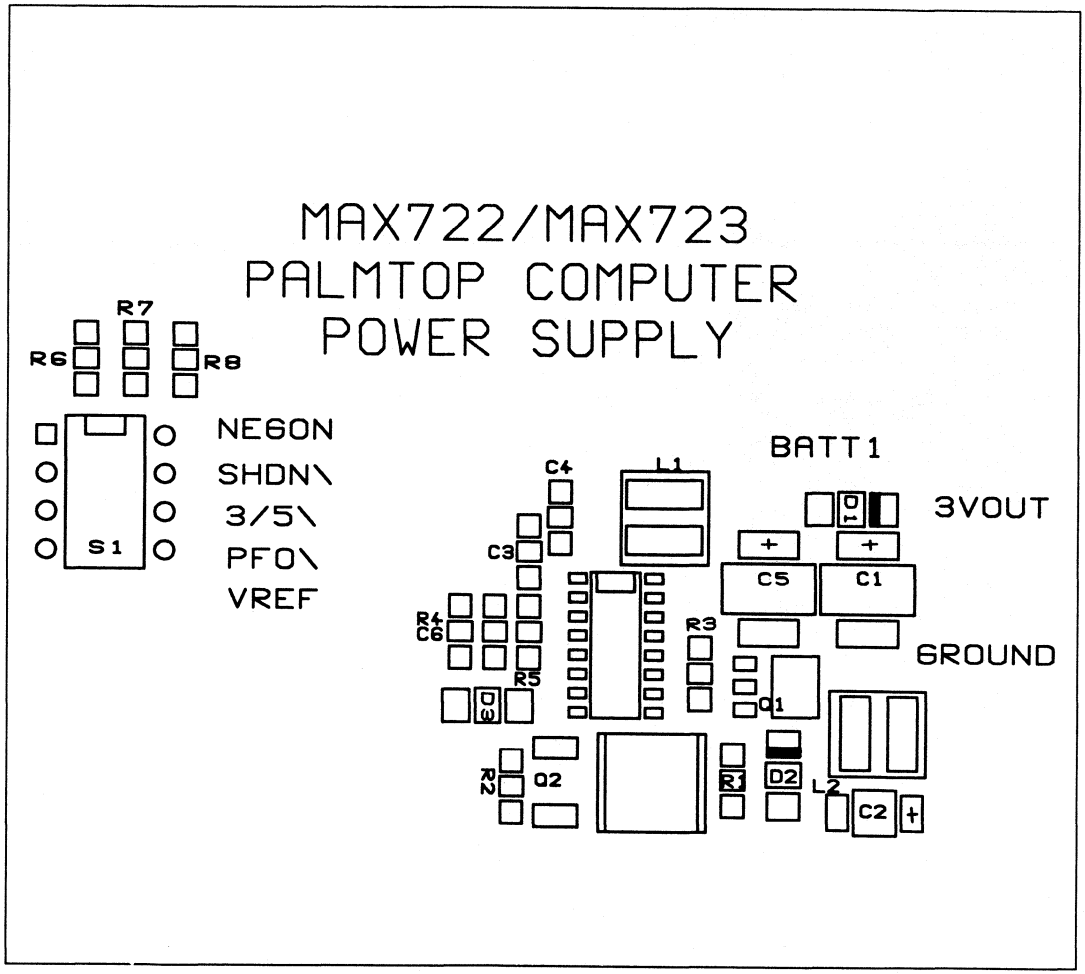
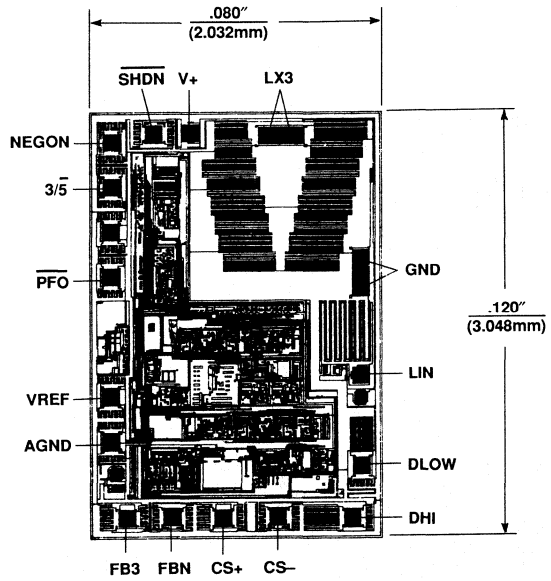


Figure 11. MAX722 EV Kit Component Placement Diagram

Palmtop Computer and LCD Power-Supply Regulators

Chip Topography



TRANSISTOR COUNT: 743.
SUBSTRATE IS CONNECTED TO V+.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

5A, Step-Down, PWM, Switch-Mode DC-DC Regulator

General Description

The MAX724 is a monolithic, bipolar, pulse-width modulation (PWM), switch-mode DC-DC regulator optimized for step-down applications. The MAX724 is rated at 5A. Few external components are needed for standard operation because the power switch, oscillator, and control circuitry are all on-chip. Employing a classic buck topology, this regulator performs high-current step-down functions, and can also be configured as an inverter, a negative boost converter, or a flyback converter.

This regulator has excellent dynamic and transient-response characteristics, while featuring cycle-by-cycle current limiting to protect against overcurrent faults and short-circuit output faults. The MAX724 also has a wide 8V to 40V input range (up to 60V for the high-voltage MAX724H version) in the 5V output step-down configuration. In inverting and boost configurations, the input can be as low as 5V.

Available in 5-pin TO-220, 4-pin TO-3, and 11-pin SIP packages, these devices have a preset 100kHz oscillator frequency and a preset 6.5A current limit. The 11-pin package allows for such options as an external oscillator drive input (to raise the frequency to 200kHz), adjustable current limit, micropower shutdown, soft-start, and microprocessor reset.

Applications

Distributed Power from High-Voltage Buses

High-Current, High-Voltage Step-Down Applications

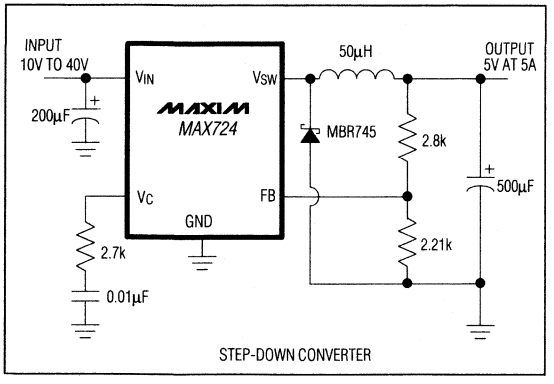
High-Current Inverter

Negative Boost Converter

Multiple-Output Buck Converter

Isolated DC-DC Conversion

Typical Operating Circuit



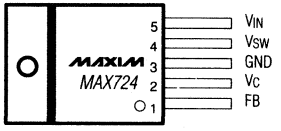
STEP-DOWN CONVERTER

Features

- ♦ 40V Input Range (60V for MAX724H)
- ♦ 5A On-Chip Power Switch
- ♦ 2.5V to 40V Adjustable Output (50V for MAX 724H)
- ♦ 100kHz Switching Frequency (Adjustable to 200kHz)
- ♦ Excellent Dynamic Characteristics
- ♦ Few External Components
- ♦ 8.5mA Quiescent Current
- ♦ TO-220, TO-3, SIP Packages

Pin Configurations

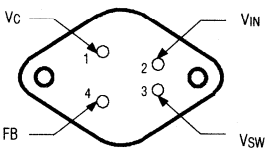
FRONT VIEW



TO-220

CONTACT FACTORY FOR STRAIGHT PINS.

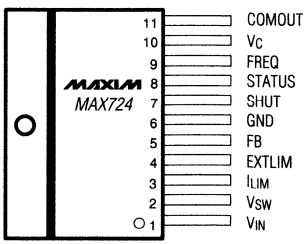
BOTTOM VIEW



TO-3

CASE IS GND.

FRONT VIEW



SIP

CASE IS CONNECTED TO GROUND. PINS ARE FORMED.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

2A, Step-Down, PWM, Switch-Mode DC-DC Regulators

General Description

The MAX726 - MAX729 are monolithic, bipolar pulse-width modulation (PWM), switch-mode DC-DC regulators optimized for step-down applications. Their internal switches are rated at 2A. Few external components are needed for standard operation because the power switch, oscillator, and control circuitry are all on-chip. Employing a classic buck topology, these regulators perform high-current step-down functions, and can also be configured as inverters, negative boost converters, or flyback converters.

The MAX726 has a 2.5V to 40V adjustable output, while the MAX727, MAX728, and MAX729 have preset outputs of +5V, +3.3V, and +3V, respectively. These regulators have excellent dynamic and transient-response characteristics, and feature cycle-by-cycle current limiting to protect against overcurrent faults and short-circuit output faults. They also have a wide 8V to 40V input range (up to 60V for the high-voltage "H" version) in the 5V-output buck configuration. In inverting and boost configurations, the input can be as low as 5V.

Available in 5-pin TO-220 and 11-pin SIP packages, these devices have a preset 100kHz oscillator frequency and a preset 2.6A current limit. The 11-pin packages allow for options such as an external oscillator drive input (to raise the frequency to 200kHz), adjustable current limit, micropower shutdown, soft-start, and micropower reset.

Features

- ♦ **40V Input Range (60V for "H" Versions)**
- ♦ **2A On-Chip Power Switch**
- ♦ **Adjustable Output (2.5V to 40V) – MAX726**
- ♦ **Preset Outputs: +5V for MAX727**
  +3.3V for MAX728
  +3V for MAX729
- ♦ **100kHz Switching Frequency (Adjustable to 200kHz)**
- ♦ **Excellent Dynamic Characteristics**
- ♦ **Few External Components**
- ♦ **8.5mA Quiescent Current**
- ♦ **5-Pin TO-220 and 11-Pin SIP Packages**

Applications

Distributed Power from High-Voltage Buses

High-Current, High-Voltage Step-Down Applications

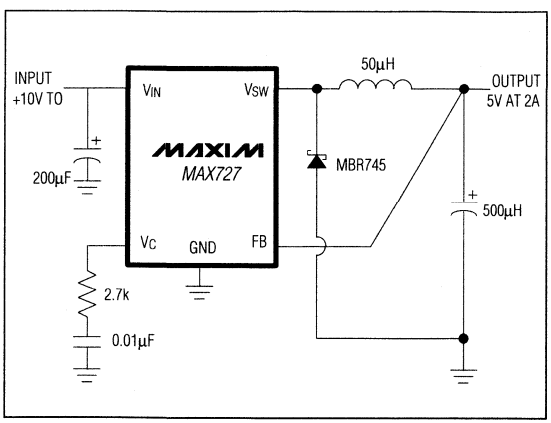
High-Current Inverter

Negative Boost Converter

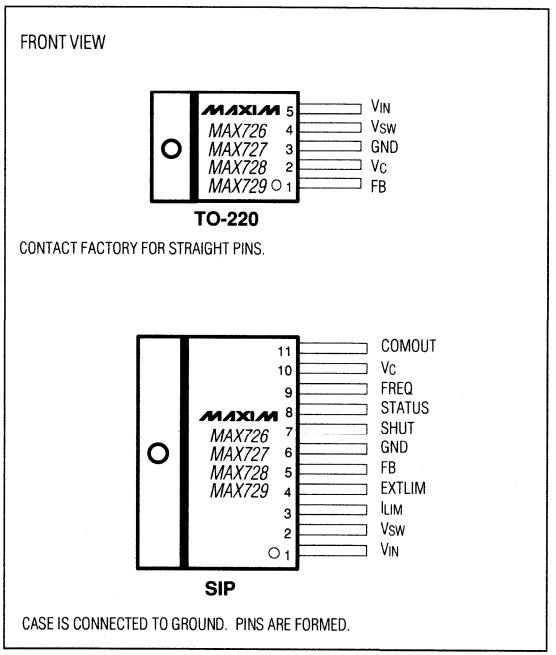
Multiple-Output Buck Converter

Isolated DC-DC Conversion

Typical Operating Circuit



Pin Configurations



19-4143; Rev. 0; 2/92

EVALUATION KIT AVAILABLE

+5V and Adjustable Step-Down Current-Mode PWM Regulators

General Description

The MAX730/MAX738 are +5V-output CMOS, step-down, switching DC-DC regulators. The MAX750/MAX758 are adjustable output versions of the MAX730/MAX738. The MAX738 accepts inputs from 6.0V to 16.0V and delivers up to 750mA at 5V. The MAX730 accepts inputs from 5.2V to 11.0V and delivers up to 300mA at 5V. The MAX758 delivers up to 3.75W from inputs of 4.0V to 16.0V. The MAX750 delivers up to 1.5W from 4.0V to 11.0V inputs. Typical efficiencies exceed 90%, and accuracy is guaranteed over temperature, line, and load variations. Pulse-width modulation (PWM) current-mode control provides precise output regulation and low subharmonic noise. Typical quiescent current is 1.7mA. 165kHz switching frequency allows easy ripple and noise filtering and use of small external components. These regulators require only a single inductor value to function over their entire input range, so no inductor design is necessary.

The MAX730/738/750/758 also feature cycle-by-cycle current limiting, overcurrent limiting, undervoltage lockout, and programmable soft-start protection.

For lower-power step-down applications, refer to the MAX639 data sheet.

Applications

Portable Instruments

Distributed Power Systems

Computer Peripherals

DC-DC Converter Module Replacements

Features

- **Up to 750mA Load Currents with No External MOSFETs (MAX738/MAX758)**
- **165kHz High Frequency Current-Mode PWM**
- **Greater than 90% Typ Efficiencies**
- **Single Pre-Selected Inductor Value, No Component Design Required**
- **1.7mA Typ Quiescent Current**
- **Overcurrent, Soft-Start, and Shutdown Protection**
- **Adjustable Output (MAX750/MAX758)**
- **8-Pin DIP/SO and 16-Pin Wide SO Packages**

Ordering Information

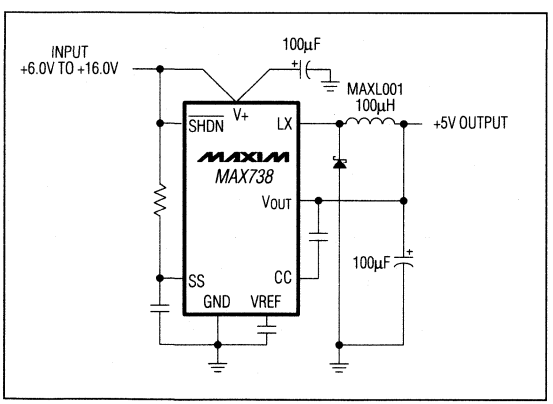
PART	TEMP. RANGE	PIN-PACKAGE
MAX730CPA	0°C to +70°C	8 Plastic DIP
MAX730CSA	0°C to +70°C	8 SO
MAX730C/D	0°C to +70°C	Dice*
MAX730EPA	-40°C to +85°C	8 Plastic DIP
MAX730ESA	-40°C to +85°C	8 SO
MAX730MJA	-55°C to +125°C	8 CERDIP**
MAX738CPA	0°C to +70°C	8 Plastic DIP
MAX738CWE	0°C to +70°C	16 Wide SO
MAX738C/D	0°C to +70°C	Dice*
MAX738EPA	-40°C to +85°C	8 Plastic DIP
MAX738EWE	-40°C to +85°C	16 Wide SO
MAX738MJA	-55°C to +125°C	8 CERDIP**

Ordering Information continued on last page.

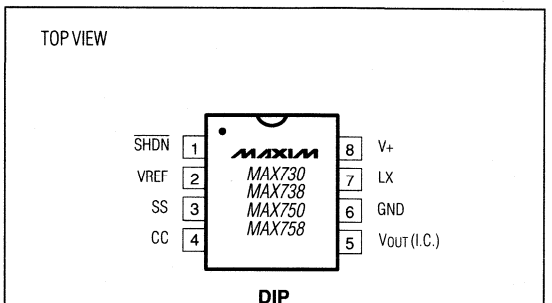
* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configurations



DIP

NOTE: ( ) ARE FOR MAX750/MAX758 ONLY.

Pin Configurations continued on last page.

+5V and Adjustable Step-Down Current-Mode PWM Regulators

ABSOLUTE MAXIMUM RATINGS

Pin Voltages:
- V+ (MAX730/750) ..... +12V, -0.3V
- V+ (MAX738/758) ..... +18V, -0.3V
- LX (MAX730/750) ..... (V+ -12V) to (V+ +0.3V)
- LX (MAX738/758) ..... (V+ -21V) to (V+ +0.3V)
- V_{OUT} ..... ±25V
- SS, CC, $\overline{SHDN}$ ..... -0.3V to (V+ +0.3V)

Peak Switch Current (I_{LX}) 2.0A
Reference Current (I_{VREF}) 2.5mA
Power Dissipation (T_A = +70°C)
- 8-Pin Plastic DIP (derate 6.90mW/°C above +70°C) . 552mW
- 8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
- 16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
- 8-Pin CERDIP (derate 8.00mW/°C above +70°C) ... 640mW

Operating Temperature Ranges:
- MAX7_ _C_ _ ..... 0°C to +70°C
- MAX7_ _E_ _ ..... -40°C to +85°C
- MAX7_ _MJA ..... -55°C to +125°C

Junction Temperatures:
- MAX7_ _C/E ..... +150°C
- MAX7_ _M ..... +175°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 3; V+ = 9V for the MAX730/750; V+ = 12V for the MAX738/758; V_{OUT} = 5V, R2 = 40.20kΩ, R3 = 13.0kΩ for the MAX750/758; I_{LOAD} = 0mA; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MAX730/MAX750			MAX738/MAX758			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage (Note 1)	V+ = 6.0V to 11.0V, 0 < I_{LOAD} < 300mA	4.75	5.00	5.25				V
	V+ = 6.6V to 16.0V, 0 < I_{LOAD} < 300mA				4.75	5.00	5.25	
	V+ = 10.2V to 16.0V, 0 < I_{LOAD} < 750mA				4.75	5.00	5.25	
Input Voltage Range	MAX730 only	5.2		11.0				V
	MAX738 only				6.0		16.0	
	MAX750 only	4.0		11.0				
	MAX758 only				4.0		16.0	
Line Regulation	V+ = 5.2V to 11.0V		0.15					%/V
	V+ = 6.0V to 16.0V					0.15		
Load Regulation	I_{LOAD} = 0mA to 300mA		0.0005					%/mA
	I_{LOAD} = 0mA to 750mA					0.0005		
Efficiency	V+ = 9.0V, I_{LOAD} = 300mA		92			90		%
	V+ = 12V, I_{LOAD} = 750mA					87		
Supply Current	Includes switch current		1.7	3.0		1.7	3.0	mA
Standby Current	$\overline{SHDN}$ = 0 (Note 2)		6.0	100.0		6.0	100.0	µA
Shutdown Input Threshold	V_{IH} (Note 3)	V+ - 0.5V			V+ - 0.5V			V
	V_{IL} (Note 3)			0.25			0.25	
Shutdown Input Leakage Current				1.0			1.0	µA
Short-Circuit Current			1.5			1.5		A
Undervoltage Lockout	MAX730 only		4.7	5.2				V
	MAX738 only					5.7	6.0	
	MAX750 only		3.75	4.00				
	MAX758 only					3.75	4.00	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 3; V+ = 9V for the MAX730/750; V+ = 12V for the MAX738/758; V_{OUT} = 5V, R2 = 40.20kΩ, R3 = 13.0kΩ for the MAX750/758; I_{LOAD} = 0mA; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MAX730/750			MAX738/758			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
LX On Resistance	I_{LX} = 500mA		0.5			0.5		Ω
LX Leakage Current	V+ = 12V, LX = 0		1.0			1.0		µA
Reference Voltage (Note 1)		1.15	1.23	1.30	1.15	1.23	1.30	V
Reference Drift	T_A = T_{MIN} to T_{MAX}		50			50		ppm/°C
Oscillator Frequency		130	170	210	130	160	190	kHz
Compensation Pin Impedance			7500			7500		Ω

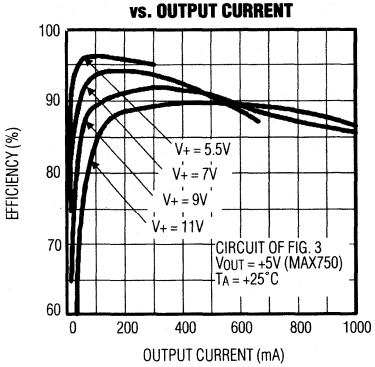
Note 1: Output voltage tolerance over temperature is ±4.5% plus external feedback resistor tolerances for adjustable devices (MAX750/MAX758).

Note 2: The standby current typically settles to 25µA (over temperature) within 2 seconds; however, to decrease test time, the part is guaranteed at a 100µA maximum value.

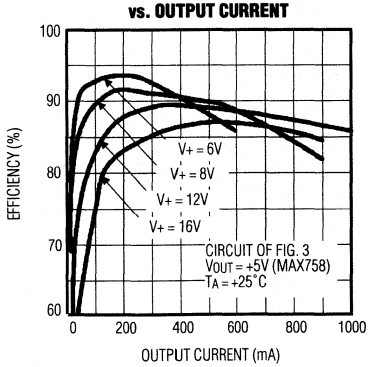
Note 3: Shutdown input thresholds not tested, but guaranteed by design.

Typical Operating Characteristics

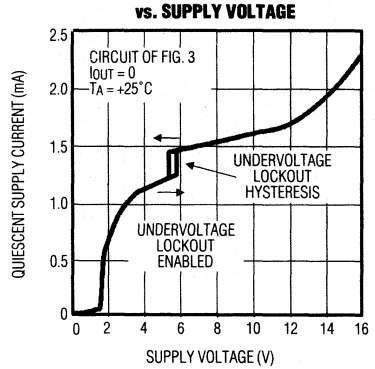
MAX730/MAX750 EFFICIENCY vs. OUTPUT CURRENT



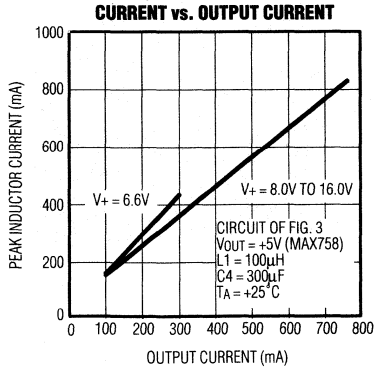
MAX738/MAX758 EFFICIENCY vs. OUTPUT CURRENT



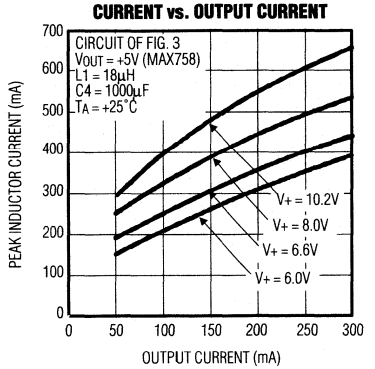
MAX738 QUIESCENT SUPPLY CURRENT vs. SUPPLY VOLTAGE



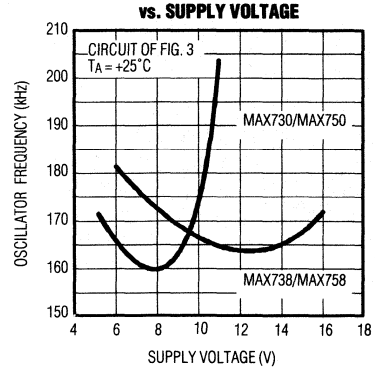
MAX738/MAX758 PEAK INDUCTOR CURRENT vs. OUTPUT CURRENT



MAX738/MAX758 PEAK INDUCTOR CURRENT vs. OUTPUT CURRENT



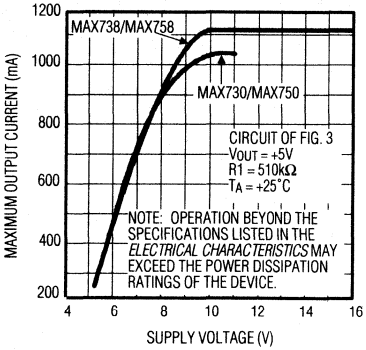
OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



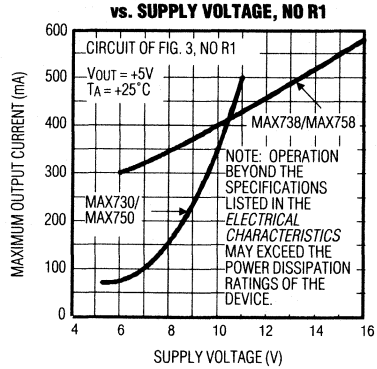
+5V and Adjustable Step-Down Current-Mode PWM Regulators

Typical Operating Characteristics (continued)

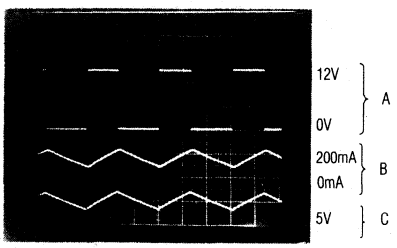
MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE, NO R1



SWITCHING WAVEFORMS CONTINUOUS CONDUCTION

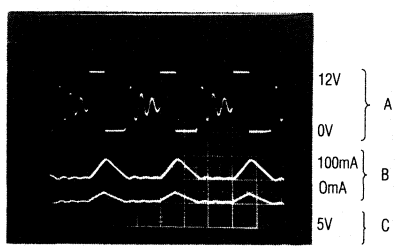


2µs/div

A: SWITCH VOLTAGE (LX PIN), 5V/DIV, 0V TO +12V
B: INDUCTOR CURRENT, 200mA/DIV
C: OUTPUT VOLTAGE RIPPLE, 50mV/DIV

MAX738/MAX758, CIRCUIT OF FIG. 3, C_{OUT} = 390µF, V+ = 12V, I_{OUT} =150µA, T_A = +25°C

SWITCHING WAVEFORMS DISCONTINUOUS CONDUCTION

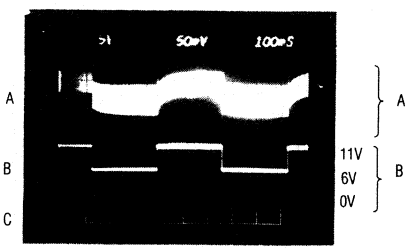


2µs/div

A: SWITCH VOLTAGE (LX PIN), 5V/DIV, 0V TO +12V
B: INDUCTOR CURRENT, 100mA/DIV
C: OUTPUT VOLTAGE RIPPLE, 50mV/DIV

MAX738/MAX758, CIRCUIT OF FIG. 3, C_{OUT} = 390µF, V+ = 12V, I_{OUT} = 150µA, T_A = +25°C

MAX730/MAX750 LINE-TRANSIENT RESPONSE

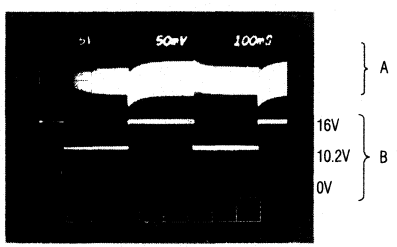


100ms/div

A: V_{OUT}, 50mV/DIV, DC-COUPLED
B: V+, 5V/DIV, 6.0V TO 11.0V

CIRCUIT OF FIG. 3, I_{OUT} = 300mA, T_A = +25°C

MAX738/MAX758 LINE-TRANSIENT RESPONSE

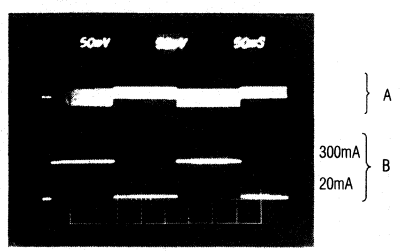


100ms/div

A: V_{OUT}, 50mV/DIV, DC-COUPLED
B: V+, 5V/DIV, 10.2V TO 16.0V

CIRCUIT OF FIG. 3, I_{OUT} = 750mA, T_A = +25°C

MAX730/MAX750 LOAD-TRANSIENT RESPONSE

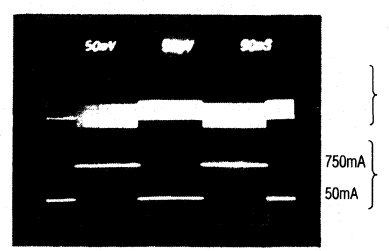


50ms/div

A: V_{OUT}, 50mV/DIV, DC-COUPLED
B: I_{OUT}, 200mA/DIV, 20mA TO 300mA

CIRCUIT OF FIG. 3, V+ = 9V, T_A = +25°C

MAX738/MAX758 LOAD-TRANSIENT RESPONSE



50ms/div

A: V_{OUT}, 50mV/DIV, DC-COUPLED
B: I_{OUT}, 500mA/DIV, 50mA TO 750mA

CIRCUIT OF FIG. 3, V+ = 12V, T_A = +25°C

+5V and Adjustable Step-Down Current-Mode PWM Regulators

Pin Description

PIN # 8-PIN DIP/SO	PIN # 16-PIN WIDE SO	NAME	FUNCTION
1	2	$\overline{SHDN}$	Shutdown – active low. Ground to power-down chip, tie to V+ for normal operation. Output voltage falls to 0V when $\overline{SHDN}$ is low.
2	3	VREF	Reference Voltage Output (+1.23V) supplies up to 100µA for external loads. Bypass to GND with a capacitor that does not exceed 0.047µF.
3	7	SS	Soft-Start. Capacitor between SS and GND provides SS and short-circuit protection. 510kΩ resistor from SS to $\overline{SHDN}$ provides current boost.
4	8	CC	MAX730/MAX738 Compensation Capacitor Input externally compensates the outer feedback loop. Connect to V_{OUT} with a 330pF capacitor.
			MAX750/MAX758 External voltage divider feedback point. When an external voltage divider is connected from the output voltage to CC and GND, this pin becomes the feedback input for adjustable output operation. A 330pF compensation capacitor must be used between the output voltage and the CC pin.
5	9	V_{OUT}	MAX730/MAX738 Output-Voltage Sense Input provides regulation feedback sensing. Connect to +5V output.
		I.C.	MAX750/MAX758 Internal Connection. Do not connect to anything.
6	10, 11	GND	Ground pins are internally connected.
7	12,13, 14	LX	Drain of internal P-channel power MOSFET.
8	1, 15, 16	V+	Supply Voltage Input. Bypass to GND with 0.1µF ceramic and large value electrolytic capacitors in parallel. The 0.1µF capacitor must be as close to the device as possible.
	4, 5, 6	N.C.	No Connect – no internal connections to these pins.

Operating Principle

The MAX730/738/750/758 switch-mode regulators use a current-mode pulse-width modulation (PWM) control system coupled with a simple buck regulator topography. They convert an unregulated DC voltage from the ranges specified in Table 1 to a lower voltage. The current-mode PWM architecture provides cycle-by-cycle current limiting, improved load transient response characteristics, and simpler outer-loop design.

Table 1. Input Voltage Range

PART	MIN (V)	MAX (V)
MAX730	5.2	11.0
MAX750	4.0	11.0
MAX738	6.0	16.0
MAX758	4.0	16.0

Detailed Description

The controller consists of two feedback loops: an inner (current) loop that monitors the switch current via the current-sense resistor and amplifier, and an outer (voltage) loop that monitors the output voltage through the error amplifier (Figure 1). The inner loop performs cycle-by-cycle current limiting, truncating the power transistor on-time when the switch current reaches a predetermined threshold. This threshold is determined by the outer loop. For example, a sagging output voltage produces an error signal that raises the threshold, allowing the circuit to store and transfer more energy during each cycle.

Programmable Soft-Start

Figures 1 and 2 show a capacitor and a resistor connected to the Soft-Start (SS) pin to ensure an orderly power-up. Typical values are 0.1µF and 510kΩ. SS controls both the SS timing and the maximum output

+5V and Adjustable Step-Down Current-Mode PWM Regulators

current that can be delivered while maintaining regulation.

The charging capacitor slowly raises the clamp on the error-amplifier output voltage, limiting surge currents at power-up by slowly increasing the cycle-by-cycle current-limit threshold. The 510Ω resistor sets the SS clamp at a value high enough to maintain regulation, even at currents exceeding 1A. This resistor is not necessary for lower current loads. Refer to *Typical Operating Characteristics, Maximum Output Current vs. Supply Voltage*. Table 2 lists timing characteristics for selected capacitor values and circuit conditions.

The output sags if more than the maximum load current is drawn, and the overcurrent comparator trips if the load exceeds approximately 1.5A. An SS cycle is actively initiated when either an undervoltage or overcurrent fault condition triggers an internal transistor to momentarily discharge the SS capacitor to ground. An SS cycle is also enabled at power-up and when coming out of the shutdown mode.

Overcurrent Limiting

When the load current exceeds approximately 1.5A, the output stage is turned off by the inner loop cycle-by-cycle current-limiting action, and the overcurrent comparator signals the control logic to initiate an SS cycle. On each clock cycle, the output FET turns on again and attempts to deliver current until cycle-by-cycle or overcurrent limits are exceeded. Note that the SS capacitor must be greater than 0.01µF for overcurrent protection to function properly.

Undervoltage Lockout

The undervoltage lockout feature monitors the supply voltage at V+ and allows operation to continue for supply voltages greater than 5.7V (typ) with 0.25V hysteresis for the MAX738 and 3.750V (typ) with 0.25V hysteresis for the MAX758 (see *Typical Operating Characteristics*,

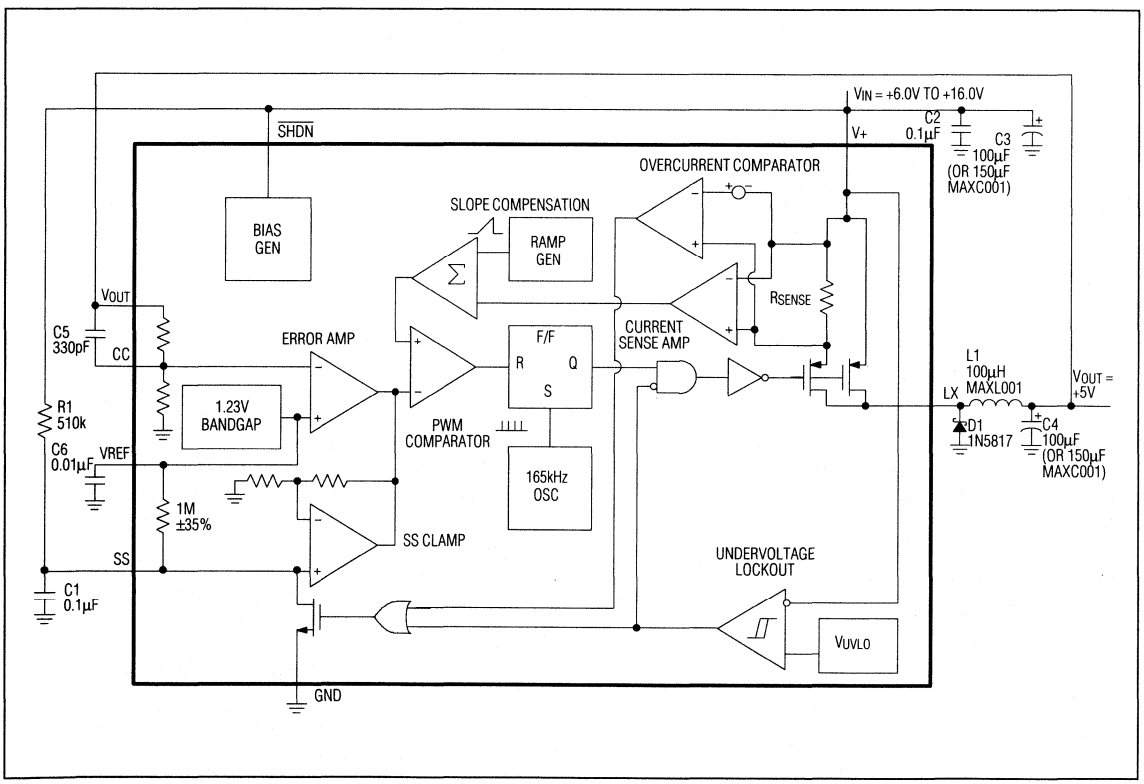


Figure 1. MAX730/MAX738 Detailed Block Diagram with External Components

Table 2. Typical Soft-Start Times

MAX730/MAX750 Circuit Conditions				Soft-Start Time (ms) vs. C1 (µF)			
R1 (kΩ)	V+ (V)	IOUT (mA)	C4 (µF)	0.01µF (ms)	0.047µF (ms)	0.1µF (ms)	0.47µF (ms)
510	6	0	100	2	6	11	28
510	9	0	100	1	4	6	15
510	11	0	100	1	2	4	11
510	9	150	100	1	4	8	21
510	9	300	100	1	5	9	27
510	9	150	390	3	6	9	23
510	9	150	680	4	6	9	24
none	6	0	100	16	34	51	125
none	9	0	100	10	22	34	82
none	11	0	100	8	18	28	66
none	9	150	100	34	134	270	1263
none	9	150	390	39	147	280	1275
none	9	150	680	40	152	285	1280

MAX738/MAX758 Circuit Conditions				Soft-Start Time (ms) vs. C1 (µF)			
R1 (kΩ)	V+ (V)	IOUT (mA)	C4 (µF)	0.01µF (ms)	0.047µF (ms)	0.1µF (ms)	0.47µF (ms)
510	7	0	100	1	4	6	18
510	12	0	100	1	2	3	8
510	16	0	100	1	1	2	6
510	12	300	100	1	3	5	3
510	12	750	100	1	5	8	21
none	7	0	100	12	27	40	100
none	12	0	100	7	16	25	54
none	16	0	100	6	13	20	68
none	12	300	100	27	112	215	1114

+5V and Adjustable Step-Down Current-Mode PWM Regulators

MAX738 Quiescent Supply Current vs. Supply Voltage). The MAX730 and MAX750 have a typical threshold of 4.7V and 3.75V, respectively. When an undervoltage condition is detected, control logic turns off the output power FET and discharges the SS capacitor to ground. This prevents partial turn-on of the power MOSFET and avoids excessive power dissipation. The control logic holds the output power FET off until the supply voltage rises above approximately 4.95V (MAX730), 5.95V (MAX738), and 3.95V (MAX750/MAX758), when an SS cycle begins.

Shutdown Mode

The MAX730/738/750/758 are held in shutdown mode by keeping $\overline{SHDN}$ at ground. In shutdown mode, the output drops to 0V and the output power FET is held in an off state. The internal reference also turns off, which causes the SS capacitor to discharge. Typical standby current in shutdown mode is 6µA. The actual design limit for standby current is much less than the 100µA specified in the *Electrical Characteristics* table. However, testing to tighter limits is prohibitive because the current takes several seconds to settle to a final value. For normal operation, connect $\overline{SHDN}$ to V+. Coming out of shutdown mode intiates an SS cycle.

Internal Reference

The +1.23V bandgap reference supplies up to 100µA at VREF. A bypass capacitor from VREF to GND is required and must not exceed 0.047µF.

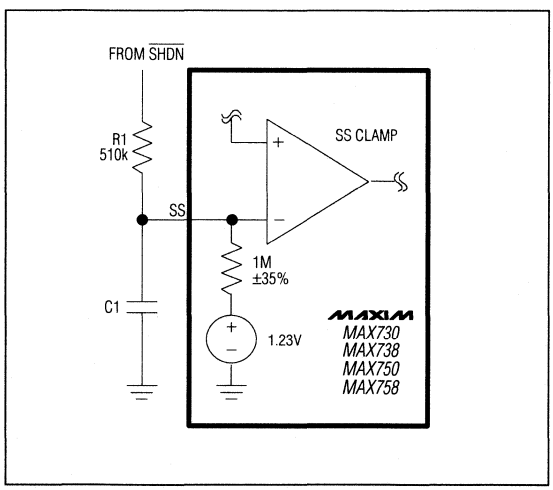


Figure 2. Block Diagram of Soft-Start Circuitry

Oscillator

The internal oscillators of the MAX730/MAX750 typically operate at 170kHz (160kHz for the MAX738/MAX758). Temperature stability over the military temperature range is about 0.06%/°C.

Application Information

Fixed +5V and Adjustable Output Step-Down Converter Application

Figure 3 shows both the standard 5V and the adjustable step-down application circuits. These circuits are useful in systems that require high current and high efficiency and are powered by an unregulated supply, such as a battery or wall-plug AC-DC transformer. These circuits will operate over the entire line, load, and temperature ranges using the single set of component values shown. All components shown are suitable for the MAX730/738/750/758. The actual value of the input and output capacitors is not critical as long as it is greater than 100µF, has low ESR, and has sufficient voltage rating.

The MAX738/MAX758 deliver a guaranteed 5V at 300mA for supply voltages of 6.6V to 16.0V, and a guaranteed 5V at 750mA for supply voltages of 10.2V to 16.0V. The MAX738/MAX758 operate from supplies down to 6.0V and 4.0V, respectively (the upper limit of undervoltage lockout), but some reduction of the maximum output current may occur. The MAX730/MAX750 input voltages can be as low as 5.2V and 4.0V respectively, but the maximum output current may also be lower.

Inductor Selection

The MAX730/MAX738 require no inductor design because they are tested in-circuit, and are guaranteed to deliver the power specified in the *Electrical Characteristics* with high efficiency using a single 100µH inductor. The 100µH inductor's incremental saturation current rating should be greater than 1A for 750mA load operation. Table 3 shows recommended inductor types and suppliers for various applications. 100µH through-hole inductors (MAXL001) are available from Maxim in production quantities. The surface-mount inductors have nearly equivalent efficiencies to the larger-sized through-hole inductors.

Adjustable Output

For other output voltages, the MAX750/MAX758 have adjustable outputs from 1.25V to the input voltage. To adjust for other output voltages, connect a voltage divider to the compensation capacitor input (CC) pin as shown in Figure 3.

The output voltage is set by R2 and R3 as follows:

Let R3 be any resistance in the 10kΩ to 1MΩ range, typically 100kΩ, then:

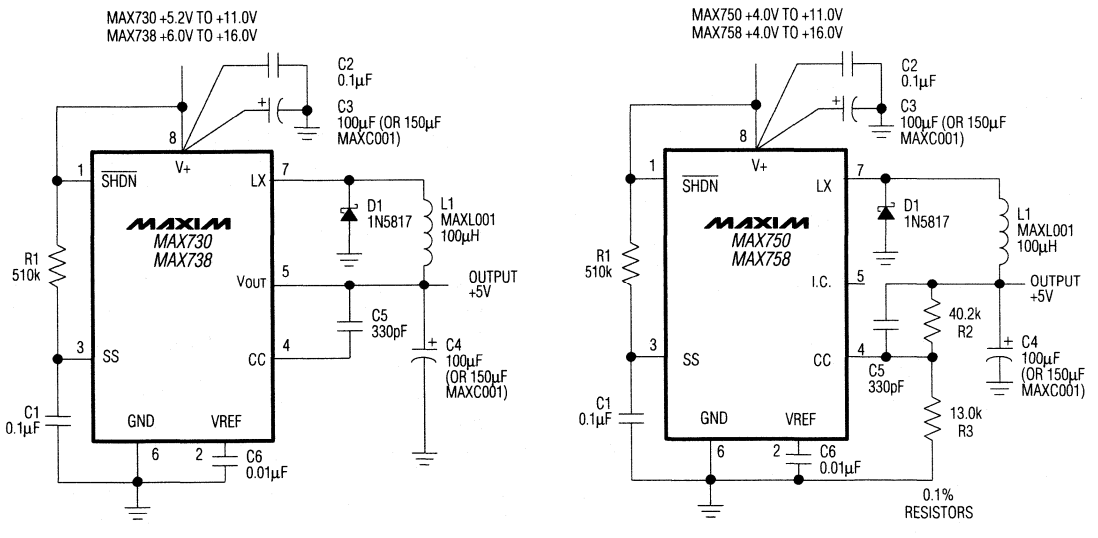
$$R2 = R3 \left(\frac{V_{OUT}}{1.23V} - 1 \right)$$

Output tolerance over temperature is ±4.5% plus external resistor tolerances.

Low Input Supply Voltage Operation

A unique aspect of the these devices is that they are guaranteed to deliver their specified power even at low input voltages. Normally, the output voltage ripples at the converter switching frequency. For a 5V output and at supply voltages less than about 6.8V (MAX730/MAX750) or 7.6V (MAX738/MAX758), the output ripple is no longer at the switching frequency only, but also at subharmonics of the switching frequency. Efficiency and regulation are unchanged under these conditions, but if this subharmonic ripple is undesirable, a smaller (18µH) inductor value may be appropriate.

To minimize subharmonic output ripple over the entire low supply voltage range of the MAX738/MAX758 (6.6V to 10.2V, up to 300mA), a single inductor value of 18µH can be used in combination with a larger output filter capacitor (1000µF). Using the 18µH inductor results in about a 5% to 10% efficiency drop when compared to the 100µH inductor. The subharmonic output ripple at low input voltages in the MAX730/MAX750 is not remedied by this solution.



Part	Input Supply Range (V)	Guaranteed Output Current at 5V (mA)
MAX730/ MAX750	6.0 to 11.0	300
MAX738/ MAX758	6.6 to 16.0	300
	10.2 to 16.0	750

NOTE: PIN NUMBERS REFER TO 8-PIN PACKAGES

Figure 3. Standard +5V Step-Down Application Circuit

+5V and Adjustable Step-Down Current-Mode PWM Regulators

Table 3. Component Suppliers

Production Method	Inductors	Capacitors
Surface Mount	Sumida (708) 956-0666 CD54-101KC (MAX730) CD105-101KC (MAX738) Coiltronics (305) 781-8900 CTX100-series	Matsuo (714) 969-2491 267-series
Miniature Through-Hole	Sumida (708) 956-0666 RCH654-101K (MAX730) RCH895-101K (MAX738)	Sanyo (619) 661-6322 OS-CON-series Low ESR Organic Semiconductor
Low-Cost Through-Hole	Maxim MAXL001 100µH Iron-Powder Toroid Renco (516) 586-5566 RL1284-100	Maxim MAXC001 150µF, Low ESR Electrolytic Nichicon (708) 843-7500 PL-series Low ESR Electrolytics United Chemicon (708) 696-2000 LXF-series

Output Filter Capacitor Selection

The primary criterion for selecting the output filter capacitor is low equivalent series resistance (ESR). The product of the inductor current variation and the ESR of the output capacitor determines the amplitude of the sawtooth ripple seen on the output voltage. In addition, the ESR of the output filter capacitor should be minimized to maintain AC stability. The ESR of the capacitor should be less than 0.25Ω to keep the output ripple less than 50mVp-p over the entire current range (using a 100µH inductor). The ESR of capacitors goes up as the capacitor temperature goes down. For this reason, ESR must be considered for operation at less than 0°C to keep ripple at an acceptable level. Refer to Table 3 for suggested capacitor suppliers.

Other Components

The catch diode should be a Schottky or high-speed silicon rectifier with a peak current rating of at least 1.5A for full-load (750mA) operation. The 1N5817 is a good choice. The 330pF outer-loop compensation capacitor provides the widest input voltage range and best transient characteristics. For low-current applications, the 510kΩ resistor may be omitted (see *Typical Operating Characteristics, Maximum Output Current vs. Supply Voltage, No R1*).

Printed Circuit Layouts

A good layout is essential for clean, stable operation. The layouts and component placement diagrams given in Figures 4, 5, 6, and 7 have been successfully tested over a wide range of operating conditions. This board layout is configured for a fixed +5V output, but can be modified for the MAX750/MAX758 adjustable output. To configure for adjustable output voltages: 1. Turn the board solder side up. 2. Cut the trace between the two through holes at pin 5. 3. Determine the value of R2 and R3. 4. Install at these positions. Note that the 0.1µF input bypass capacitor must be positioned as close to the pins as possible. Also, the output capacitor should be as close to the V_{OUT} and GND pins as possible. The traces connecting ground to the input and output filter capacitors and to the catch diode must be short to reduce inductance.

Thermal Considerations

The MAX730/738/750/758 do not require a heat sink for normal operation. Operation at load currents above those guaranteed in the Electrical Characteristics may require a heat sink. The ambient temperature plus the temperature rise caused by power dissipation in the device must not exceed the junction temperature ratings (see *Absolute Maximum Ratings*). The junction-to-air thermal coefficients of the packages are +105°C/W (16-pin wide SO), +125°C/W (8-pin CERDIP), +120°C/W (8-lead plastic DIP), +170°C/W (8-pin SO). The temperature rise of the device is the product of the thermal coefficient and the power dissipated in the device.

Output-Ripple Filtering

A simple lowpass pi-filter (Figure 3) can be added to the output to reduce output ripple to about 5mVp-p. The cutoff frequency shown is 21kHz. Since the filter inductor is in series with the circuit output, its resistance should be kept to a minimum so the voltage drop across it is not excessive.

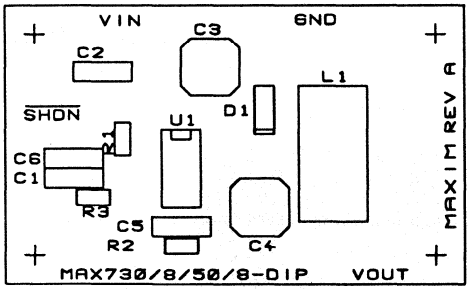


Figure 4. DIP PC Layout, Through-Hole Component Placement Diagram (1X Scale)

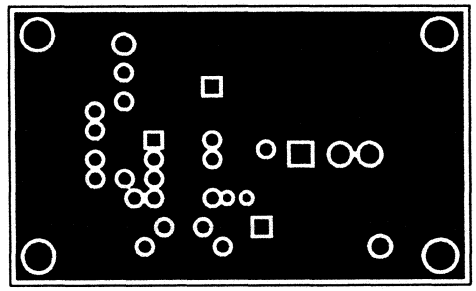


Figure 5. DIP PC Layout, Component Side (1X Scale)

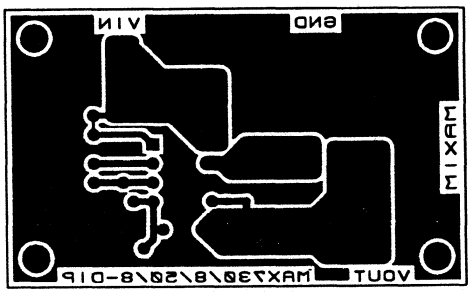


Figure 6. DIP PC Layout, Solder Side (1X Scale)

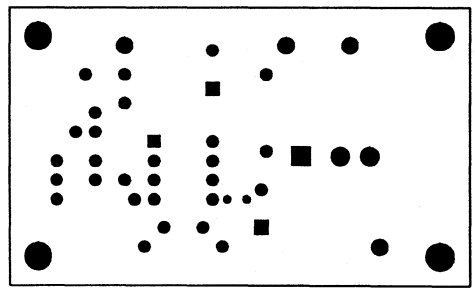


Figure 7. DIP PC Layout, Drill Guide (1X Scale)

+5V and Adjustable Step-Down Current-Mode PWM Regulators

_ Ordering Information (continued)

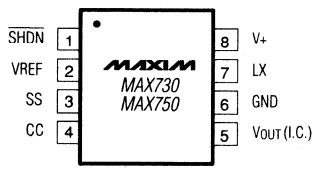
PART	TEMP. RANGE	PIN-PACKAGE
MAX750CPA	0°C to +70°C	8 Plastic DIP
MAX750CSA	0°C to +70°C	8 SO
MAX750C/D	0°C to +70°C	Dice*
MAX750EPA	-40°C to +85°C	8 Plastic DIP
MAX750ESA	-40°C to +85°C	8 SO
MAX750MJA	-55°C to +125°C	8 CERDIP**
MAX758CPA	0°C to +70°C	8 Plastic DIP
MAX758CWE	0°C to +70°C	16 Wide SO
MAX758C/D	0°C to +70°C	Dice*
MAX758EPA	-40°C to +85°C	8 Plastic DIP
MAX758EWE	-40°C to +85°C	16 Wide SO
MAX758MJA	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

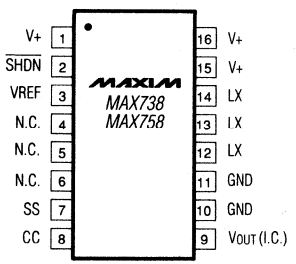
____ Pin Configurations (continued)

TOP VIEW



SO

NOTE: ( ) ARE FOR MAX750.

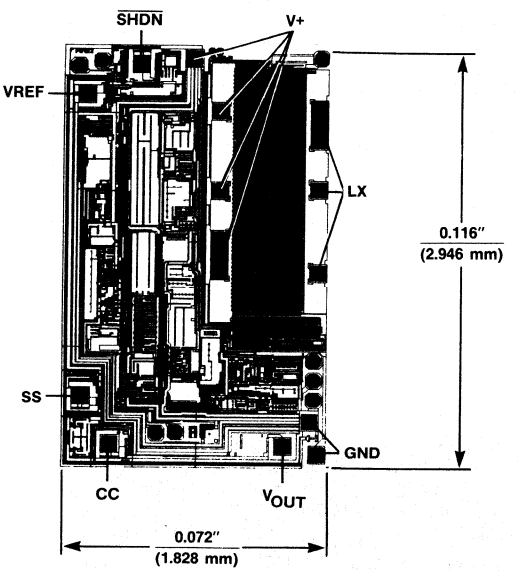


WIDE SO

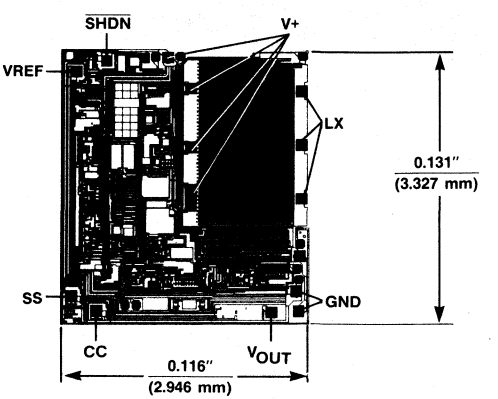
NOTE: ( ) ARE FOR MAX758.

_____ Chip Topographies

MAX730/MAX750



MAX738/MAX758



NOTES: ( ) ARE FOR MAX750/MAX758, DO NOT USE.
CONNECT SUBSTRATE TO V+.
TRANSISTOR COUNT 274 (MAX730/MAX750)
286 (MAX738/MAX758)

19-4672; Rev 1; 7/92

EVALUATION KIT AVAILABLE

MAXIM

+5V/Adjustable Step-Up Current-Mode DC-DC Converters

General Description

The MAX731 and MAX752 are fixed and adjustable CMOS, step-up, DC-DC switch-mode regulators. The MAX731 accepts a positive input voltage between +2.5V and +5.25V and converts it to a fixed +5V at 200mA, guaranteed over temperature. Typical full-load efficiencies are 82% to 87%. It requires a single inductor value of 22µH to function over the entire range, so no inductor-related design is necessary. The MAX752 is an adjustable version that converts a minimum of +1.8V to any higher voltage up to +15V, at up to 200mA. Typical full-load efficiencies are 85% to 95%. A single 50µH inductor is suitable for the entire range of operating conditions, so no inductor-related design is necessary.

The MAX731/MAX752 use current-mode pulse-width modulation (PWM) controllers to provide precise output regulation and low subharmonic noise. Typical no-load supply current is 2mA. A fixed 170kHz oscillator frequency allows easy filtering of ripple and noise, and provides for small external components.

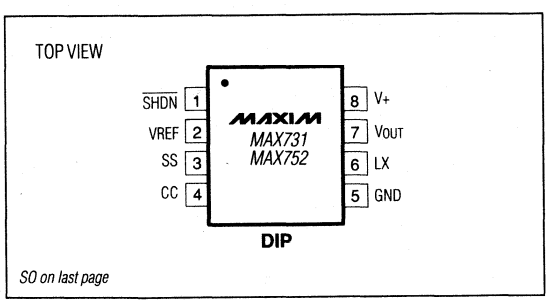
The MAX731/MAX752 feature cycle-by-cycle current limiting, overcurrent limiting, external shutdown, and programmable soft-start protection.

For fixed +12V and +15V step-up regulators, refer to the MAX732/MAX733 data sheet. For lower-power step-up applications, refer to the MAX631/632/633 and MAX654-659 data sheets.

Applications

+5V-Logic Supply in +3V-Logic System
DC-DC Converter Module Replacement
Portable Instruments
Laptop Computers
Distributed Power Systems
Cellular Phones
Battery-Powered Equipment

Pin Configurations



SO on last page

Features

- ♦ 200mA Load Currents Guaranteed with No External MOSFET
- ♦ Step-Up from a 2.5V Input
- ♦ 170kHz High-Frequency Current-Mode PWM
- ♦ 82% to 87% Typical Efficiencies at Full Load (MAX731)
- ♦ 85% to 95% Typical Efficiencies at Full Load (MAX752)
- ♦ Small Inductor - No Component Design Required
- ♦ 2mA Quiescent Current (MAX752)
- ♦ Overcurrent and Soft-Start Protection
- ♦ 8-Pin DIP, 16-Pin Wide SO Packages
- ♦ Shutdown Pin

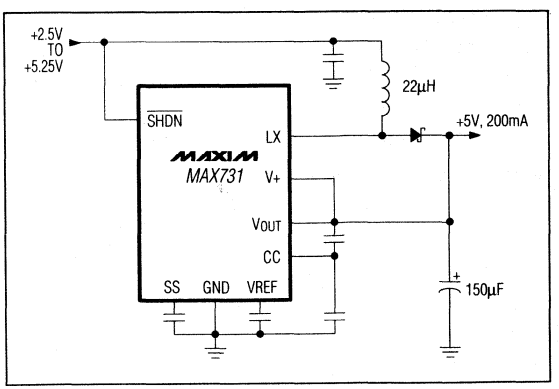
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX731CPA	0°C to +70°C	8 Plastic DIP
MAX731CWE	0°C to +70°C	16 Wide SO
MAX731C/D	0°C to +70°C	Dice*
MAX731EPA	-40°C to +85°C	8 Plastic DIP
MAX731EWE	-40°C to +85°C	16 Wide SO
MAX731MJA	-55°C to +125°C	8 CERDIP

Ordering information continued on last page.

* *Dice are tested at T_A = +25°C only.*
***Contact factory for availability and processing to MIL-STD-883.*

Typical Application Circuit



+5V/Adjustable Step-Up Current-Mode DC-DC Converters

ABSOLUTE MAXIMUM RATINGS

V+, LX to GND ..... -0.3V to +17V
V_{OUT} to GND ..... ±25V
SS, CC, SHDN to GND ..... -0.3V to (V+ + 0.3V)
Peak Switch Current (I_{LX}) 1.5A
Reference Current (I_{VREF}) 2.5mA
Continuous Power Dissipation (T_A = +70°C)
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) . 727mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) ... 640mW

Operating Temperature Ranges:
MAX731/752C_ _ ..... 0°C to +70°C
MAX731/752E_ _ ..... -40°C to +85°C
MAX731/752MJA ..... -55°C to +125°C
Junction Temperatures:
MAX731/752C_ _/E_ _ ..... +150°C
MAX731/752MJA ..... +175°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS - MAX731

(Circuit of Figure 1a, V_{IN} = +3V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Start-Up Input Voltage	I_{LOAD} = 0mA		1.8		V
	I_{LOAD} = 200mA		2.0	2.5	
Minimum Operating Voltage, V_{IN}	I_{LOAD} = 100mA		1.4		V
	I_{LOAD} = 200mA		2.0		
Output Voltage (Note 1)	V_{IN} = 2.7V to 4.65V, 0mA < I_{LOAD} < 200mA	4.75	5.00	5.25	V
Output Current		200			mA
Line Regulation	V_{IN} = 2.7V to 4.65V		0.20		%/V
Load Regulation	I_{LOAD} = 0mA to 100mA		0.005		%/mA
Efficiency	V_{IN} = 3V, I_{LOAD} = 100mA		87		%
Supply Current	Includes switch current		2.0	4.0	mA
Standby Current	$\overline{SHDN}$ = 0, entire circuit		35	100	µA
	$\overline{SHDN}$ = 0, into V+		6		
Shutdown Input Threshold	V_{IH}	V+ - 0.5			V
	V_{IL}			0.25	
Shutdown Input Leakage Current				1.0	µA
Short-Circuit Current			1.5		A
LX On Resistance			0.5		Ω
LX Leakage Current	V_{DS} = 5V		1.0		µA
Reference Voltage		1.15	1.23	1.30	V
Reference Drift	T_A = T_{MIN} to T_{MAX}		50		ppm/°C
Oscillator Frequency		125	170	215	kHz
Compensation Pin Impedance			20		kΩ

Note 1: Circuit will regulate properly with input voltage as high as 5.25V due to voltage drop across the external diode.

ELECTRICAL CHARACTERISTICS - MAX752

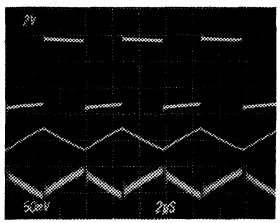
(Circuit of Figure 1b, R1 and R2 configured for +12V output operation, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	I_{LOAD} = 0mA			1.8	2.5	V
Output Voltage	V+ = 4.5V to 11.0V, 0mA < I_{LOAD} < 150mA	MAX752C/E	11.46	12.0	12.54	V
	V+ = 4.5V to 11.0V, 0mA < I_{LOAD} < 125mA	MAX752M	11.46	12.0	12.54	
	V+ = 6.0V to 11.0V, 0mA < I_{LOAD} < 200mA	MAX752C/E/M	11.46	12.0	12.54	
Output Current	V+ = 4.5V to 11.0V	MAX752C/E	150			mA
		MAX752M	125			
	V+ = 6.0V to 11.0V	MAX752C/E/M	200			
Output Voltage Range	$V_{IN} \leq V_{OUT}$		2.7		15.75	V
Line Regulation	V+ = 4.0V to 11.0V			0.20		%/V
Load Regulation	I_{LOAD} = 0mA to 100mA			0.0035		%/mA
Efficiency	V+ = 5V, I_{LOAD} = 100mA			88		%
Supply Current	Includes switch current			1.7	3.0	mA
Standby Current	$\overline{SHDN}$ = 0, entire circuit			70	100	µA
	$\overline{SHDN}$ = 0, into V+			6		
Shutdown Input Threshold	V_{IH}		V+ - 0.5			V
	V_{IL}				0.25	
Shutdown Input Leakage Current					1.0	µA
Short-Circuit Current				1.5		A
LX On Resistance				0.5		Ω
LX Leakage Current	V_{DS} = 12V			1.0		µA
Reference Voltage			1.15	1.23	1.30	V
Reference Drift	T_A = T_{MIN} to T_{MAX}			50		ppm/°C
Oscillator Frequency			130	170	210	kHz

+5V/Adjustable Step-Up Current-Mode DC-DC Converters

Typical Operating Characteristics

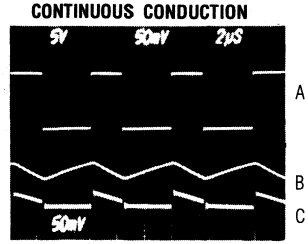
MAX731
SWITCHING WAVEFORMS
CONTINUOUS CONDUCTION



2µs/div

A: Switch Voltage (LX pin), 2V/div, 0V to +5V
B: Inductor Current, 500mA/div
C: Output Voltage Ripple, 50mV/div
Circuit of Fig. 2a, C_{OUT} = 150µF, V+ = 3V, I_{OUT} = 200mA, T_A = +25°C

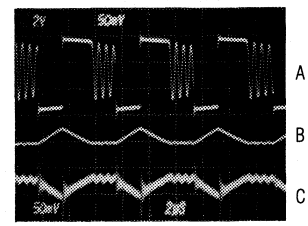
MAX752
SWITCHING WAVEFORMS
CONTINUOUS CONDUCTION



2µs/div

A: Switch Voltage (LX pin), 5V/div, 0V to +12.4V
B: Inductor Current, 500mA/div
C: Output Voltage Ripple, 50mV/div
Circuit of Fig. 2b, C_{OUT} = 300µF, V+ = 3V, I_{OUT} = 100mA, T_A = +25°C

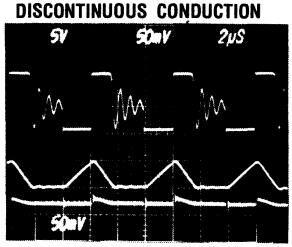
MAX731
SWITCHING WAVEFORMS
DISCONTINUOUS CONDUCTION



2µs/div

A: Switch Voltage (LX pin), 2V/div, 0V to +5V
B: Inductor Current, 500mA/div
C: Output Voltage Ripple, 50mV/div
Circuit of Fig. 2a, C_{OUT} = 150µF, V+ = 3V, I_{OUT} = 100mA, T_A = +25°C

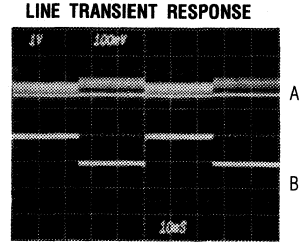
MAX752
SWITCHING WAVEFORMS
DISCONTINUOUS CONDUCTION



2µs/div

A: Switch Voltage (LX pin), 5V/div, 0V to +12.4V
B: Inductor Current, 200mA/div
C: Output Voltage Ripple, 50mV/div
Circuit of Fig. 2b, C_{OUT} = 300µF, V+ = 3V, I_{OUT} = 200mA, T_A = +25°C

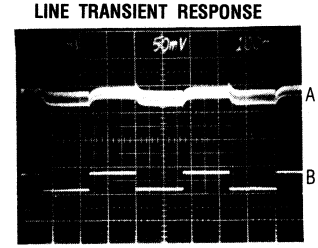
MAX731
LINE TRANSIENT RESPONSE



10ms/div

A: V_{OUT}, 100mV/div
B: V_{IN}, 2V to 3V
Circuit of Fig. 2a, I_{LOAD} = 200mA
T_A = +25°C

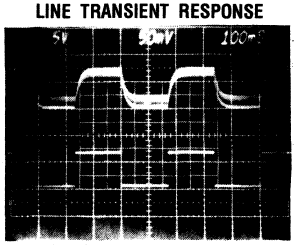
MAX752
LINE TRANSIENT RESPONSE



100µs/div

A: V_{OUT}, 50mV/div, DC-Coupled
B: V+, 5V/div, 6.0V to 9.0V
Circuit of Fig. 2b, I_{OUT} = 200mA, V_{OUT} = 12V
T_A = +25°C

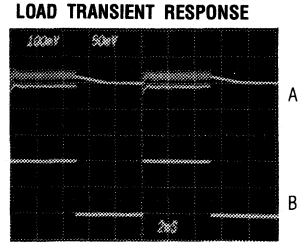
MAX752
LINE TRANSIENT RESPONSE



100µs/div

A: V_{OUT}, 50mV/div, DC-Coupled
B: V+, 5V/div, 6.0V to 12.0V
Circuit of Fig. 2b, I_{OUT} = 125mA, V_{OUT} = 15V, T_A = +25°C

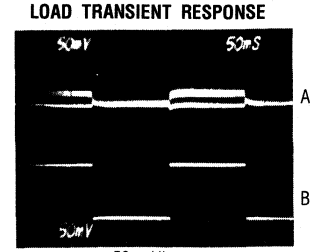
MAX731
LOAD TRANSIENT RESPONSE



2ms/div

A: V_{OUT},100mV/div
B: I_{OUT}, 100mA/div
Circuit of Fig. 2a, T_A = +25°C

MAX752
LOAD TRANSIENT RESPONSE

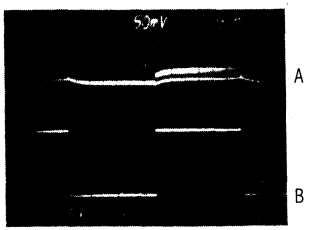


50µs/div

A: V_{OUT}, 50mV/div, DC-Coupled
B: I_{OUT}, 100mA/div, 10mA to 200mA
Circuit of Fig. 2b, V+ = +6V, T_A = +25°C
V_{OUT} = 12V

Typical Operating Characteristics (continued)

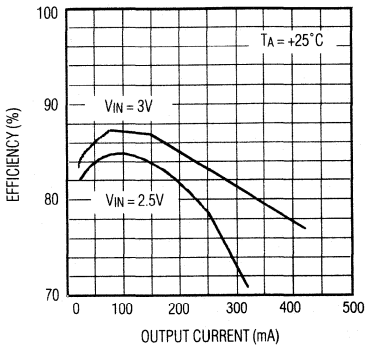
MAX752
LOAD TRANSIENT RESPONSE



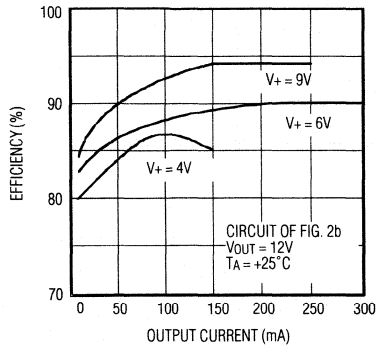
50µs/div

A: VOUT, 50mV/div, D-C Coupled
B: IOUT, 50mA/div, 10mA to 125mA
Circuit of Fig. 2b, V+ = +6V, TA = +25°C
VOUT = 15V

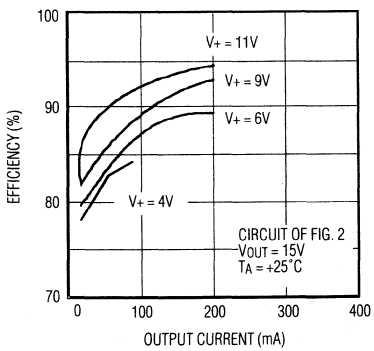
MAX731
EFFICIENCY vs. OUTPUT CURRENT



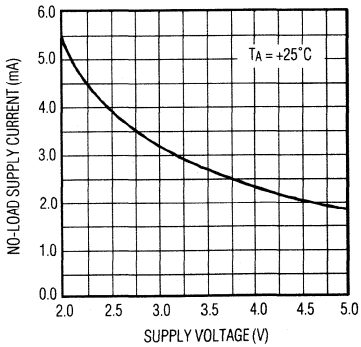
MAX752
EFFICIENCY vs. OUTPUT CURRENT



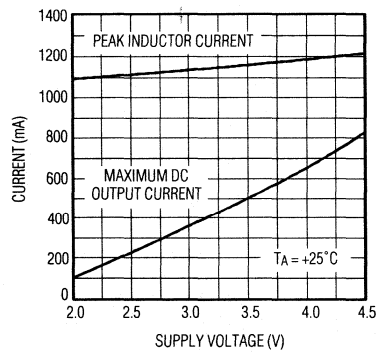
MAX752
EFFICIENCY vs. OUTPUT CURRENT



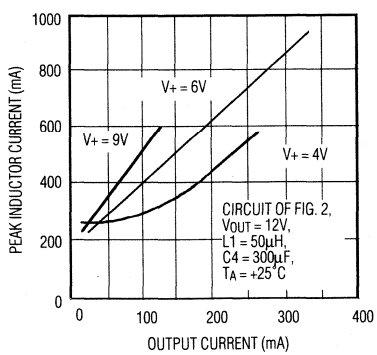
MAX731
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



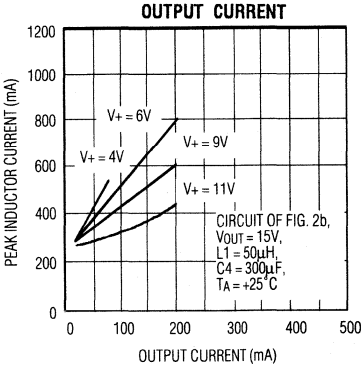
MAX731
PEAK INDUCTOR CURRENT AND MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



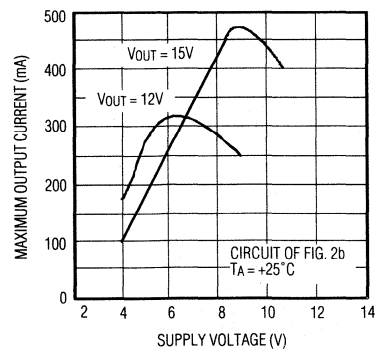
MAX752 PEAK INDUCTOR CURRENT vs. OUTPUT CURRENT



MAX752
PEAK INDUCTOR CURRENT vs. OUTPUT CURRENT



MAX752 MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



+5V/Adjustable Step-Up Current-Mode DC-DC Converters

Table 1a. MAX731 Typical Soft-Start Times

V_{IN} = 3V, C_{OUT} = 150µF	
C_{SS} (µF)	Delay (ms)
0.1	10
0.2	20
0.5	50
1.0	100
2.0	160
5.0	170

NOTE: SOFT-START TIMES ARE ±35%. C1 IS THE SOFT-START CAPACITOR; C4 IS THE OUTPUT CAPACITOR

Table 1b. MAX752 Typical Soft-Start Times

CIRCUIT CONDITIONS V_{OUT} = +12V, C4 = 300µF		SOFT-START TIME (ms) vs. C1 (µF)		
V+ (V)	I_{OUT} (mA)	0.1µF	0.47µF	1.0µF
4.5	0	55	115	125
6.0	0	40	80	70
9.0	0	30	60	45
4.5	100	90	350	780
6.0	100	60	210	445
9.0	100	30	60	60
4.5	200	175	715	1690
6.0	200	85	340	760
9.0	200	30	75	125

CIRCUIT CONDITIONS V_{OUT} = +15V, C4 = 300µF		SOFT-START TIME (ms) vs. C1 (µF)		
V+ (V)	I_{OUT} (mA)	0.1µF	0.47µF	1.0µF
4.5	0	90	210	250
6.0	0	65	135	150
9.0	0	35	65	50
12.0	0	30	50	35
4.5	75	155	680	1380
6.0	75	105	425	880
9.0	75	45	160	305
12.0	75	30	50	35
4.5	125	235	1125	2260
6.0	125	135	595	1255
9.0	125	55	230	475
12.0	125	30	50	40

NOTE: SOFT-START TIMES ARE ±35%. C1 IS THE SOFT-START CAPACITOR; C4 IS THE OUTPUT CAPACITOR

Pin Description

8-PIN DIP	16-PIN SO	NAME	FUNCTION
	1, 4, 10, 15	N.C.	No Connect - no internal connection
1	2	$\overline{SHDN}$	Shutdown - active low. Ground to power-down the IC; tie to V+ for normal operation. Output power FET is held off when SHDN is low.
2	3	VREF	Reference Voltage Output (+1.23V) supplies up to 100µA for external loads.
3	5	SS	Soft-Start. Capacitor between SS and GND provides soft-start and short-circuit protection.
4	6	CC	Compensation Capacitor Input. Externally compensates the outer feedback loop.
5	7	GND	Ground
	8, 9	GND (SW)	Switch Ground - ground of the output power FET. Both pins must be separately tied to ground because they are not internally connected.
6	11, 12, 13	LX	Drain of internal N-channel power MOSFET
7	14	VOUT	Output-Voltage Sense Input
8	16	V+	Supply Voltage Input

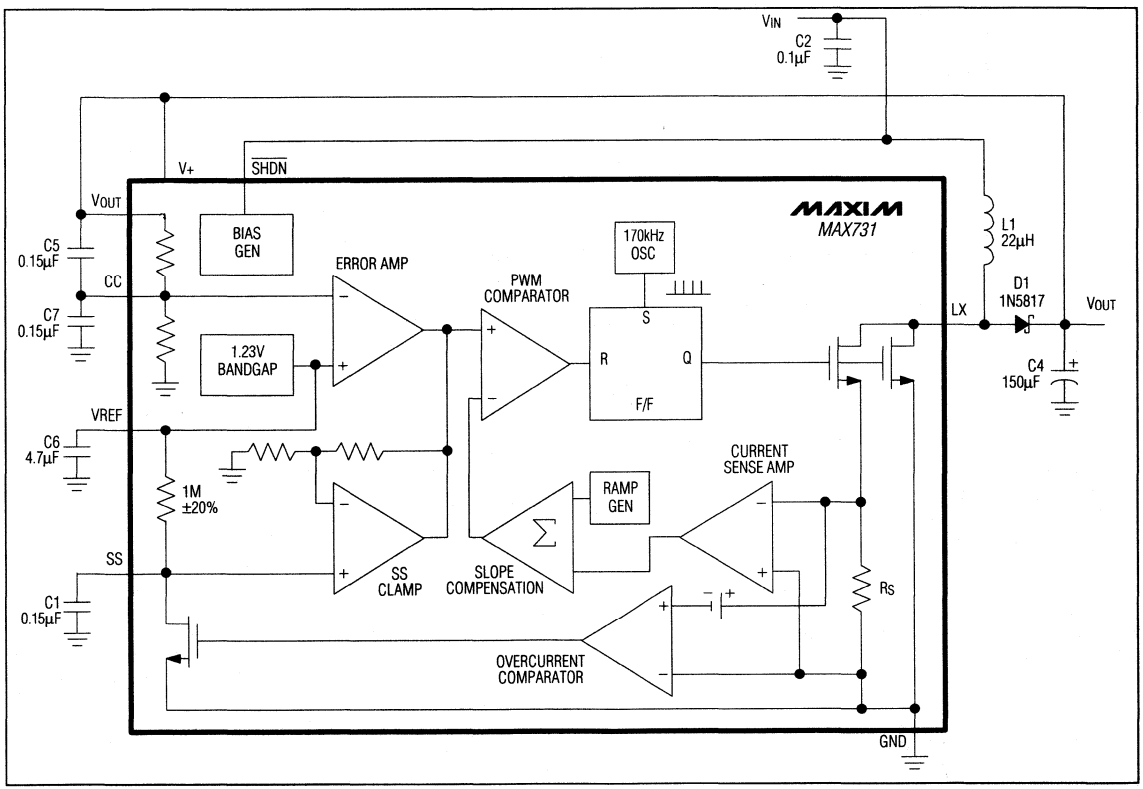


Figure 1a. MAX731 Detailed Block Diagram with External Components, Bootstrap Mode

+5V/Adjustable Step-Up Current-Mode DC-DC Converters

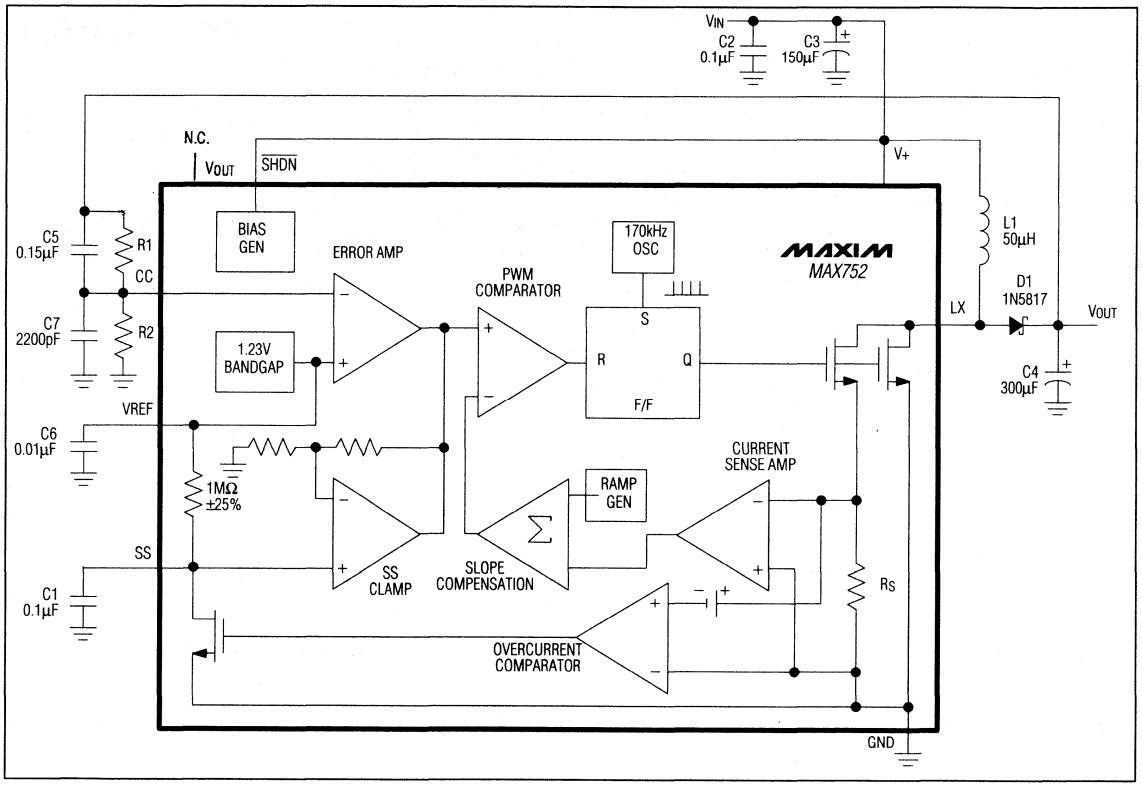


Figure 1b. MAX752 Detailed Block Diagram with External Components, Optimized for 12V Output.

Detailed Description

The input voltage range has three important components: no-load starting voltage, full-load starting voltage and minimum operating voltage. The no-load starting voltage is usually less than 2.0V, but if a load is added, the circuit may not start. At a slightly higher voltage, more current can be drawn, and the output voltage will rise to the regulated value. With a 2.5V input voltage, the MAX731 will start up and regulate with a 200mA load. The MAX752 will start up and regulate at 12V at 150mA from a minimum input voltage of 4.5V.

The MAX731 has a "bootstrapped" output, which means it operates from the output that it generates. Once it generates 5V, it then operates from this 5V, and subsequently can furnish 200mA from an input as low as 2.0V (the holding voltage). The holding voltage is typically 1.4V for 100mA loads. This capability is very important in battery-operated equipment, because it indicates the voltage to which the battery can discharge without losing output regulation.

Input voltages as high as 16V can be applied without damage, but regulation is lost when the input exceeds the normal regulated output. This happens because a DC path through the inductor and diode produces an output voltage one diode drop (0.3-0.6V) less than the input voltage. (The MAX731/MAX752 sense this high output and stop switching.) This path exists even with the IC removed from the circuit.

+5V/Adjustable Step-Up Current-Mode DC-DC Converters

Operating Principle

The MAX731/MAX752 switch-mode regulators use a current-mode pulse-width modulation (PWM) controller coupled with a simple boost regulator topography to step up an unregulated DC voltage. The MAX731 converts a voltage ranging from 1.4V to 5.25V to 5V. The MAX752 has an adjustable output. The current-mode PWM architecture provides cycle-by-cycle current limiting and excellent load-transient response characteristics.

The controller consists of two feedback loops: an inner (current) loop that monitors the switch current through the current-sense resistor (RS) and amplifier, and an outer (voltage) loop that monitors the output voltage through the error amplifier (Figure 1). The inner loop performs cycle-by-cycle current limiting, truncating the power transistor on-time when the switch current reaches a threshold determined by the outer loop. For example, a sagging output voltage produces an error signal that raises the threshold, allowing the circuit to store and transfer more energy during each cycle.

Programmable Soft Start

A capacitor between 0.1µF and 5µF is required on the Soft-Start (SS) pin to ensure an orderly power-up. The charging capacitor's voltage slowly raises the clamp on the error-amplifier output voltage, limiting surge currents at power-up by slowly increasing the cycle-by-cycle current-limit threshold. SS timing is controllable from the SS pin by capacitor choice. A typical value is 0.1µF. Table 1 lists timing characteristics for selected capacitor values and circuit conditions.

The output voltage sags if more than the maximum load current is drawn. The overcurrent comparator trips if the load exceeds approximately 1.5A. An SS cycle is actively initiated when an overcurrent fault condition triggers an internal transistor to discharge the SS capacitor to ground.

Overcurrent Limiting

When the load current exceeds approximately 1.5A, the output stage is turned off by the inner loop cycle-by-cycle current-limiting action, and the overcurrent comparator signals the control logic to initiate an SS cycle. On each clock cycle, the output FET turns on again and attempts to deliver current until cycle-by-cycle or overcurrent limits are exceeded. Note that the SS capacitor must be at least 0.01µF for overcurrent protection to function properly.

Shutdown

Keeping the Shutdown ($\overline{SHDN}$) pin at ground holds the MAX731/MAX752 in shutdown mode. In shutdown mode, the output power FET is off, but there is still an external path from V+ to the load through the inductor and diode, and another path from V+ to GND through the inductor, diode, and external feedback resistors. For the MAX731, the feedback resistors are approximately 80kΩ. The internal reference turns off, which causes the SS capacitor to discharge. Typical device standby current in shutdown mode is 35µA. For normal operation, connect $\overline{SHDN}$ to V+. An SS cycle brings the MAX731 out of shutdown mode.

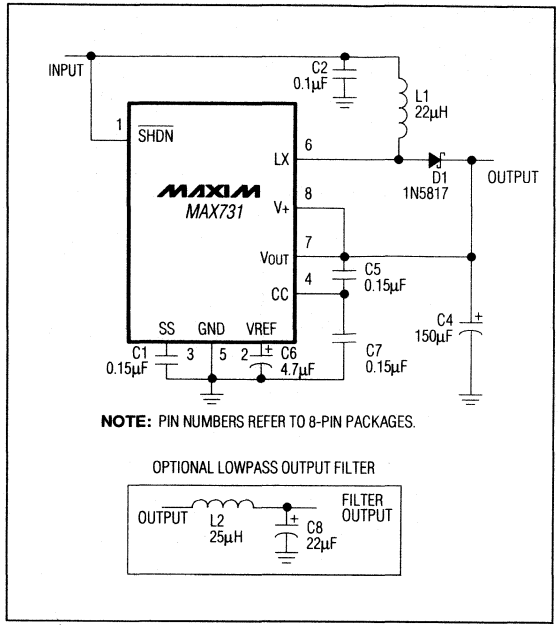


Figure 2a. MAX731 Standard Boost Application Circuit

The +1.23V bandgap reference supplies up to 100µA at VREF. A bypass capacitor from VREF to GND is required: 4.7µF for the MAX731 and 0.01µF for the MAX752.

Output Adjustment - MAX752

The output voltage for the MAX752 is set by two resistors, R1 and R2 (Figures 1b and 2b), which form a voltage divider between the output and the Compensation Capacitor (CC) pin. The regulator adjusts the output so the voltage at the junction of R1 and R2 is equal to the +1.23V bandgap reference voltage. Since CC is a CMOS input, its input impedance is nearly an open circuit, which will not load the voltage divider. R2 can be any value between 10kΩ to 30kΩ. R1 is given by the formula:

$$R1 = R2\left(\frac{V_{OUT}}{1.23V} - 1\right)$$

Capacitors C5 and C7 furnish loop compensation. Smaller values are not recommended because they may produce instability.

+5V/Adjustable Step-Up Current-Mode DC-DC Converters

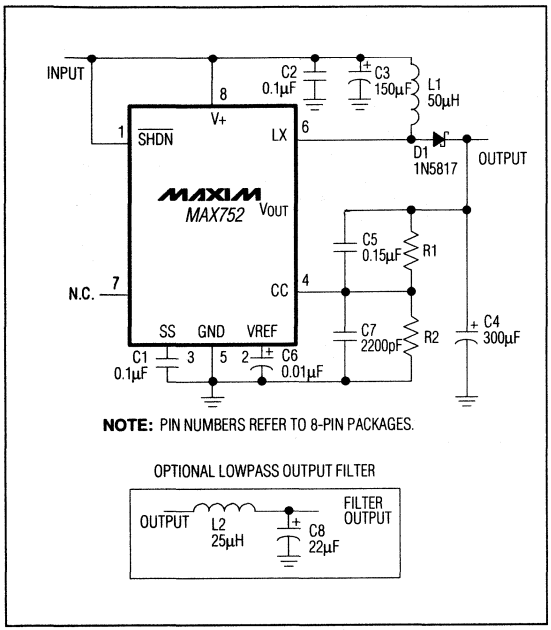


Figure 2b. MAX752 Standard Boost Application Circuit

Modes

Continuous-Current Mode: The MAX731/MAX752 normally operate in continuous-current mode, which means current always flows in the inductor, and the control circuit adjusts the switch's duty cycle on a cycle-by-cycle basis to maintain regulation without exceeding the switch current capability. This mode provides excellent load-transient response. During start-up conditions and under very light loads, this method cannot adjust the duty cycle to the correct value without exceeding the switch current capability, so the controller changes to discontinuous-current mode.

Discontinuous-Current Mode: In discontinuous-current mode, current through the inductor starts at zero, rises to a peak value, then ramps down to zero on each cycle. Although efficiency is still excellent, the output ripple increases slightly and the switch waveforms display ringing (the inductor's self-resonant frequency). This ringing may seem disconcerting at first, but it does not indicate problems.

Pulse-Skipping Mode: At load currents under a few milliamperes, even discontinuous-current mode tends to put more energy into the coil than the load requires, so the controller changes to pulse-skipping mode, in which regulation is achieved by skipping entire cycles. Efficiency is still good, typically 70% to 80%, reduced in part because the MAX731/MAX752 quiescent supply current becomes a significantly larger fraction of the total current when load currents are low. Pulse-skipping switch waveforms can be irregular, and the output ripple contains a low-frequency component that may exceed 50mV. Larger, low-ESR filter capacitors can help reduce the ripple voltage in critical applications.

The MAX731/MAX752 controller normally operates in continuous-current mode and reverts to discontinuous-current mode or pulse-skipping mode during extreme conditions. Continuous-current mode operation gives a cleaner output than discontinuous or pulse-skipping modes, because peak-to-peak ripple amplitude is minimized and the ripple frequency is fixed at the oscillator frequency, making the output easy to filter.

It is possible to design circuits around the MAX731 that use discontinuous-current mode as the primary means of regulation, eliminating the compensation capacitor shown in Figure 2. This is not normally recommended for several reasons. First, the peak currents in the switch and the inductor become much higher, reducing the output current. Second, the coil's inductance, peak current rating, and resistance values become critical; its physical size increases as well. Finally, the output filter requirements demand larger components.

Application Information

For fixed outputs of 12V or 15V, the MAX732 or MAX733 can be used. These devices are fully characterized at these voltages at output currents up to 200mA (125mA for MAX733), and do not require external voltage dividers. They accept input voltages above 4.0V.

Figure 2a shows the standard step-up application circuit. This circuit will operate with inputs from 2.5V to 5.25V. The output current depends on the input voltage (see Maximum Output Current vs. Supply Voltage, *Typical Operating Characteristics*).

Inductor Selection

A 22µH inductor is sufficient for most MAX731 designs and a 50µH inductor is sufficient for most MAX752 designs. The important specification is the inductor's incremental saturation current rating, which should be greater than 2.5 times the DC load current (500mA for 12V, 200mA loads). For lower-power applications, smaller inductor values may be used. Table 2 shows recommended inductor types and suppliers for various applications. The listed surface-mount inductors' efficiencies are nearly equivalent to those of the larger-sized, through-hole inductors.

Table 2. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS
Surface Mount	Sumida For MAX731: CD54-220 (22µH) For MAX752: CD54-220 (22µH) CD54-470 (47µH) for discontinuous mode Coiltronics CTX 100-series	Matsuo 267-series
Miniature Through-Hole	Sumida For MAX731: RCH654-220 For MAX752: RCH654-470	Sanyo OS-CON OS-CON-series Low ESR Organic Semiconductor
Low-Cost Through-Hole	Renco For MAX731: RL 1284-22 For MAX752: RL1284-47	Maxim MAXC001 150µF, Low ESR Electrolytic Nichicon PL-series Low ESR Electrolytics United Chemi-Con LXF-series

Sumida (708) 956-0666
Renco (516) 586-5566
Sanyo OS-CON (619) 661-6835
Coiltronics (305) 781-8900
Matsuo USA (714) 969-6291
Matsuo Japan (06) 332-0871
United Chemi-Con (708) 696-2000
Nichicon (708) 843-7500

Output Filter Capacitor Selection

The primary criterion for selecting the output filter capacitor is low equivalent series resistance (ESR). The product of the inductor current variation and the output capacitor's ESR determines the high-frequency amplitude seen on the output voltage. The capacitor's ESR should be less than 0.25Ω to keep the output ripple less than $50mV_{p-p}$ over the entire current range (using the recommended inductor). In addition, the output filter capacitor's ESR should be minimized to maintain AC stability. Refer to Table 2 for suggested capacitor suppliers.

In the standard application of Figure 2, the output capacitor value should be at least 300µF in order to maintain stability at full loads. 150µF capacitors (MAXC001) are available from Maxim in production quantities. Two of these capacitors can be connected in parallel. Lighter loads require proportionately lower capacitor values.

Other Components

Use a Schottky diode with a current rating of at least 500mA for full-load (200mA) operation. The 1N5817 is a good choice. The two compensation capacitor values at the CC input are critical because they have been selected to provide the best transient response.

Output-Ripple Filtering

An optional lowpass pi-filter (Figure 2) can be added to the output to reduce output ripple to about $5mV_{p-p}$. The cutoff frequency of the filter shown is 21kHz. Since the filter inductor is in series with the circuit output, its resistance should be minimized to avoid excessive voltage drop. Note that the feedback must be taken before the filter, not after the filter.

Printed Circuit Layout

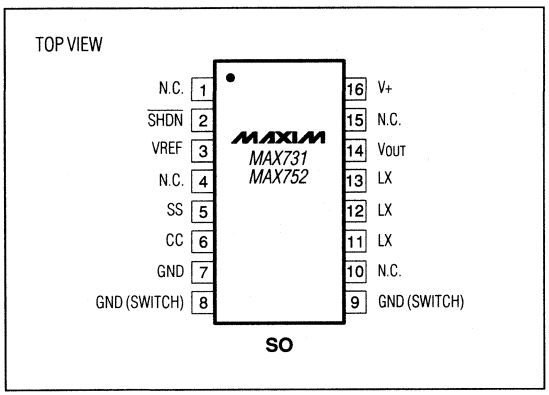
Printed circuit board layout is not critical, except to ensure quiet operation. Bypass capacitors should be located as close to the device as possible to prevent instability and noise pickup. The Schottky diode leads should also be kept short to prevent fast rise-time pulses in the output. A ground plane is recommended but not necessary.

V+ Bypassing

For MAX752 applications where greater than 13V is generated with more than 100mA load current, capacitor C2 (Fig2b) should be located less than 1/2 inch from V+ and GND pins of the IC. This capacitor snubs high voltages created by large load transients.

+5V/Adjustable Step-Up Current-Mode DC-DC Converters

Pin Configurations (continued)



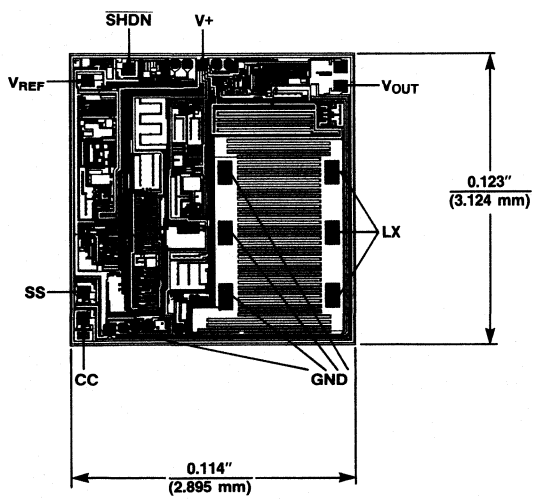
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX752CPA	0°C to +70°C	8 Plastic DIP
MAX752CWE	0°C to +70°C	16 Wide SO
MAX752C/D	0°C to +70°C	Dice*
MAX752EPA	-40°C to +85°C	8 Plastic DIP
MAX752EWE	-40°C to +85°C	16 Wide SO
MAX752MJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C only.*
***Contact factory for availability and processing to MIL-STD-883.*

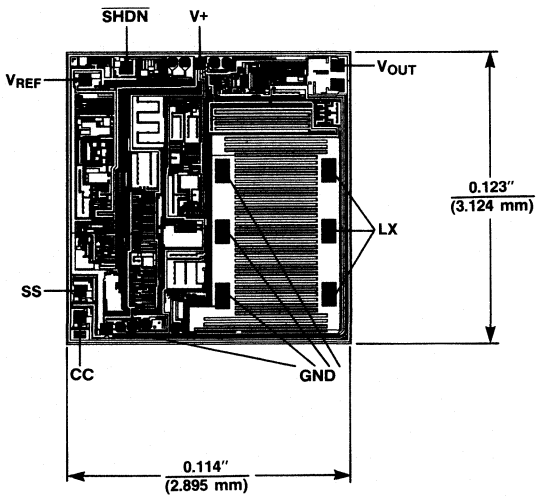
Chip Topographies

MAX731



NOTE: CONNECT SUBSTRATE TO V+
TRANSISTOR COUNT: 228

MAX752



NOTE: CONNECT SUBSTRATE TO V+
TRANSISTOR COUNT: 228

19-3966; Rev 1; 3/92

EVALUATION KIT AVAILABLE

MAXIM

+12V/+15V Step-Up Current-Mode PWM Regulators

General Description

The MAX732/MAX733 are CMOS step-up DC-DC switch-mode regulators. The MAX732 is a +12V regulator that accepts inputs from 4.0V to 9.3V and delivers up to 200mA of DC current. The MAX733 is a +15V regulator that delivers up to 125mA and accepts inputs from 4.0V to 11.0V. Typical full-load efficiencies are 85% to 92%. They require only a single inductor value of 50µH to function over their entire ranges, so no inductor-related design is necessary. Accuracy is guaranteed over temperature, line, and load variations. The MAX732/MAX733 use a current-mode pulse-width modulation (PWM) controller to provide precise output regulation and low subharmonic noise. Typical no load supply current is 1.7mA. Fixed 170kHz oscillator frequencies allow easy filtering of ripple and noise and provide for small external components.

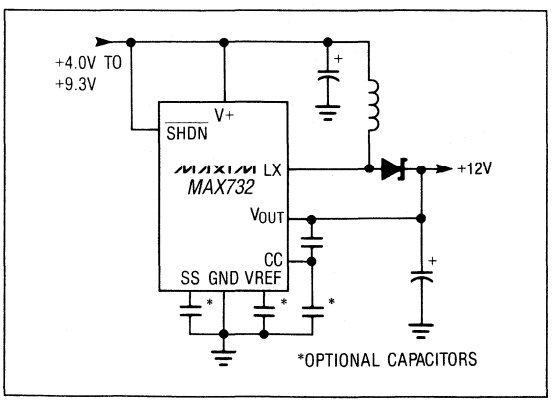
The MAX732/MAX733 feature cycle-by-cycle current limiting, overcurrent limiting, undervoltage lockout, and programmable soft-start protection.

For an adjustable version of these devices, refer to the MAX752 data sheet. For lower-power step-up applications, refer to the MAX632/MAX633 and MAX642/MAX643 data sheets. For more applications information, refer to AN-4.1, *MAX732 EV Surface-Mount Evaluation Board and Flash EEPROM Power Supply Application Notes.*

Applications

Flash Memory Programming Power Supply
Portable Instruments
Distributed Power Systems
Computer Peripherals
DC-DC Converter Module Replacement

Typical Application Circuit



Features

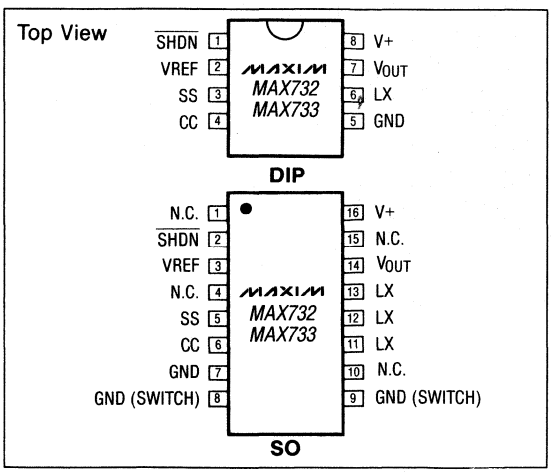
- ◆ **Load Currents Guaranteed to 200mA with No External MOSFET (125mA for MAX733)**
- ◆ **170kHz High-Frequency Current-Mode PWM**
- ◆ **Small Inductor and No Component Design Required**
- ◆ **85% to 92% Typical Efficiencies at Full Load**
- ◆ **Overcurrent and Soft-Start Protection**
- ◆ **8-Pin DIP, 16-Pin Wide SO Packages**
- ◆ **Step-Up from a 4.0V Input**
- ◆ **Shutdown Pin**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX732CPA	0°C to +70°C	8 Plastic DIP
MAX732CWE	0°C to +70°C	16 Wide SO
MAX732C/D	0°C to +70°C	Dice*
MAX732EPA	-40°C to +85°C	8 Plastic DIP
MAX732EWE	-40°C to +85°C	16 Wide SO
MAX732MJA	-55°C to +125°C	8 CERDIP
MAX733CPA	0°C to +70°C	8 Plastic DIP
MAX733CWE	0°C to +70°C	16 Wide SO
MAX733C/D	0°C to +70°C	Dice*
MAX733EPA	-40°C to +85°C	8 Plastic DIP
MAX733EWE	-40°C to +85°C	16 Wide SO
MAX733MJA	-55°C to +125°C	8 CERDIP

*Contact factory for dice specifications.

Pin Configurations



+12V/+15V Step-Up Current-Mode PWM Regulators

ABSOLUTE MAXIMUM RATINGS

Pin Voltages
- V+, LX ..... +17V, -0.3V
- V_{OUT} ..... ±25V
- SS, CC, $\overline{SHDN}$ ..... -0.3V to (V+ + 0.3V)

Peak Switch Current (I_{LX}) 1.5A
Reference Current (I_{VREF}) 2.5mA
Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 6.9mW/°C above +70°C) 550mW
- Wide SO (derate 9.5mW/°C above +70°C) 760mW
- CERDIP (derate 8.0mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX73_C_ ..... 0°C to +70°C
- MAX73_E_ ..... -40°C to +85°C
- MAX73_MJA ..... -55°C to +125°C

Junction Temperatures:
- MAX73_C_/E_ ..... +150°C
- MAX73_MJA ..... +175°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the devices at these or any conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted, typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS		MAX732 MIN	MAX732 TYP	MAX732 MAX	MAX733 MIN	MAX733 TYP	MAX733 MAX	UNITS
Output Voltage	V+ = 4.5V to 9.3V, 0 < I_{LOAD} < 150mA	MAX732C/E	11.52	12.0	12.48				V
		MAX732M	11.40	12.0	12.60				
	V+ = 6V to 9.3V, 0 < I_{LOAD} < 200mA	MAX732C/E	11.52	12.0	12.48				
		MAX732M	11.40	12.0	12.60				
	V+ = 4.5V to 11V, 0 < I_{LOAD} < 100mA	MAX733C/E/M				14.25	15.0	15.75	
	V+ = 6V to 11V, 0 < I_{LOAD} < 125mA	MAX733C/E/M				14.25	15.0	15.75	
Input Voltage Range			4.0		9.3	4.0		11	V
Line Regulation	V+ = 4V to 9.3V			0.20					%/V
	V+ = 4V to 11V						0.20		
Load Regulation	I_{LOAD} = 0mA to 100mA			0.0035			0.0035		%/mA
Efficiency	V+ = 5V, I_{LOAD} = 100mA			88			88		%
Supply Current	Includes switch current			1.7	3.0		1.7	3.0	mA
Standby Current	$\overline{SHDN}$ = 0, Entire circuit			70	100		55	100	µA
	SHDN = 0, Into V+			6			6		
Shutdown Input Threshold	V_{IH} (Note 1)		V+-0.5V			V+-0.5V			V
	V_{IL} (Note 1)				0.25			0.25	
Shutdown Input Leakage Current				1.0			1.0		µA
Short-Circuit Current				1.5			1.5		A
Undervoltage Lockout				3.7	4.0		3.7	4.0	V

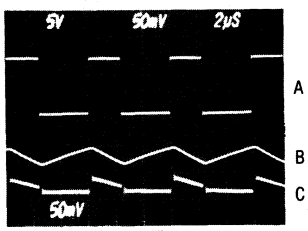
ELECTRICAL CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MAX732 MIN	MAX732 TYP	MAX732 MAX	MAX733 MIN	MAX733 TYP	MAX733 MAX	UNITS
LX On Resistance	I_{LX} = 500mA		0.5			0.5		Ω
LX Leakage Current	V_{DS} = 12V		1.0			1.0		µA
Reference Voltage		1.15	1.23	1.30	1.15	1.23	1.30	V
Reference Drift	$T_A = T_{MIN}$ to T_{MAX}		50			50		ppm/°C
Oscillator Frequency		130	170	210	130	170	210	kHz
Compensation Pin Impedance			7500			7500		Ω

Note 1: Shutdown input thresholds not tested, but guaranteed by design.

Typical Operating Characteristics

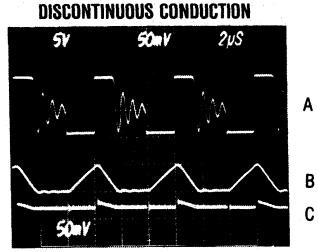
SWITCHING WAVEFORMS CONTINUOUS CONDUCTION



2µs/div

A: Switch Voltage (LX pin), 5V/div, 0V to +12.4V
B: Inductor Current, 500mA/div
C: Output Voltage Ripple, 50mV/div
MAX732, Circuit of Fig. 2, C_{OUT} = 300µF, V+ = +5V, I_{OUT} = 100mA, T_A = +25°C

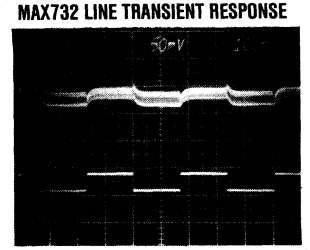
SWITCHING WAVEFORMS DISCONTINUOUS CONDUCTION



2µs/div

A: Switch Voltage (LX pin), 5V/div, 0V to +12.4V
B: Inductor Current, 200mA/div
C: Output Voltage Ripple, 50mV/div
MAX732, Circuit of Fig. 2, C_{OUT} = 300µF, V+ = +5V, I_{OUT} = 20mA, T_A = +25°C

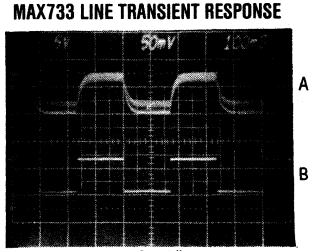
MAX732 LINE TRANSIENT RESPONSE



100ms/div

A: V_{OUT}, 50mV/div, DC-Coupled
B: V+, 5V/div, 6.0V to 9.0V
Circuit of Fig. 2, I_{OUT} = 200mA, T_A = +25°C

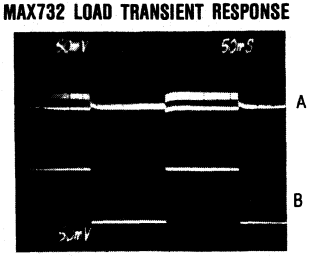
MAX733 LINE TRANSIENT RESPONSE



100ms/div

A: V_{OUT}, 50mV/div, DC-Coupled
B: V+, 5V/div, 6.0V to 12.0V
Circuit of Fig. 2, I_{OUT} = 125mA, T_A = +25°C

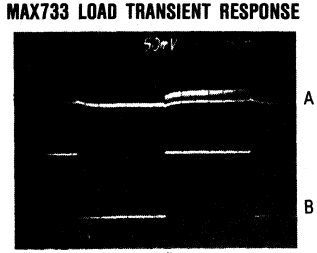
MAX732 LOAD TRANSIENT RESPONSE



50ms/div

A: V_{OUT}, 50mV/div, DC-Coupled
B: I_{OUT}, 100mA/div, 10mA to 200mA
Circuit of Fig. 2, V+ = +6V, T_A = +25°C

MAX733 LOAD TRANSIENT RESPONSE



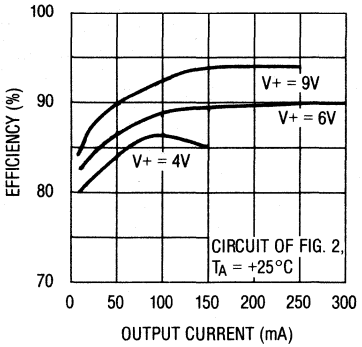
50ms/div

A: V_{OUT}, 50mV/div, DC-Coupled
B: I_{OUT}, 50mA/div, 10mA to 125mA
Circuit of Fig. 2, V+ = +6V, T_A = +25°C

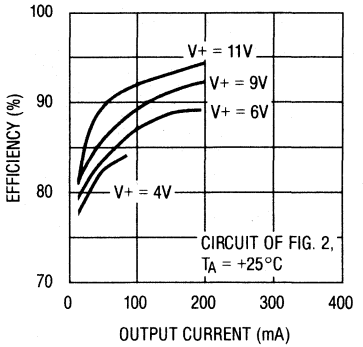
+12V/+15V Step-Up Current-Mode PWM Regulators

Typical Operating Characteristics (cont'd)

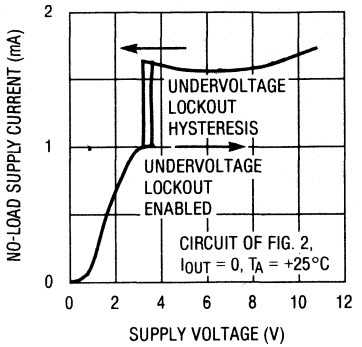
MAX732 EFFICIENCY vs. OUTPUT CURRENT



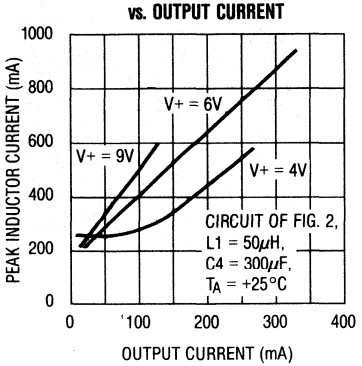
MAX733 EFFICIENCY vs. OUTPUT CURRENT



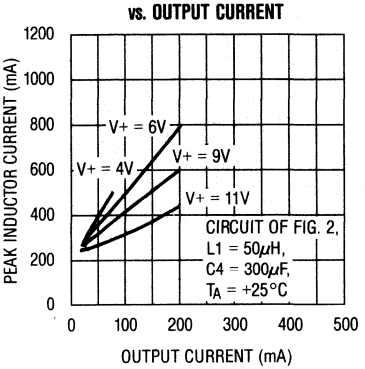
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



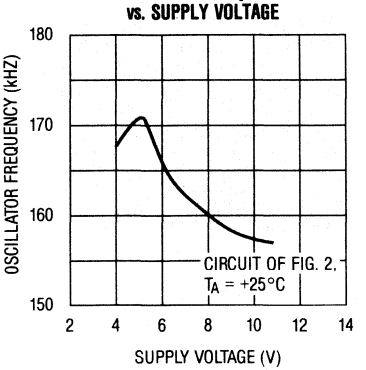
MAX732 PEAK INDUCTOR CURRENT vs. OUTPUT CURRENT



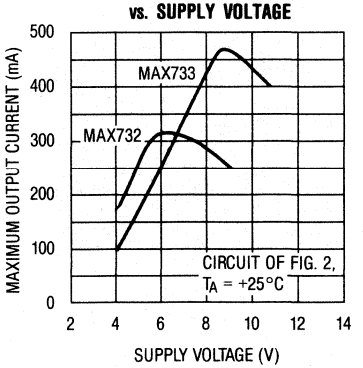
MAX733 PEAK INDUCTOR CURRENT vs. OUTPUT CURRENT



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



MAXIMUM OUTPUT CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN # 8-PIN DIP	PIN # 16-PIN WIDE SO	NAME	FUNCTION
1	2	$\overline{SHDN}$	Shutdown—active low. Ground to power-down chip, tie to V+ for normal operation. Output power FET is held off when $\overline{SHDN}$ is low.
2	3	VREF	Reference Voltage Output (+1.23V). Supplies up to 100μA for external loads.
3	5	SS	Soft-Start. Capacitor between SS and GND provides SS and short-circuit protection.
4	6	CC	Compensation Capacitor Input. Externally compensates the outer feedback loop.
5	7	GND	Ground. Ground for control circuitry.
	8, 9	GND (SW)	Switch Ground. Ground of the output power FET. Both pins must be separately tied to ground because they are not internally connected.
6	11, 12, 13	LX	Drain of internal N-channel power MOSFET.
7	14	V_{OUT}	Output-Voltage Sense Input. Provides regulation feedback sensing. Connect to +12V or +15V output.
8	16	V+	Supply Voltage Input. Bypass to GND with 0.1μF ceramic and large-value electrolytic capacitors in parallel. The 0.1μF capacitor must be as close to the device as possible.
	1, 4, 10, 15	N.C.	No Connect. No internal connections to these pins.

Table 1. Typical Soft-Start Times

MAX732 CIRCUIT CONDITIONS			SOFT-START TIME (ms) vs. C1 (μF)		
V+ (V)	I_{OUT} (mA)	C4 (μF)	0.1μF	0.47μF	1.0μF
4.5	0	300	57 ms	115 ms	123 ms
6.0	0	300	40	80	70
9.0	0	300	29	57	44
4.5	100	300	92	348	780
6.0	100	300	59	209	444
9.0	100	300	29	57	60
4.5	200	300	175	713	1690
6.0	200	300	84	340	756
9.0	200	300	28	76	123

MAX733 CIRCUIT CONDITIONS			SOFT-START TIME (ms) vs. C1 (μF)		
V+ (V)	I_{OUT} (mA)	C4 (μF)	0.1μF	0.47μF	1.0μF
4.5	0	300	90 ms	208 ms	251 ms
6.0	0	300	64	135	148
9.0	0	300	36	67	53
12.0	0	300	28	49	33
4.5	75	300	157	680	1380
6.0	75	300	103	426	882
9.0	75	300	46	162	305
12.0	75	300	28	49	33
4.5	125	300	235	1124	2260
6.0	125	300	133	596	1255
9.0	125	300	54	231	476
12.0	125	300	30	49	41

Note: Soft-start times are ± 35% accurate, C1 is the soft-start capacitor, C4 is the output capacitor.

+12V/+15V Step-Up Current-Mode PWM Regulators

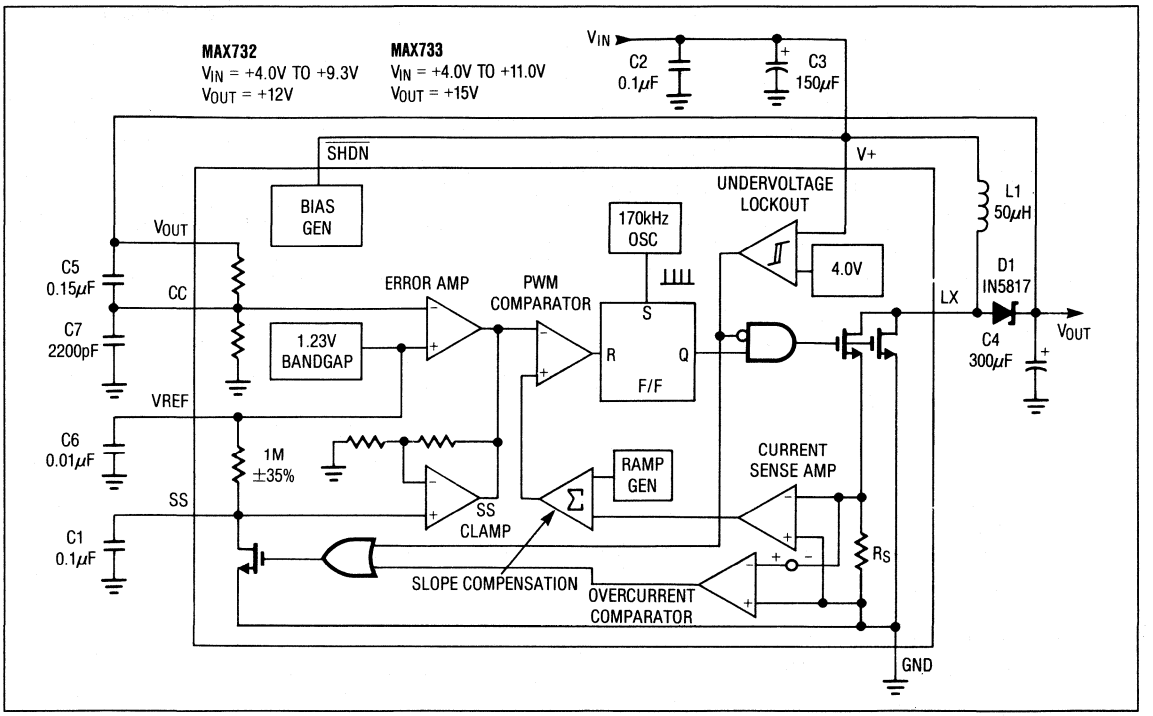


Figure 1. MAX732/MAX733 Detailed Block Diagram with External Components

Operating Principle

The MAX732 +12V switch-mode regulator uses a current-mode pulse-width modulation (PWM) control system coupled with a simple boost regulator topology to convert an unregulated DC voltage ranging from 4.0V to 9.3V to a +12V output. The MAX733 operates likewise, stepping up to +15V from a 4.0V to 11.0V supply. The current-mode PWM architecture provides cycle-by-cycle current limiting and excellent load-transient response characteristics.

Detailed Description

The controller consists of two feedback loops: an inner (current) loop that monitors the switch current via the current-sense resistor (R_S) and amplifier, and an outer (voltage) loop that monitors the output voltage via the error amplifier (Figure 1). The inner loop performs cycle-by-cycle current limiting, truncating the power transistor on-time when the switch current reaches a predetermined threshold. This threshold is determined by the outer loop. For example, a sagging output voltage produces an error signal that raises the threshold, allowing the circuit to store and transfer more energy during each cycle.

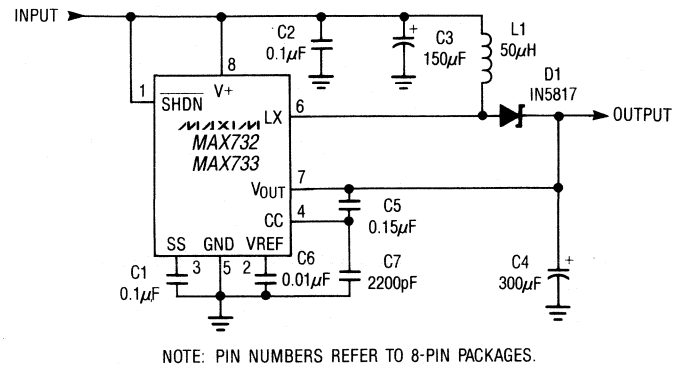
Programmable Soft Start

A capacitor connected to the Soft-Start (SS) pin ensures an orderly power-up. The voltage on the charging capacitor slowly raises the clamp on the error-amplifier output voltage, limiting surge currents at power-up by slowly increasing the cycle-by-cycle current-limit threshold. Soft-start timing is controllable from SS by capacitor choice. A typical value is 0.1µF. Table 1 lists timing characteristics for selected capacitor values and circuit conditions.

The output sags if more than the maximum load current is drawn. The overcurrent comparator trips if the load exceeds approximately 1.5A. An SS cycle is actively initiated when either an undervoltage or overcurrent fault condition triggers an internal transistor to discharge the SS capacitor to ground.

Overcurrent Limiting

When the load current exceeds approximately 1.5A, the output stage is turned off by the inner loop cycle-by-cycle current-limiting action, and the overcurrent comparator signals the control logic to initiate an SS cycle. On each clock cycle, the output FET turns on again and attempts to deliver current until cycle-by-cycle or overcurrent limits are exceeded. Note that the SS capacitor must be at least 0.01µF for overcurrent protection to function properly.



PART	INPUT SUPPLY RANGE (V)	OUTPUT VOLTAGE	GUARANTEED OUTPUT CURRENT
MAX732	4.5 to 9.3	+12V	150mA
	6.0 to 9.3	+12V	200mA
MAX733	4.5 to 11.0	+15V	100mA
	6.0 to 11.0	+15V	200mA

OPTIONAL LOWPASS OUTPUT FILTER

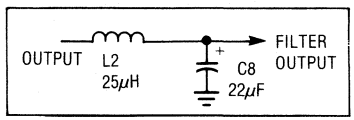


Figure 2. Standard Boost Application Circuit

Undervoltage Lockout

The MAX732/MAX733 monitor the supply voltage at V+ and operate for supply voltages greater than 3.7V (typ), 4.0V guaranteed, with 0.25V hysteresis (see MAX732 Quiescent Supply Current vs. Supply Voltage, *Typical Operating Characteristics*). When an undervoltage condition is detected, control logic turns off the output power FET and discharges the SS capacitor to ground. The control logic holds the output power FET in an off state until the supply voltage rises above the undervoltage threshold, at which time an SS cycle begins.

Shutdown

The MAX732/MAX733 are held in shutdown mode by keeping SHDN at ground. In shutdown, the output power FET is off, but there is still an external path from V+ to the load via the inductor and diode. There is also a path from V+ to GND via the inductor, diode, and internal feedback resistors at the VOUT pin. The internal reference also turns off, which causes the SS capacitor to discharge. Typical device standby current in shutdown mode is 6µA. For normal operation, connect SHDN to V+. An SS cycle is initiated when the MAX732/MAX733 come out of shutdown.

Internal Reference

The +1.23V bandgap reference supplies up to 100µA at VREF. A bypass capacitor from VREF to GND may be required.

Oscillator

The internal oscillator typically operates at 170kHz. Temperature stability over the military temperature range is about 0.06%/°C.

Application Information

Standard +12V or +15V Output Step-Up Converter Application in Continuous-Conduction Mode

Figure 2 shows the standard +12V or +15V step-up application circuit for continuous-conduction mode operation. This circuit will operate over its entire line, load, and temperature ranges using the single set of component values shown. All components shown are suitable for both the MAX732 and the MAX733.

The MAX732 delivers a guaranteed 150mA for 4.5V to 9.3V supply voltages, and a guaranteed 200mA for supplies from 6.0V to 9.3V. The MAX733 is guaranteed to deliver 100mA for inputs ranging from 4.5V to 11.0V and 125mA for inputs from 6.0V to 12.0V. Both devices regulate at supply voltages down to 4.0V (the upper limit of undervoltage lockout), but some reduction of the maximum output current will occur.

Continuous-conduction mode operation gives a cleaner output than discontinuous operation: Peak-to-peak ripple amplitude is minimized and ripple frequency is fixed at the oscillator frequency. Both conditions make the output noise easy to filter. However, continuous-conduction mode operation requires additional compensation and bypass capacitors, as shown in Figure 2.

V+ BYPASS REQUIREMENTS

MAX733 applications should place capacitor C2 (fig 2) to within ½ inch from V+ and GND pins of IC. This capacitor helps snub high voltages created by a large load transients.

+12V/+15V Step-Up Current-Mode PWM Regulators

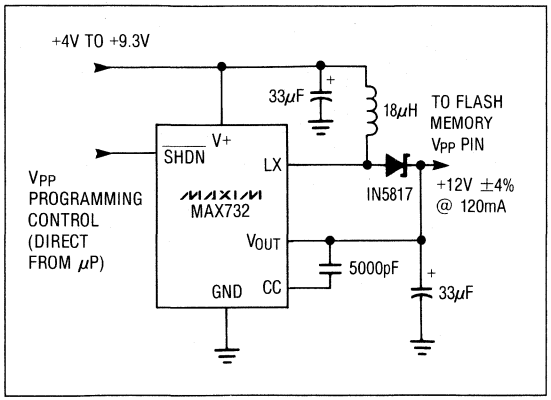


Figure 3. Flash Memory Programmer

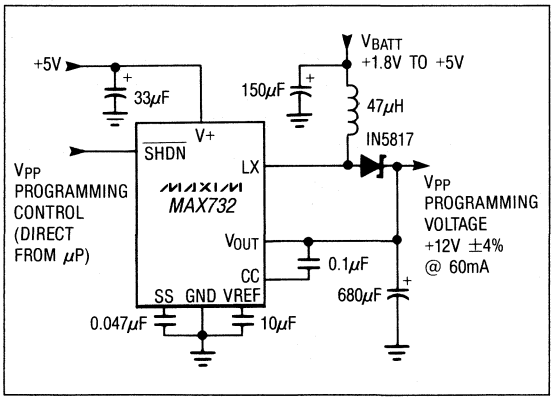


Figure 4. 2-Cell to +12V Battery-Powered Flash Memory Programmer

+12V Flash Memory Programming Power Supply

The circuit of Figure 3 is a simple +12V ±4%, 120mA flash memory programmer. The small 18µH inductor forces the circuit to operate in discontinuous-conduction mode, which allows for smaller input and output filter capacitors and the removal of several bypass and compensation capacitors relative to the standard application. It also makes the circuit less sensitive to PC layout errors. Programming is controlled by a direct microprocessor input to the SHDN pin of the MAX732. When SHDN is forced high, the output voltage, which is connected to the VPP input of the flash memory, rises to +12V and programs the flash memory. When SHDN goes low, the output voltage drops to approximately a diode drop below VIN. The voltage at the VPP pin has to be kept below 6.5V to avoid inadvertent programming.

For a +5V input, efficiency is 88%, quiescent current for this circuit is 1.7mA, circuit shutdown current is 70µA, and shutdown current into the V+ pin is 6µA. See Application Note 4.2.

2-Cell to +12V Battery-Powered Flash Memory Programming Supply

The circuit of Figure 4 allows for +12V step-up operation with battery supplies as low as 1.8V. The MAX732 supply voltage (V+) and programming control pin (SHDN) operate from the +5V logic supply, while the voltage across the inductor is supplied directly from the battery.

This application is targeted for 60mA operation. It is not possible to achieve output currents greater than 80mA with VBATT below 2.0V because of the high peak currents required.

Inductor Selection

The MAX732/MAX733 require no inductor design. They are tested in-circuit, and are guaranteed to deliver the power specified in the *Electrical Characteristics* with high efficiency using a single 50µH inductor. A 47µH inductor can also be used. The 50µH inductor's incremental saturation current rating should be greater than 500mA for 200mA load operation. For lower power applications, smaller inductor values may be used. Table 2 shows recommended inductor types and suppliers for various applications. The listed surface-mount inductors' efficiencies are nearly equivalent to those of the larger-sized, through-hole inductors.

Output Filter Capacitor Selection

The primary criterion for selecting the output filter capacitor is low equivalent series resistance (ESR). The product of the inductor current variation and the ESR of the output capacitor determines the amplitude of the high-frequency ripple seen on the output voltage. The ESR of the capacitor should be less than 0.25Ω to keep the output ripple less than $50mV_{p-p}$ over the entire current range (using a 50µH inductor). In addition, the ESR of the output filter capacitor should be minimized to maintain AC stability. Refer to Table 2 for suggested capacitor suppliers.

In the standard application of Fig. 2, the output capacitor value should be at least 300µF in order to maintain stability at full loads. 150µF capacitors (MAXC001) are available from Maxim in production quantities. Two of these capacitors can be connected in parallel. Lighter loads require proportionately lesser capacitor values.

Table 2. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS
Surface Mount	Sumida (708) 956-0666 CD54-470 (47µH) CD54-180 (18µH) for discontinuous mode Coiltronics (305) 781-8900 CTX 100-series	Matsuo (714) 969-2491 267-series
Miniature Through-Hole	Sumida (708) 956-0666 RCH654-470	Sanyo (619) 661-6322 OS-CON-series Low ESR Organic Semiconductor
Low-Cost Through-Hole	Renco (516) 586-5566 RL 1284-47	Maxim MAXC001 150µF, Low ESR Electroyltic Nichicon (708) 843-7500 PL-series Low ESR Electrolytics United Chemicon (708) 696-2000 LXF-series

Other Components

The catch diode should be a Schottky or high-speed silicon rectifier with a current rating of at least 500mA for full-load (200mA) operation. The 1N5817 is a good choice. The two compensation capacitor (CC) values at the CC input are critical because they have been selected to provide the best transient responses.

Output Ripple Filtering

An optional lowpass pi-filter (Figure 2) can be added to the output to reduce output ripple to about $5mV_{p-p}$. The cutoff frequency of the filter shown is 21kHz. Since the filter inductor is in series with the circuit output, its resistance should be minimized to avoid excessive voltage drop.

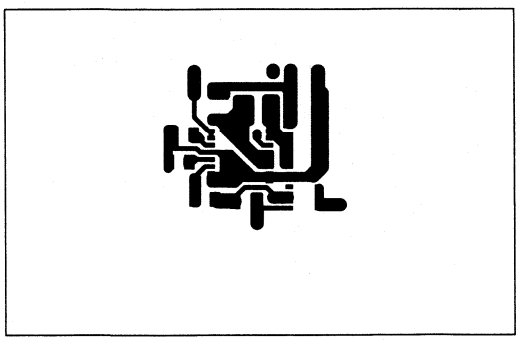


Figure 5. Surface-Mount PC Layout for Standard Step-Up Application (1x Scale, Top-Side Trace View)

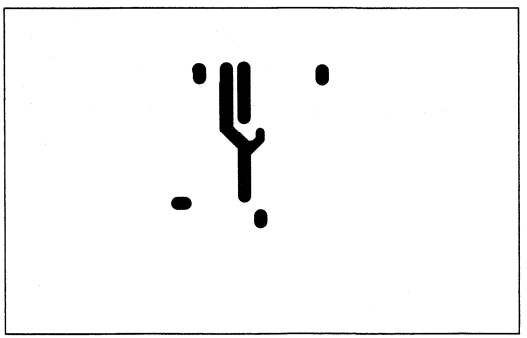


Figure 6. Surface-Mount PC Layout for Standard Step-Up Application (1x Scale, Bottom-Side Trace View)

+12V/+15V Step-Up Current-Mode PWM Regulators

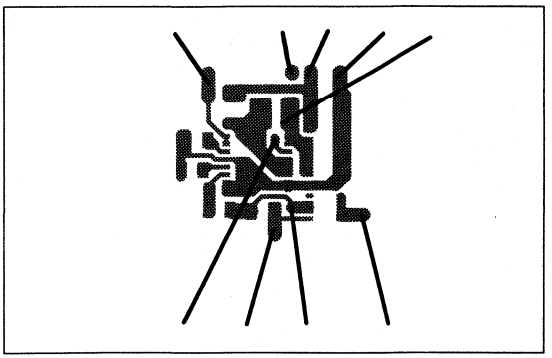


Figure 7. Surface-Mount Drilling Guide for Standard Step-Up Application. All Holes are 0.031" in diameter. (1x Scale, Top-Side Trace View)

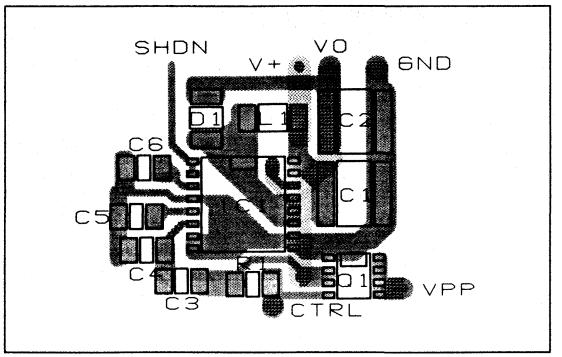


Figure 8. Surface-Mount Component Placement Diagram for Standard Step-Up Application. Component Labels Refer to Figure 9

Printed Circuit Layouts

A good layout is essential to clean, stable operation. The surface-mount layout and component placement diagrams in Figures 5-8 have been successfully tested over a wide range of operating conditions. The surface-mount layout shown is configured for the Sumida and Matsuo surface-mount components listed in Table 2. Note that the input bypass capacitors must be positioned as close to the V_{OUT} and GND pins as possible. The traces connecting the ground to the input and output filter capacitors and the MAX732/MAX733 GND pin must be short to reduce stray inductance.

MAX732 Evaluation Board

An assembled surface-mount printed circuit board is available for the MAX732. Intended for prototyping and performance evaluation, this board is a +12V switched power supply capable of delivering 120mA. The evaluation board circuit is configured as the flash memory programmer shown in Figure 9, and contains all components, including a miniature surface-mount inductor and tantalum filter capacitors on a printed circuit layout similar to Figures 5-8. Also included on the board is a P-channel MOSFET switch for applications that require total turn-off of the MAX732 output. The evaluation board can be ordered as part number "MAX732EVKIT." For more information about the MAX732 evaluation board refer to AN-4.1, "MAX732 EV Surface-Mount Evaluation Board and Flash EEPROM Power Supply Application Notes."

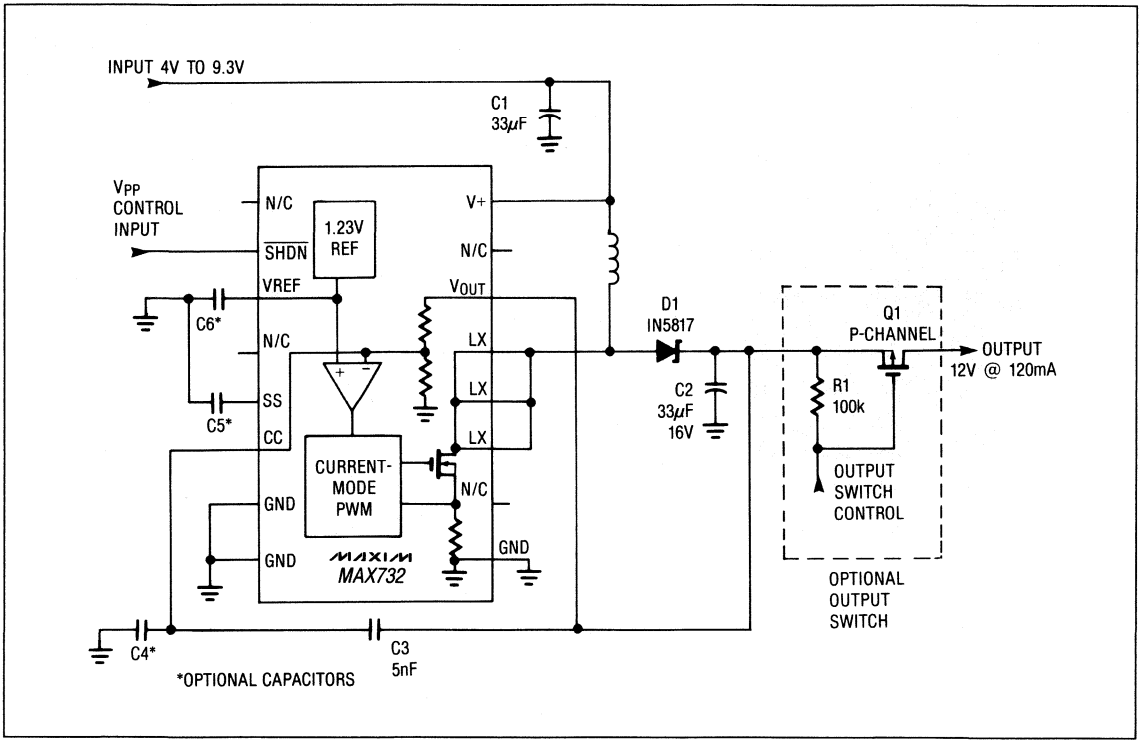


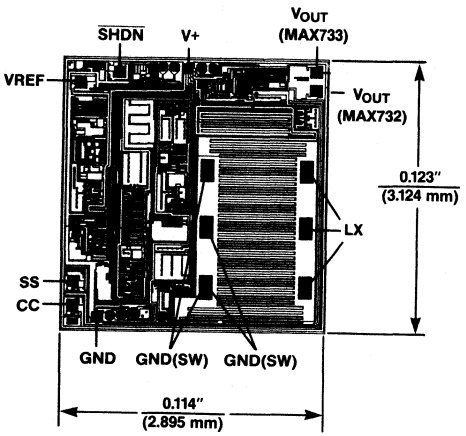
Figure 9. Circuit Schematic for Surface-Mount Evaluation Board

4

+12V/+15V Step-Up Current-Mode PWM Regulators

Chip Topography

MAX732/MAX733



NOTE: CONNECT SUBSTRATE TO V+
TRANSISTOR COUNT: 226

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

+12V, 120mA Flash Memory Programming Supply

General Description

The MAX734 is a +12V-output, step-up, DC-DC switch-mode regulator. It delivers a guaranteed 120mA from a 4.75V input, and is ideal for programming flash memories. It comes in 8-pin SO and DIP packages, and uses only a diode, an 18µH inductor, and two 33µF capacitors. The entire circuit is completely surface-mountable and fits into less than $0.3in^2$. The MAX734 also features a logic-controlled shutdown pin that allows direct microprocessor control. In-circuit testing ensures guaranteed output specifications over load, line, and temperature limits.

Battery-saving features include 88% efficiency, 1.1mA operating quiescent supply current, and 70µA shutdown supply current. The operating supply current can be reduced to less than 500µA by toggling the shutdown pin with the microprocessor. The minimum input start-up voltage is 1.9V.

The MAX734 uses current-mode pulse-width modulation (PWM) control to provide precise output regulation and low subharmonic noise. A fixed 170kHz oscillator frequency facilitates ripple filtering and allows the use of tiny external capacitors.

For higher-current solutions up to 250mA, refer to the MAX732 data sheet and evaluation kit (MAX732EVKIT-SO).

Applications

+12V Flash Memory Programming Supplies

PCMCIA +12V Supplies

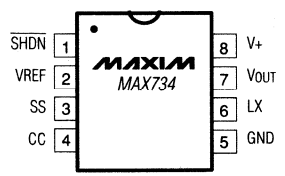
Solid-State Disk Drives

Palmtop Computers

Compact +12V Op-Amp Supplies

Pin Configuration

TOP VIEW



DIP/SO

Features

- ♦ **Regulated +12V ±5% Output**
- ♦ **Guaranteed 120mA Output Current**
- ♦ **Tiny Flash Memory Programming Circuit:**
  Fits into $0.3in^2$
  8-Pin SO and Plastic DIP Packages
  Uses Tiny 18µH Inductor and 33µF Capacitors
- ♦ **Logic-Controlled 70µA Shutdown**
- ♦ **88% Typical Efficiency**
- ♦ **1.9V Minimum Input Start-Up Voltage**

Ordering Information

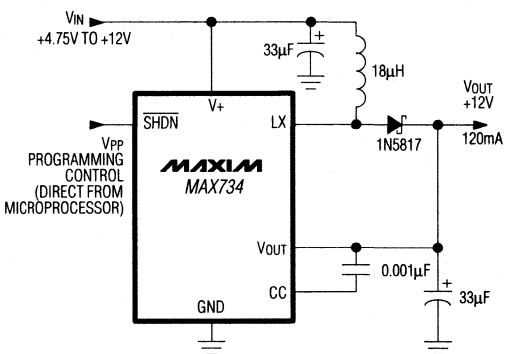
PART	TEMP. RANGE	PIN-PACKAGE
MAX734CPA	0°C to +70°C	8 Plastic DIP
MAX734CSA	0°C to +70°C	8 SO
MAX734C/D	0°C to +70°C	Dice*
MAX734EPA	-40°C to +85°C	8 Plastic DIP
MAX734ESA	-40°C to +85°C	8 SO
MAX734MJA	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

4

Typical Operating Circuit

+12V FLASH MEMORY PROGRAMMING SUPPLY



+12V, 120mA Flash Memory Programming Supply

ABSOLUTE MAXIMUM RATINGS

Pin Voltages
- V+, LX ..... +17V, -0.3V
- V_{OUT} ..... ±25V
- SS, CC, $\overline{SHDN}$ ..... -0.3V to (V+ + 0.3V)

Peak Switch Current (I_{LX}) 1.5A
Reference Current (I_{VREF}) 2.5mA
Continuous Power Dissipation (T_A = +70°C)
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX734C_ _ ..... 0°C to +70°C
- MAX734E_ _ ..... -40°C to +85°C
- MAX734MJA ..... -55°C to +125°C

Junction Temperatures:
- MAX734C_ _/E_ _ ..... +150°C
- MAX734MJA ..... +175°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V+ = 4.75V to 12V, Figure 1, 0mA < I_{LOAD} < 120mA	MAX734C/E	11.64	12.12	12.60	V
	V+ = 2V to V_{OUT}, Figure 2	MAX734M	11.40	12.12	12.60	
Load Current	V+ = 4.75V, Figure 1		120	150		mA
	V+ = 4.75V, Figure 2			175		
	V+ = 3.5V, Figure 2			110		
	V+ = 2.7V, Figure 2			75		
	V+ = 2.0V, Figure 2			40		
Minimum Input Start-Up Voltage	Figure 1			3.5		V
	Figure 2			1.9		
Maximum Input Voltage					V_{OUT}	V
Line Regulation	V+ = 5V to 12V			0.20		%/V
Load Regulation	I_{LOAD} = 0mA to 100mA			0.0035		%/mA
Efficiency	V+ = 5V, I_{LOAD} = 100mA			88		%
Supply Current	Includes switch current (Note 1)			1.1	2.5	mA
Standby Current	$\overline{SHDN}$ = 0, entire circuit			70	100	µA
	SHDN = 0, into V+			6		
Shutdown Input Threshold	V_{IH} (Note 1)		2.0			V
	V_{IL} (Note 1)				0.25	
Shutdown Input Leakage Current					1.0	µA
LX On Resistance	I_{LX} = 500mA			0.5		Ω
LX Leakage Current	V_{DS} = 12V			1.0		µA
Reference Voltage				1.23		V
Reference Drift	T_A = T_{MIN} to T_{MAX}			50		ppm°C
Oscillator Frequency				170		kHz
Compensation Pin Impedance				7500		Ω

Note 1: Quiescent supply current can be reduced to less than 500µA by pulsing $\overline{SHDN}$ while supplying 12V to a small load. See *General Description*.

+12V, 120mA Flash Memory Programming Supply

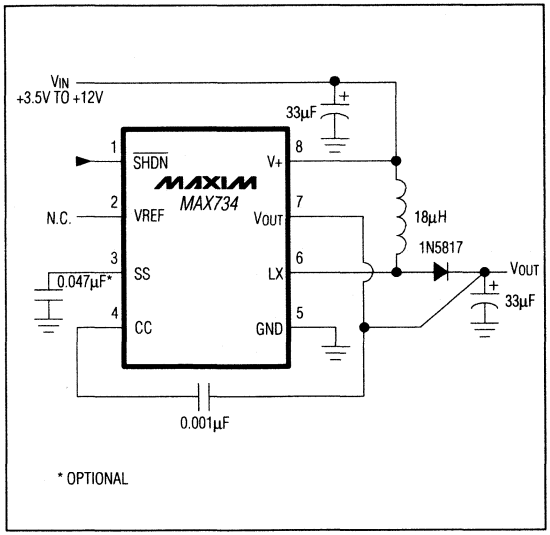


Figure 1. Standard Operation

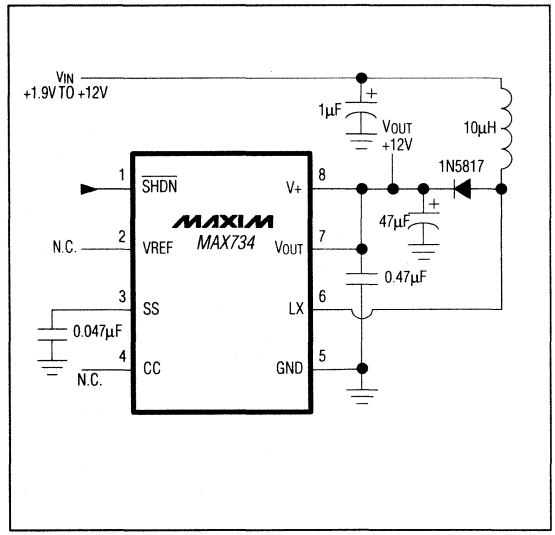


Figure 2. Bootstrap Operation

4

19-0017; Rev 1; 5/92

EVALUATION KIT AVAILABLE

MAXIM

-5V-Output Inverting Current-Mode PWM Regulator

General Description

The MAX735 is a CMOS inverting switch-mode regulator with an internal power MOSFET. It operates from a 4.0V to 6.2V input. 200mA output current is guaranteed for inputs greater than 4.5V. Quiescent supply current is typically 1.6mA, and a shutdown mode reduces this to 10µA. These power-conserving features, along with high efficiency and an application circuit that lends itself to miniaturization, make the MAX735 excel in a broad range of on-card and portable equipment applications.

The MAX735 employs a high-performance current-mode pulse-width modulation (PWM) control scheme to provide tight output-voltage regulation and low subharmonic noise. The fixed-frequency oscillator is factory-trimmed to 160kHz, allowing for easy noise filtering. The regulator is production tested in an actual application circuit, and output accuracy is guaranteed to within ±5% over all specified conditions of line, load, and temperature.

For a similar device with a wider input voltage range, refer to the MAX739 data sheet. For fixed -12V and -15V versions, refer to the MAX736/MAX737 data sheets. For a regulator with an adjustable 0V to -15V output, see the MAX759 data sheet. For lower-power applications, refer to the MAX635/636/637 data sheet.

Applications

Board-Level DC-DC Conversion

Battery-Powered Equipment

Computer Peripherals

Features

- ♦ **Converts +4.0V to +6.2V Input to -5V Output**
- ♦ **200mA Guaranteed Output Current (V_{IN} ≥ 4.5V)**
- ♦ **78% Typical Efficiency**
- ♦ **1.6mA Quiescent Current**
- ♦ **10µA Shutdown Mode**
- ♦ **160kHz Fixed-Frequency Oscillator**
- ♦ **Current-Mode PWM - Low Noise and Jitter**
- ♦ **Undervoltage Lockout and Soft-Start**
- ♦ **Simple Application Circuit**

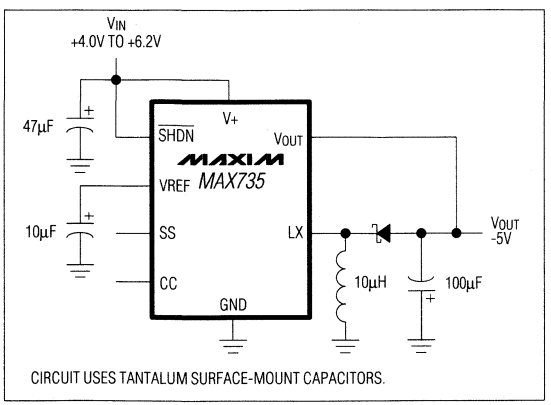
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX735CPA	0°C to +70°C	8 Plastic DIP
MAX735CSA	0°C to +70°C	8 SO
MAX735C/D	0°C to +70°C	Dice*
MAX735EPA	-40°C to +85°C	8 Plastic DIP
MAX735ESA	-40°C to +85°C	8 SO
MAX735MJA	-55°C to +125°C	8 CERDIP**

* *Contact factory for dice specifications.*

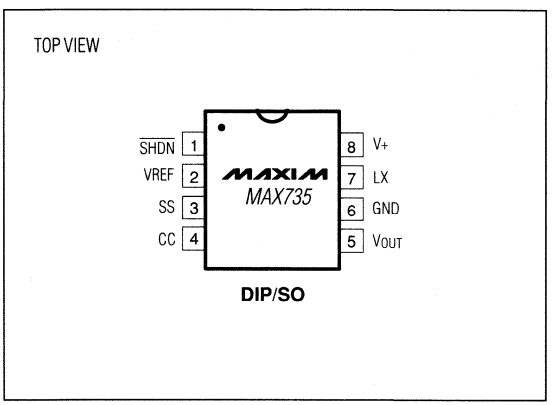
** *Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



CIRCUIT USES TANTALUM SURFACE-MOUNT CAPACITORS.

Pin Configuration



DIP/SO

-5V-Output Inverting Current-Mode PWM Regulator

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND) ..... +7V, -0.3V
Switch Voltage (LX to V+) ..... +12.5V, -0.3V
Feedback Voltage (V_{OUT} to GND) ..... ±25V
Auxiliary Input Voltages
(SS, CC, $\overline{SHDN}$ to GND) ..... -0.3V to (V+ + 0.3V)
Peak Switch Current (I_{LX}) 2.0A
Reference Current (I_{VREF}) 2.5mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX735C_ _ ..... 0°C to +70°C
MAX735E_ _ ..... -40°C to +85°C
MAX735MJA ..... -55°C to +125°C
Junction Temperatures:
MAX735C/E_ _ ..... +150°C
MAX735MJA ..... +175°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

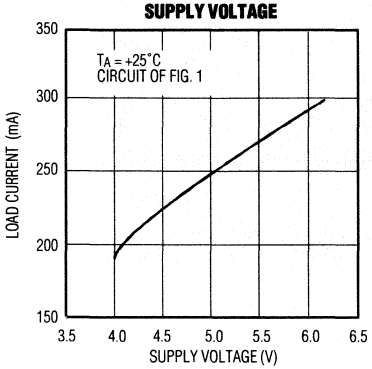
(Circuit of Figure 2, V+ = 5V, I_{LOAD} = 0mA, T_A = T_{MIN} to T_{MAX}, typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			4.0		6.2	V
Output Voltage	V+ = 4.5V to 6.2V	0mA < I_{LOAD} < 200mA, T_A = -40°C to +85°C	-5.25	-5.0	-4.75	V
		0mA < I_{LOAD} < 175mA, T_A = -55°C to +125°C	-5.25	-5.0	-4.75	
Output Current	V+ = 4.5V to 6.2V	T_A = -40°C to +85°C	200	275		mA
		T_A = -55°C to +125°C	175			
Line Regulation	V+ = 4.0V to 6.2V			0.1		%/V
Load Regulation	I_{LOAD} = 0mA to 200mA			0.001		%/mA
Efficiency	I_{LOAD} = 100mA			78		%
Supply Current	Includes switch current			1.6	3.0	mA
Standby Current	$V_{\overline{SHDN}}$ = 0V			10	100	µA
Short-Circuit Current				1.5		A
Undervoltage Lock-Out				3.7	4.0	V
LX On Resistance				0.5		Ω
LX Leakage Current	V_{DS} = +10V			1		µA
Reference Voltage	T_A = +25°C (I_{VREF} = 0µA)		1.15	1.23	1.30	V
Reference Drift	T_A = T_{MIN} to T_{MAX}			50		ppm/°C
Oscillator Frequency			130	160	210	kHz
Compensation Pin Impedance				7500		Ω
$\overline{SHDN}$ Input Current					1	µA
$\overline{SHDN}$ Logic High					V+ - 0.5	V
$\overline{SHDN}$ Logic Low			0.25			V

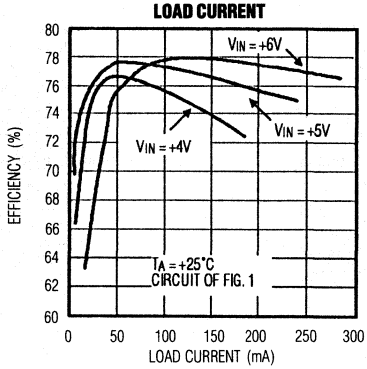
-5V-Output Inverting Current-Mode PWM Regulator

Typical Operating Characteristics

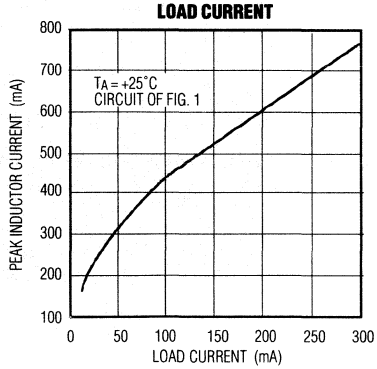
LOAD CURRENT vs. SUPPLY VOLTAGE



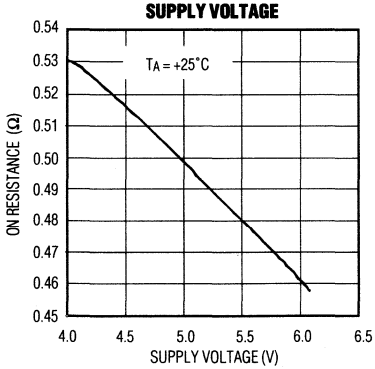
EFFICIENCY vs. LOAD CURRENT



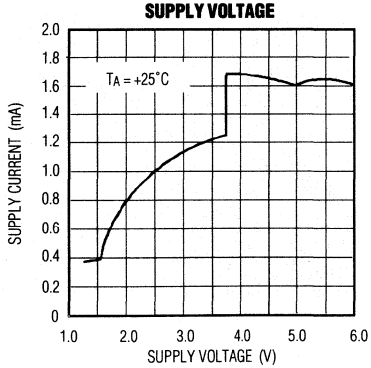
PEAK INDUCTOR CURRENT vs. LOAD CURRENT



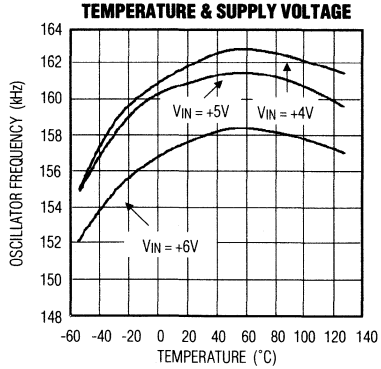
SWITCH ON RESISTANCE vs. SUPPLY VOLTAGE



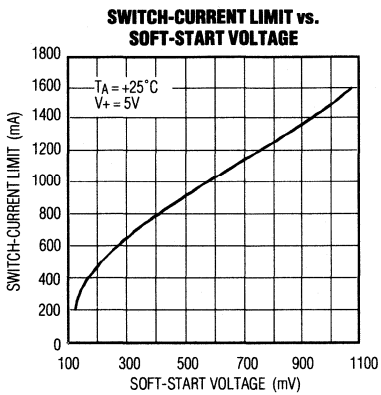
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



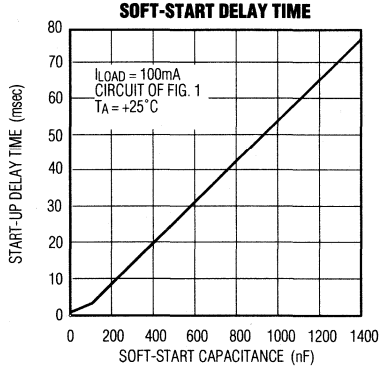
OSCILLATOR FREQUENCY vs. TEMPERATURE & SUPPLY VOLTAGE



SWITCH-CURRENT LIMIT vs. SOFT-START VOLTAGE



SOFT-START DELAY TIME



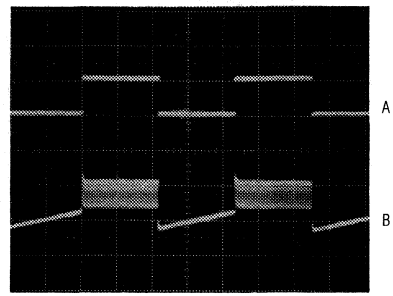
-5V-Output Inverting Current-Mode PWM Regulator

Typical Operating Characteristics (continued)

SWITCHING WAVEFORMS

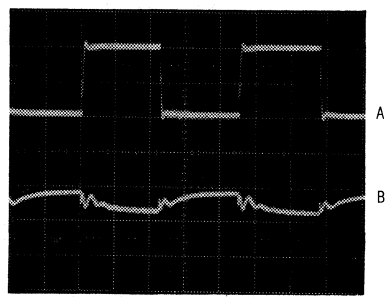
A = SWITCH VOLTAGE (LX), 5V/div
B = INDUCTOR CURRENT, 500mA/div
C = OUTPUT VOLTAGE RIPPLE, 50mV/div
TIMEBASE = 2µs/div
CIRCUIT OF FIG. 1
V_{IN} = 5V
T_A = +25°C

LOAD-TRANSIENT RESPONSE



A = LOAD CURRENT, 0mA TO 200mA
B = OUTPUT VOLTAGE, 50mV/div
TIMEBASE = 10ms/div
CIRCUIT OF FIG. 1
V_{IN} = 5V
T_A = +25°C

LINE-TRANSIENT RESPONSE



A = INPUT VOLTAGE, 4V TO 6V
B = OUTPUT VOLTAGE, 50mV/div
TIMEBASE = 500µs/div
I_{LOAD} = 100mA
T_A = +25°C

Pin Description

PIN	NAME	FUNCTION
1	$\overline{SHDN}$	$\overline{SHUTDOWN}$ Control. V+ = normal operation, GND = shutdown.
2	VREF	Reference Voltage Output = 1.23V. Supplies up to 125µA for external loads.
3	SS	Soft-Start
4	CC	Compensation Input of the error amplifier. Held at virtual ground.
5	V_{OUT}	Output Voltage feedback terminal (actually an input). Connected to internal resistors.
6	GND	Ground
7	LX	Switch Output - internal P-channel MOSFET drain
8	V+	Positive Supply-Voltage Input. Bypass with a 1µF ceramic capacitor close to V+ and GND pins. Use additional bypass capacitor as shown in Figures 1, 2, and 3.

-5V-Output Inverting Current-Mode PWM Regulator

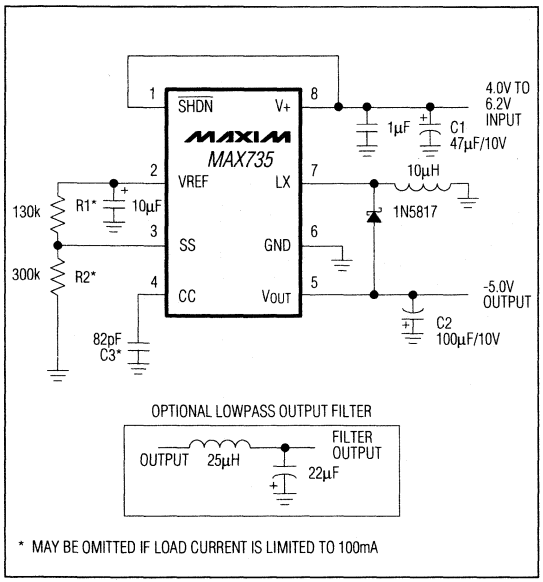


Figure 1. Application Circuit Using Surface-Mount Components (Commercial and Extended Industrial Temperature Ranges)

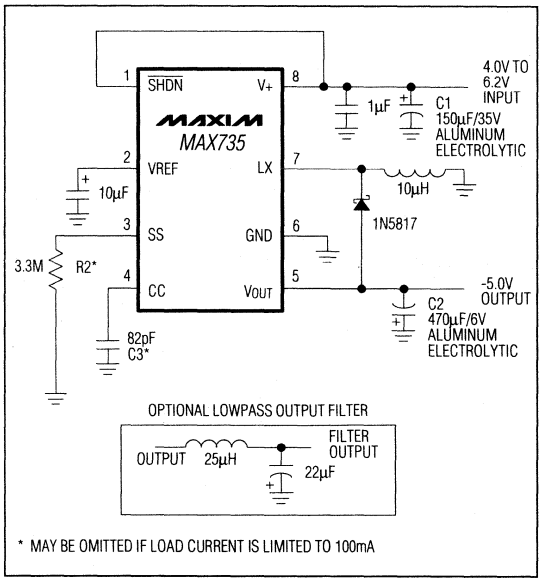


Figure 2. Application Circuit Using Through-Hole Components (Commercial Temperature Range)

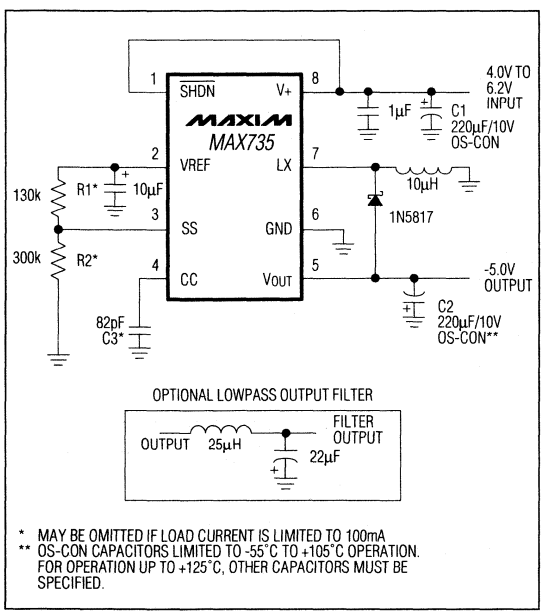


Figure 3. Application Circuit Using Through-Hole Components (All Temperature Ranges)

Detailed Description

4

Operating Principle

The MAX735 is a monolithic CMOS IC containing a current-mode PWM controller and a 2A P-channel power MOSFET. Current-mode control provides excellent line-transient response, inherent overcurrent protection, and excellent AC stability. The switch transistor is a current-sensing MOSFET that splits off a fraction of the total source current for current-limit detection.

Basic Application Circuits

The three basic application circuits shown are simple designs using standard, off-the-shelf components. Figure 1's circuit uses tantalum surface-mount capacitors and a surface-mount inductor, minimizing board space and allowing for wide-temperature operation. The low equivalent series resistance (ESR) of the tantalum capacitors (typically 70mΩ at +25°C and 140mΩ at -55°C) makes for a quiet output (see Switching Waveforms in the *Typical Operating Characteristics*).

-5V-Output Inverting Current-Mode PWM Regulator

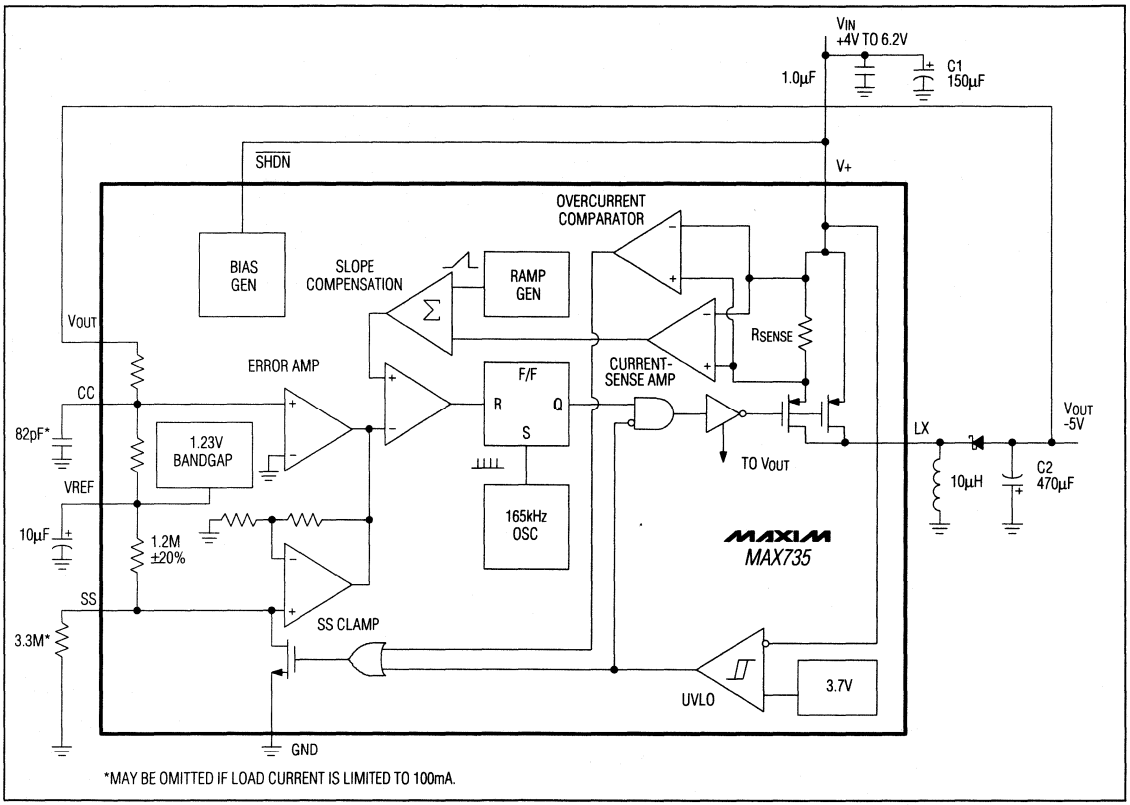


Figure 4. Detailed Block Diagram

Figure 2's circuit provides a through-hole solution for commercial-temperature operation. The capacitors are radial-lead aluminum electrolytics with an ESR of approximately 100mΩ at +25°C. These and other standard aluminum electrolytic capacitors have an ESR 100 times greater at -55°C than at +25°C, so they are not recommended for operation below 0°C. Since output voltage ripple is proportional to the ESR of the output filter capacitor, the ripple with standard aluminum electrolytic capacitors is 1.4 times that associated with tantalum capacitors.

Refer to Figure 3 for a wide-temperature, through-hole solution. The capacitors are organic semiconductor (Os-Con) aluminum electrolytics, which exhibit low ESR over a wide temperature range (typically 30mΩ at +25°C and -55°C).

Table 1 lists component suppliers for the circuits discussed above.

If the load current is limited to 100mA, R1, R2, and C3 (Figures 1-3) may be omitted. The 1.0µF V+ bypass capacitor must be placed as close as possible to pins 6 and 8.

Output-Ripple Filtering

An optional lowpass pi-filter (Figures 1-3) can be added to the output to reduce output ripple to about $5mV_{p-p}$. The cutoff frequency of the filter shown is 21kHz. Since the filter inductor is in series with the circuit output, its resistance should be minimized to avoid excessive voltage drop. Note that the feedback must be taken before the filter, not after the filter.

Soft-Start Buffer

The voltage applied to the Soft-Start (SS) input determines the peak switch-current limit (see Soft-Start Delay Time graph in *Typical Operating Characteristics*). A capacitor attached to SS ensures an orderly power-up sequence by gradually increasing the current limit. SS is pulled up to VREF internally through a 1.2MΩ resistor. The maximum current limit can be fixed externally at a lower than normal value by clamping the SS voltage to a voltage less than VREF. An SS cycle is initiated whenever either an undervoltage lockout or overcurrent fault condition triggers an internal transistor to discharge the SS capacitor to ground. Note that the SS capacitor should be at least 10nF for the overcurrent limit to function properly.

Undervoltage Lockout

The MAX735 operates for supply voltages greater than 3.7V typ (4V guaranteed), with 0.25V of hysteresis. Internal control logic holds the output power MOSFET off until the supply rises above the undervoltage threshold, at which time a soft-start cycle begins.

Inductor Selection

The MAX735 operates with a standard 10µH inductor for the entire range of supply voltages and load currents. The inductor must have a saturation (incremental) current rating greater than the peak switch current obtained from the Peak Switch Current vs. Load Current graph under *Typical Operating Characteristics*.

Printed Circuit Layout and Grounding

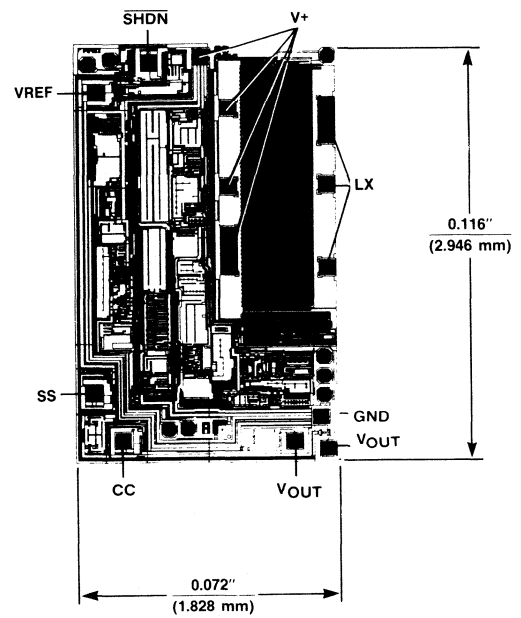
Good layout and grounding practices will ensure low-noise, jitter-free operation. Minimize wire lengths in the high-current paths, especially the distance between the inductor and the return leads of the filter and bypass capacitors (C1 and C2). These high-current ground connections should be brought to a single common point (a "star" ground). Place a low-ESR bypass capacitor directly at V+ and GND.

Table 2. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS
Surface Mount	Sumida CD54-100 (10µH)	Matsuo 267 series
Miniature Through Hole	Sumida RCH855-100M (10µH)	Sanyo Os-Con series low-ESR organic semiconductor
Low-Cost Through Hole	Renco RL 1284 (10µH)	Nichicon PL series low-ESR electrolytics United Chemicon LXF series

Matsuo USA (714) 969-2491 FAX (714) 960-6492
Matsuo Japan (06) 332-0871
Nichicon (708) 843-7500 FAX (708) 843-2798
Renco (516) 586-5566 FAX (516) 586-5562
Sanyo Os-Con USA (619) 661-6322
Sanyo Os-Con Japan (0720) 70-1005 FAX (0720) 70-1174
Sumida USA (708) 956-0666
Sumida Japan (03) 3607-5111 FAX (03) 3607-5428
United Chemi-Con (708) 696-2000 FAX (708) 640-6311

Chip Topography



Note: TRANSISTOR COUNT: 274;
CONNECT SUBSTRATE TO V+.

19-4749; Rev 1; 4/92

EVALUATION KIT AVAILABLE

MAXIM

-5V, -12V, -15V, and Adjustable Inverting Current-Mode PWM Regulators

General Description

The MAX736/737/739/759 are CMOS, inverting, switch-mode regulators with an internal power MOSFET. Guaranteed output power is 1.25W when powered from a +4.5V input, and 2.5W when powered from +12V. Quiescent supply current for the MAX739 is typically 1.7mA, and a shutdown mode reduces this to 1µA. These power-conserving features, along with high efficiency and an application circuit that lends itself to miniaturization, make these parts excel in a broad range of on-card and portable equipment applications.

The MAX736/737/739 have fixed outputs of -12V, -15V, and -5V respectively. The MAX759 is adjustable from 0V to -15V. Output voltages beyond -15V require a transformer.

These inverting DC-DC converters employ a high-performance, current-mode, pulse-width modulation (PWM) control scheme to provide tight output voltage regulation and low noise. The fixed-frequency oscillator is factory-trimmed to 165kHz, allowing easy noise filtering. The devices are production tested in an actual application circuit, and output accuracy is guaranteed at ±5% over all specified conditions of line, load, and temperature.

The input voltage range is +4V to +15V. For similar devices with smaller packages and an input voltage range of +4V to +11V, refer to the MAX735/MAX755 data sheet.

Applications

Low-Noise Analog Signal Processing Circuits
LCD Bias Supplies
Power Supplies for ECL
Board-Level DC-DC Conversion
Battery-Powered Equipment
Computer Peripherals

Features

- ♦ **Pre-Set -5V, -12V, -15V or Adjustable Outputs**
- ♦ **Convert Positive Voltages to Negative**
- ♦ **1.25W Guaranteed Output Power**
- ♦ **83% Typical Efficiency**
- ♦ **1.7mA Quiescent Current (MAX739)**
- ♦ **1µA Shutdown Mode (MAX739)**
- ♦ **+4V to +15V Input Voltage Range**
- ♦ **165kHz Current-Mode PWM – Low Noise and Jitter**
- ♦ **Undervoltage Lockout and Soft-Start Protection**

Ordering Information

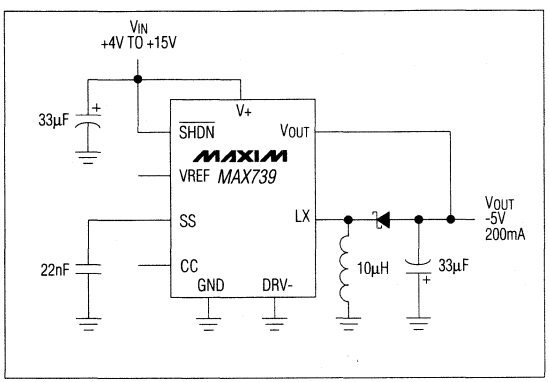
PART	TEMP. RANGE	PIN-PACKAGE
MAX736CPD	0°C to +70°C	14 Plastic DIP
MAX736CWE	0°C to +70°C	16 Wide SO
MAX736C/D	0°C to +70°C	Dice*
MAX736EPD	-40°C to +85°C	14 Plastic DIP
MAX736EWE	-40°C to +85°C	16 Wide SO
MAX736MJD	-55°C to +125°C	14 CERDIP**
MAX737CPD	0°C to +70°C	14 Plastic DIP
MAX737CWE	0°C to +70°C	16 Wide SO
MAX737C/D	0°C to +70°C	Dice*
MAX737EPD	-40°C to +85°C	14 Plastic DIP
MAX737EWE	-40°C to +85°C	16 Wide SO
MAX737MJD	-55°C to +125°C	14 CERDIP**

Ordering Information continued on last page.

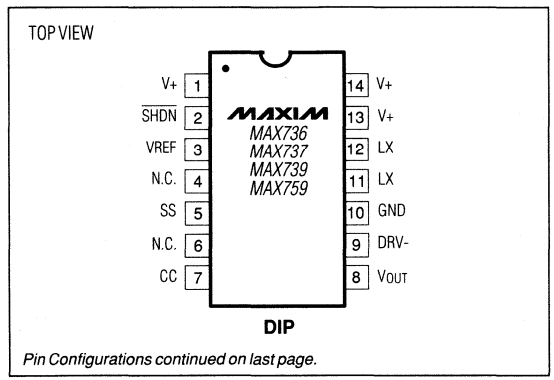
** Contact factory for dice specifications.*

***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configurations



Pin Configurations continued on last page.

-5V, -12V, -15V, and Adjustable Inverting Current-Mode PWM Regulators

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND) (Note 1)
- MAX739/759 ..... 15.5V, -0.3V
- MAX736 ..... 9.5V, -0.3V
- MAX737 ..... 6.5V, -0.3V

Max Input/Output Differential
- **MAX736/737 ..... 22V**
- **MAX739/759 (Non-Bootstrapped) 22V**
- **MAX739/759 (Bootstrapped) 17V**

Negative Drive Voltage (DRV- to V+) ..... -17V, +0.3V
Switch Voltage (LX to V+) ..... -22.5V, +0.3V
Feedback Voltage (V_{OUT} to GND) ..... ±50V
Auxiliary Input Voltages
(SS, CC, $\overline{SHDN}$ to GND) ..... -0.3V to (V+ + 0.3V)
Peak Switch Current (I_{LX}) 2.5A
Reference Current (I_{VREF}) 2.5mA

Continuous Power Dissipation (T_A = +70°C)
- 14-Pin Plastic DIP (derate 10.00mW/°C above +70°C) .. 800mW
- 16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
- 14-Pin CERDIP (derate 9.09mW/°C above +70°C) ... 727mW

Operating Temperature Ranges:
- MAX73_ /759C_ _ ..... 0°C to +70°C
- MAX73_ /759E_ _ ..... -40°C to +85°C
- MAX73_ /759MJD ..... -55°C to +125°C

Junction Temperatures:
- MAX73_ /759E/C_ _ ..... +150°C
- MAX73_ /759MJD ..... +175°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Output voltages beyond -5V or bootstrapped operation reduce the allowable supply voltage. See Max Input/Output Differential specifications.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Bootstrapped Mode (Circuit of Figure 1, V+ = 5V, I_{LOAD} = 0mA, DRV- = V_{OUT} (-5V) (MAX739/MAX759), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	DRV- ≥ -7V	MAX736	4.0		8.6	V
	DRV- ≥ -10V	MAX737	4.0		5.5	
	DRV- ≥ -5.25V	MAX739/759	4.0		11.0	
Output Voltage	V+ = 4.5V to 8.6V, I_{LOAD} = 0mA to 100mA	MAX736	-11.40		-12.60	V
	V+ = 6V to 8.6V, I_{LOAD} = 0mA to 125mA		-11.40		-12.60	
	V+ = 4.5V to 5.5V, I_{LOAD} = 0mA to 100mA	MAX737	-14.25		-15.75	
	V+ = 4.5V to 11V, I_{LOAD} = 0mA to 250mA	MAX739	-4.750		-5.250	
		MAX759 (Notes 2, 3)	-4.775		-5.225	
Output Current	V+ = 4.5V to 8.6V	MAX736	100			mA
	V+ = 6V to 8.6V		125			
	V+ = 4.5V to 5.5V	MAX737	100			
	V+ = 4.5V to 11V	MAX739/759 (Note 2)	250	350		
	V+ = 6V to 11V		300	500		
Supply Current		MAX736		4.2	6.0	mA
		MAX737		6.1	9.5	
		MAX739		1.7	3.5	
		MAX759		2.2	4.0	
Standby Current	V_{SHDN} = 0V (Note 4)			1.0	100.0	µA
$\overline{SHDN}$ Logic High Voltage					V+ - 0.5	V
$\overline{SHDN}$ Logic Low Voltage			0.25			V
$\overline{SHDN}$ Input Current				0.1	1.0	µA

ELECTRICAL CHARACTERISTICS (continued)

Bootstrapped Mode (Circuit of Figure 1, V+ = 5V, I_{LOAD} = 0mA, DRV- = V_{OUT} (-5V) (MAX739/MAX759), T_A = T_{MIN} to T_{MAX}, unless

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LX Leakage Current				10		µA
Undervoltage Lockout	Measured at V+			3.7	4.0	V
Reference Voltage	(Note 3)		1.16	1.23	1.30	V
Reference Drift				50		ppm/°C
Compensation-Pin Impedance				6		kΩ
Oscillator Frequency		MAX736/739	145	165	185	kHz
		MAX737/759	145	185	220	

ELECTRICAL CHARACTERISTICS

Non-Bootstrapped Mode (Circuit of Figure 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		MAX736	4.0		8.6	V
		MAX737	4.0		5.5	
		MAX739/759	4.0		15.0	
Output Voltage, No Load (Note 2)	V+ = 4V to 8.6V	MAX736	-11.40		-12.60	V
	V+ = 4V to 5.5V	MAX737	-14.25		-15.75	
	V+ = 4V to 15V	MAX739	-4.750		-5.250	
		MAX759 (Note 2)	-4.775		-5.225	
Output Current	V+ = 8.6V	MAX736		200		mA
	V+ = 5.5V	MAX737		165		
	V+ = 12V	MAX739/759		550		
Supply Current, No Load	V+ = 5V	MAX736/739		1.6	3.0	mA
		MAX737		2.5	4.5	
		MAX759		2.1	4.0	

Note 2: MAX759 output voltage tests are performed using an external resistor divider to set the output voltage to -5V (see Figure 5, R1 = 15kΩ, R2 = 3.69kΩ).

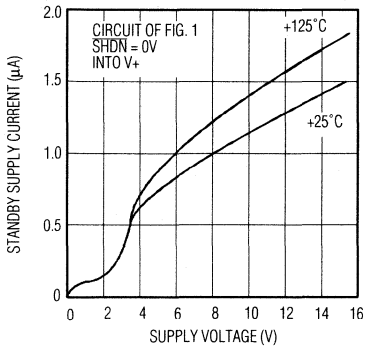
Note 3: Output voltage tolerance is ±4.5% plus external feedback resistor tolerances for the MAX759.

Note 4: The standby supply-current specification is set at 100µA due to test method limitations rather than actual device performance. The two-sigma distribution of standby supply current is less than 10µA (over temperature).

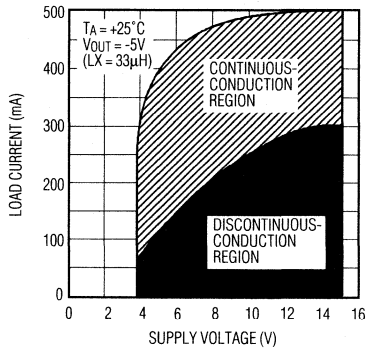
-5V, -12V, -15V, and Adjustable Inverting Current-Mode PWM Regulators

Typical Operating Characteristics

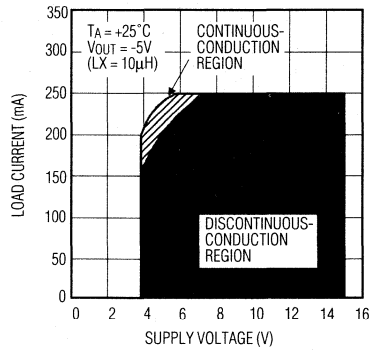
STANDBY SUPPLY CURRENT vs. SUPPLY VOLTAGE



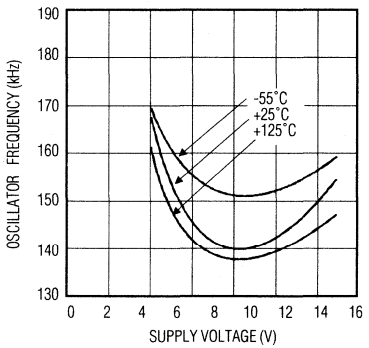
MAX739 CONTINUOUS-CONDUCTION REGION



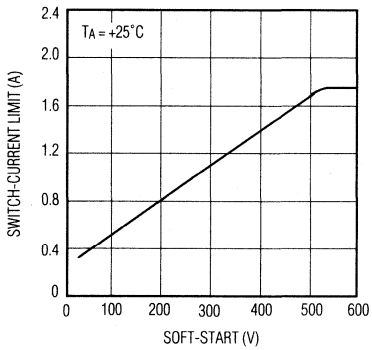
MAX739 DISCONTINUOUS-CONDUCTION REGION



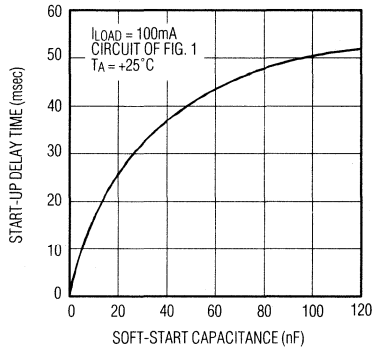
MAX739 OSCILLATOR FREQUENCY vs. TEMPERATURE AND SUPPLY VOLTAGE



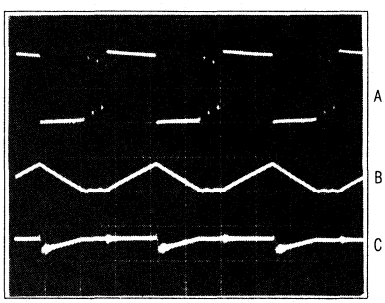
MAX739 SWITCH-CURRENT LIMIT vs. SOFT-START VOLTAGE



SOFT-START DELAY TIME

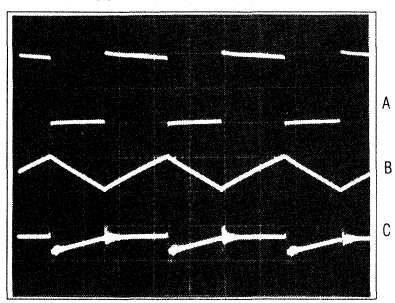


SWITCHING WAVEFORMS - DISCONTINUOUS CONDUCTION



A = Switch Voltage (LX) 5V/div (4.8V to -5.3V)
B = Inductor Current, 500mA/div
C = Output Voltage Ripple, 50mV/div
TIME = 2µs/div
CIRCUIT OF FIG. 1
VIN = +5V
TA = +25°C

SWITCHING WAVEFORMS - CONTINUOUS CONDUCTION

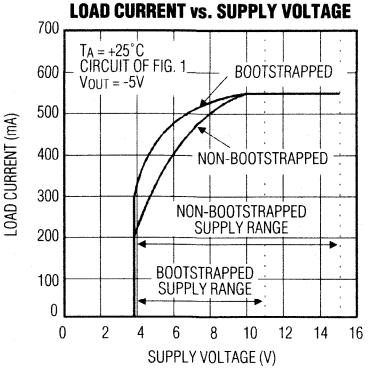


A = Switch Voltage (LX) 5V/div (4.8V to -5.3V)
B = Inductor Current, 500mA/div
C = Output Voltage Ripple, 50mV/div
TIME = 2µs/div
CIRCUIT OF FIG. 1
VIN = +5V
TA = +25°C

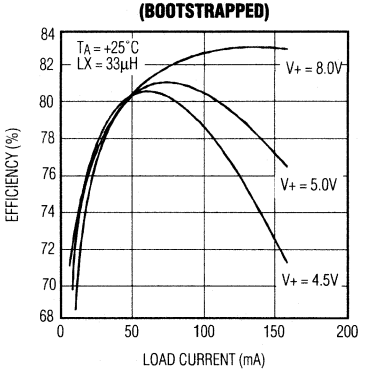
-5V, -12V, -15V, and Adjustable Inverting Current-Mode PWM Regulators

Typical Operating Characteristics (continued)

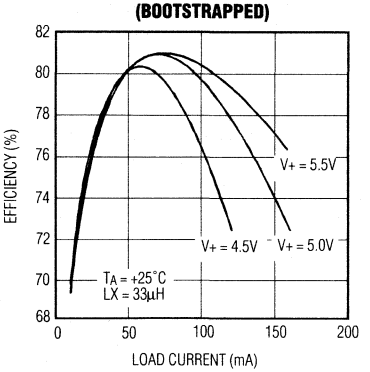
LOAD CURRENT vs. SUPPLY VOLTAGE



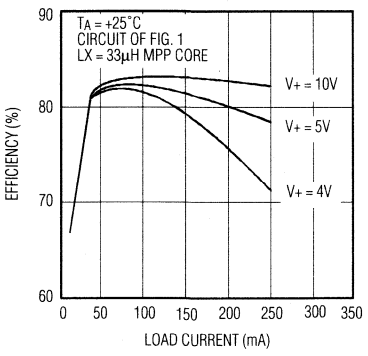
MAX736 EFFICIENCY vs. LOAD CURRENT (BOOTSTRAPPED)



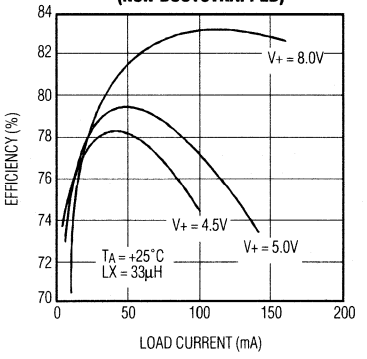
MAX737 EFFICIENCY vs. LOAD CURRENT (BOOTSTRAPPED)



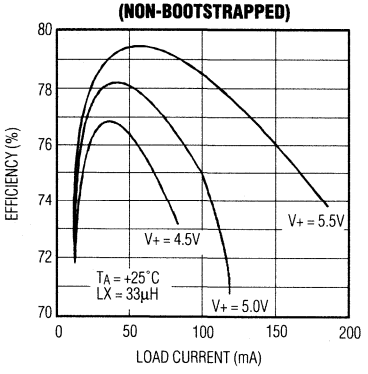
MAX739/MAX759 EFFICIENCY vs. LOAD CURRENT (BOOTSTRAPPED)



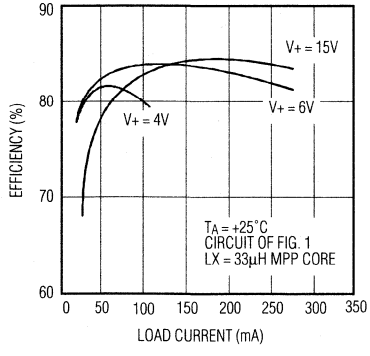
MAX736 EFFICIENCY vs. LOAD CURRENT (NON-BOOTSTRAPPED)



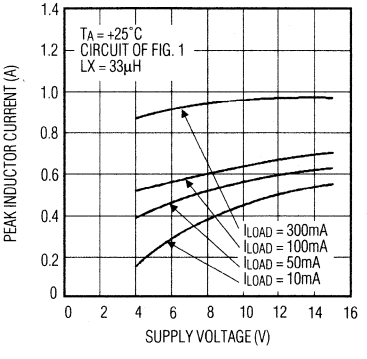
MAX737 EFFICIENCY vs. LOAD CURRENT (NON-BOOTSTRAPPED)



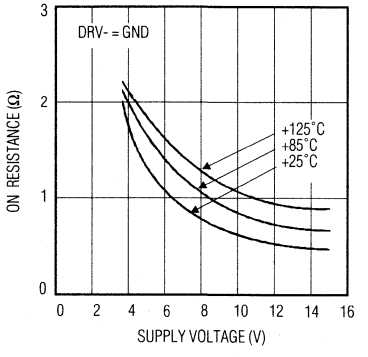
MAX739/MAX759 EFFICIENCY vs. LOAD CURRENT (NON-BOOTSTRAPPED)



PEAK INDUCTOR CURRENT vs. SUPPLY AND LOAD



SWITCH ON RESISTANCE vs. SUPPLY (DRV-) VOLTAGE (NON-BOOTSTRAPPED)

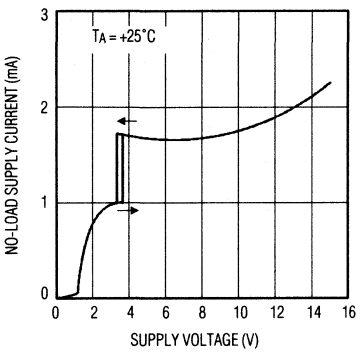


4

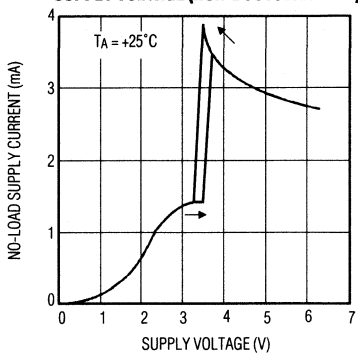
-5V, -12V, -15V, and Adjustable Inverting Current-Mode PWM Regulators

Typical Operating Characteristics (continued)

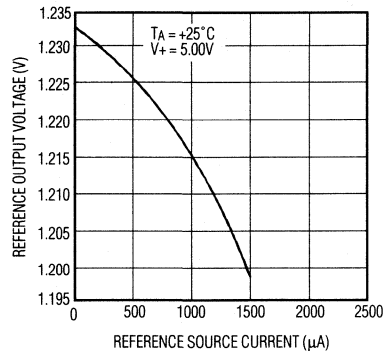
MAX736/MAX739/MAX759 NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE (NON-BOOTSTRAPPED)



MAX737 NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE (NON-BOOTSTRAPPED)



REFERENCE VOLTAGE vs. LOAD CURRENT



Pin Description

PIN		NAME	FUNCTION
14-PIN DIP	16-PIN SO		
1, 13, 14	1, 15, 16	V+	Positive Supply-Voltage Inputs. Connect all V+ pins together. Bypass with at least a 0.1µF capacitor close to V+ and GND pins.
2	2	$\overline{SHDN}$	Shutdown Control. V+ = normal operation, GND = shutdown.
3	3	VREF	Reference Voltage Output = +1.23V. Supplies up to 125µA for external loads.
4, 6	4, 5, 6	N.C.	No Connect. Not internally connected.
5	7	SS	Soft-Start
7	8	CC	Compensation Input. CC is the input of the error amplifier, and is held at virtual ground. For the MAX759, CC is connected to an external resistor divider.
8	9	VOUT	Output Voltage feedback terminal (actually an input). Connected to internal resistors (MAX736/737/739 only). Do not connect on MAX759.
9	10	DRV-	Negative Drive Voltage Input is the negative supply rail for the push-pull stage that drives the internal power FET.
10	11	GND	Ground
11, 12	12, 13, 14	LX	Switch Output - internal P-channel MOSFET drain. Connect all LX pins together.

-5V, -12V, -15V, and Adjustable Inverting Current-Mode PWM Regulators

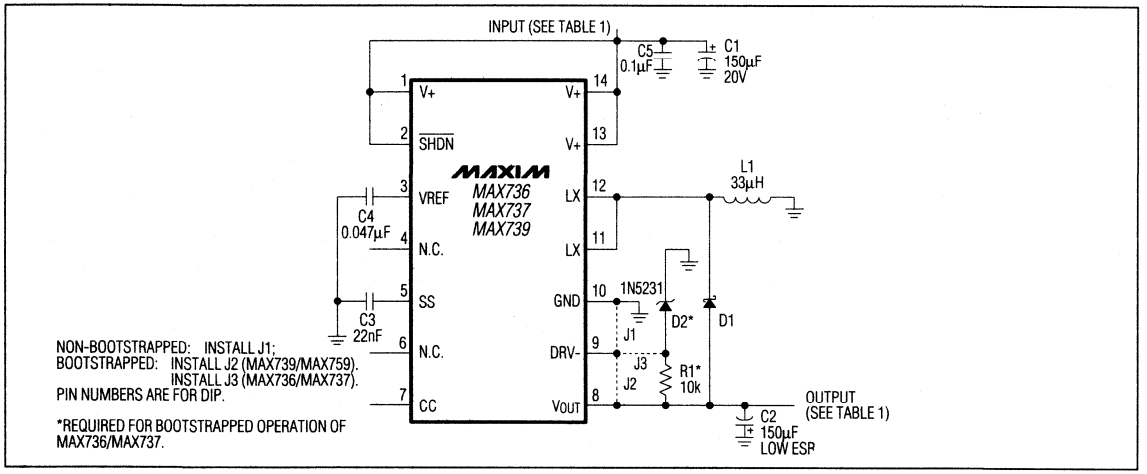


Figure 1. Standard Application Circuit

Table 1. Standard Application Test Circuit Parameters

Device	V+ Range (V)		Output Voltage (V)	Diode D1
	Bootstrapped	Non-Bootstrapped		
MAX736	4 to 8.6	4 to 8.6	-12	1N5818
MAX737	4 to 5.5	4 to 5.5	-15	1N5818
MAX739/759	4 to 11	4 to 15	-5	1N5817/1N5818

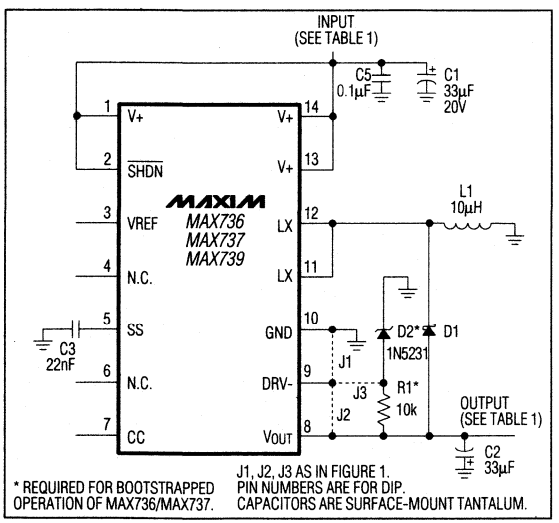


Figure 2. Discontinuous-Conduction Mode Application Using Surface-Mount Components

Detailed Description

Operating Principle

The MAX736/737/739/759 are monolithic CMOS ICs containing a current-mode PWM controller and a 1.5A P-channel power MOSFET. Current-mode control provides excellent line-transient response and AC stability. The switch transistor is a current-sensing MOSFET that splits off a fraction of the total source current for current-limit detection.

Basic Application Circuits

The two basic application circuits are simple designs using off-the-shelf components. The Standard Application Circuit (Figure 1) obtains more output power and somewhat lower noise than the Discontinuous-Mode Application (Figure 2), but requires physically larger components. The discontinuous-mode circuit has only one-third less output current (200mA vs. 300mA at V+ = 5V) and requires much smaller components. Table 2 lists external component suppliers.

-5V, -12V, -15V, and Adjustable Inverting Current-Mode PWM Regulators

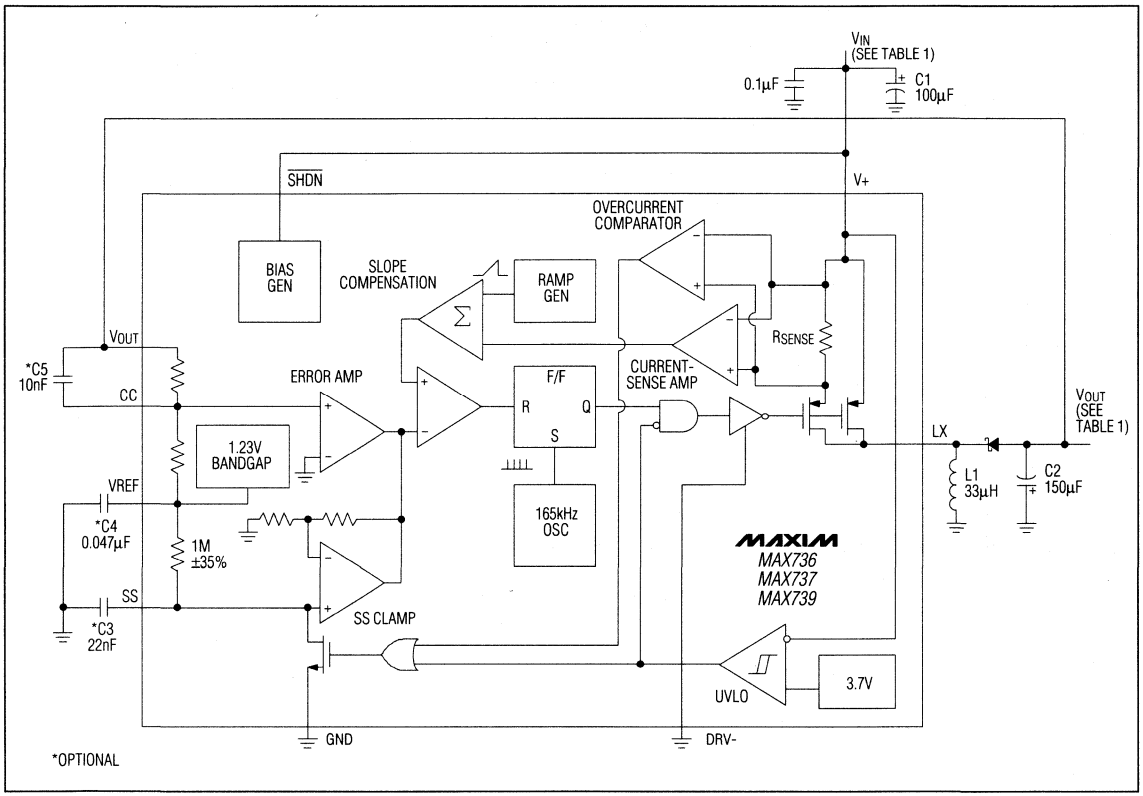


Figure 3. MAX736/737/739 Detailed Block Diagram

Bootstrapped/Non-Bootstrapped Modes

The most important decision in configuring a MAX736/737/739/759 circuit is bootstrapping - whether to connect DRV- to GND or to a negative voltage. This connection determines the input voltage range, available output power, and quiescent supply current as described in the *Typical Operating Characteristics* and *Electrical Characteristics*. DRV- connects to the negative supply rail of the driver stage that drives the internal power MOSFET gate. Increasing the negative voltage applied to DRV- reduces MOSFET on resistance, but the supply current is higher due to the higher gate-source voltage swing. Do not exceed the *Absolute Maximum Ratings* specification for the voltage difference between V+ and DRV- (17V). Intermediate bootstrap voltage levels appropriate for the MAX736/737/759 are obtained by using a zener shunt (Figure 4).

Continuous-/Discontinuous-Conduction Modes

Maximum duty cycle is 90%, so the circuit can be operated in continuous-conduction mode (CCM) or discontinuous-conduction mode (DCM) by selecting higher or lower inductor values. In CCM, the inductor current never decays to zero. In DCM, the inductor current slope is steep enough so it decays to zero before the end of the transistor off time. CCM allows the MAX736/737/739/759 to deliver maximum load current, and is also slightly less noisy than DCM, because it doesn't exhibit the ringing that occurs when the inductor current reaches zero. However, DCM allows for lower output filter capacitor values because there is no continuous-feedback path through the inductor.

-5V, -12V, -15V, and Adjustable Inverting Current-Mode PWM Regulators

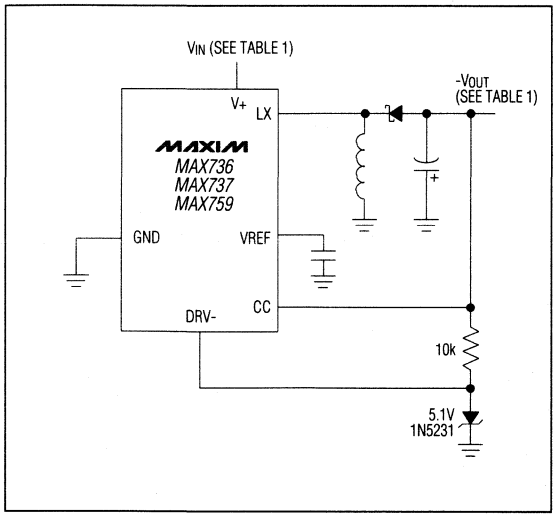


Figure 4. MAX736/738/759 Zener-Bootstrap Scheme

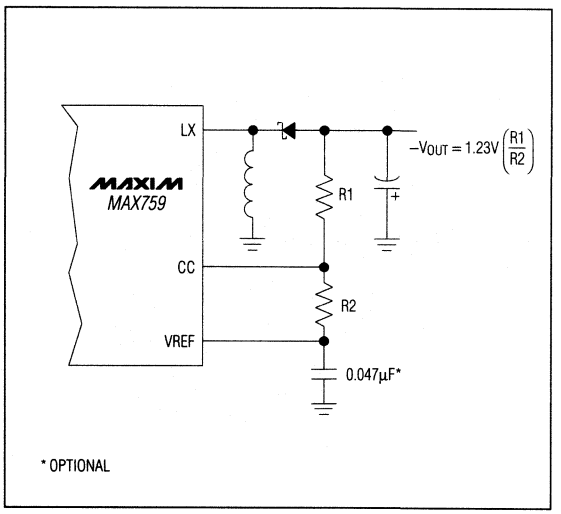


Figure 5. MAX759 Adjustable Output Voltage

AC Compensation

Primary compensation for feedback stability is provided by a dominant pole created by the filter capacitance and load resistance. The ESR of the output filter capacitor introduces a zero in the loop response, which tends to destabilize the loop. In the Standard Application Circuit, the 150µF capacitor (C2) should have a maximum ESR over temperature of 0.5Ω in order to deliver full load at the minimum supply voltage. Operation at higher input voltages with lower inductor values (low enough to force the circuit to operate in discontinuous-conduction mode) or at lower output current than the full load capability reduces the need for large filter capacitors. Surface-mount tantalum capacitors have very low ESR. Consequently, smaller capacitance values are adequate (see Figure 2).

Soft-Start Buffer

The voltage applied to SS determines the peak switch-current limit (see *Typical Operating Characteristics*). A capacitor attached to SS ensures an orderly power-up. SS is pulled up to VREF internally through a 1MΩ resistor. The maximum current limit can be fixed externally at a lower than normal value by clamping SS to a voltage less than VREF. An SS cycle is initiated whenever either an undervoltage lockout or overcurrent fault condition triggers an internal transistor to discharge the SS capacitor to ground. Note that the SS capacitor should be at least 10nF. When peak inductor currents at start-up are small, this capacitor may be omitted.

Undervoltage Lockout

The undervoltage lockout allows operation for supply voltages greater than 3.7V typ (4V guaranteed), with 0.25V of hysteresis. Internal control logic holds the output power MOSFET in an off state until the supply rises above the undervoltage threshold, at which time an SS cycle begins.

Inductor Selection

Practical nominal inductor values are in the 10µH to 50µH range. Low inductor values force discontinuous-conduction modes (see the *Continuous-/Discontinuous-Conduction Modes* section). The inductor must have a saturation (incremental) current rating greater than the peak switch current obtained from the Peak Switch Current vs. Load Current graph under *Typical Operating Characteristics*.

The MAX739 contains a slope-compensation circuit that provides AC compensation for the current-mode PWM. This slope-compensation circuit is internally fixed to provide ideal slope compensation for an inductor value of 33µH.

Adjustable Output

Adjust the MAX759's output voltage from 0V to -15V by selecting the appropriate external resistor divider (Figure 5). Output voltages beyond -15V require a transformer to protect the power MOSFET from overvoltage. With R2 feedback resistor (5kΩ to 15kΩ), a compensation capacitor (typically 10nF) from the output to CC gives best transient-response characteristics. Be careful to observe the *Absolute Maximum Ratings* on the difference between input voltage and output voltage.

-5V, -12V, -15V, and Adjustable Inverting Current-Mode PWM Regulators

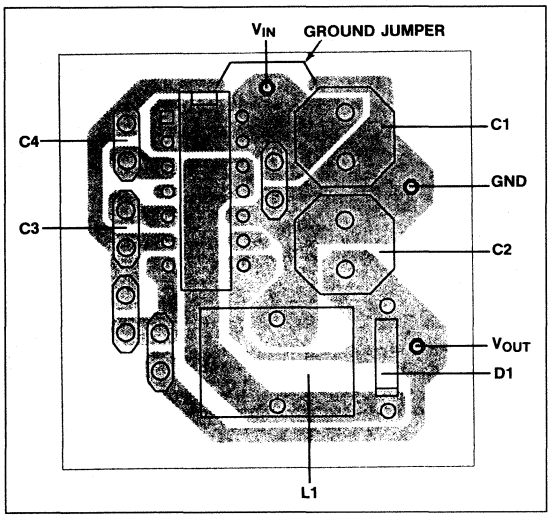


Figure 6. MAX739 Low-Noise PC Layout

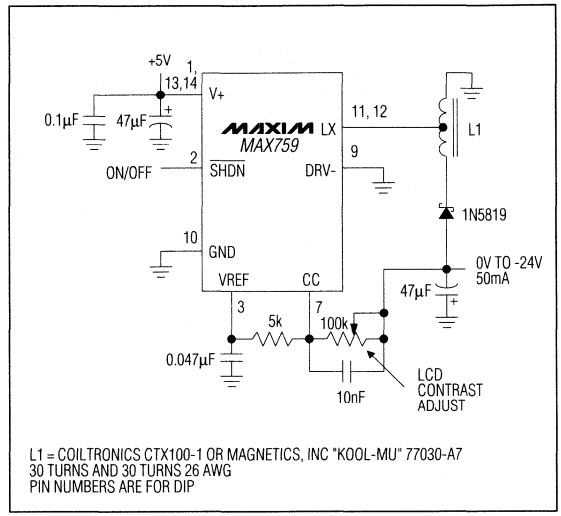


Figure 8. -24V LCD Power Supply

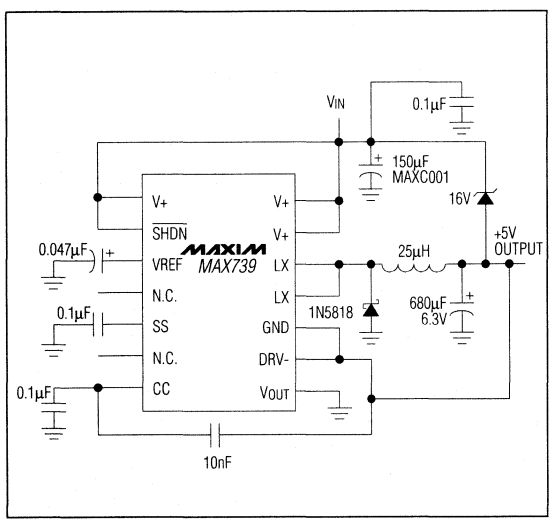


Figure 7. MAX739 +5V Step-Down Application

Printed Circuit Layout and Grounding

Good layout and grounding practices will help achieve low-noise, jitter-free operation. Minimize wiring lengths in the high-current paths, especially the distance between the inductor and the return leads of the filter and bypass capacitors (C1 and C2 of Figure 1). These high-current ground connections should be brought to a single common point (a "star" ground). Place a low-ESR bypass capacitor directly at the V+ and GND pins of the IC (C5 in Figure 1).

The suggested low-noise printed circuit (PC) layout of Figure 6 is configured for the low-cost, radial through-hole components specified in the standard application circuit. The layout is hard-wired into the non-bootstrapped mode.

Applications Information

+5V Step-Down Application

The MAX739/MAX759 can operate as step-down (buck) regulators with a positive output (Figure 7). Because their supply currents flow into the load, this +5V step-down circuit offers good efficiency even at low load currents: 60% to 85% from 3mA, up to the full-load capability of 1A. It requires a minimum load of 3mA, however. The input voltage range is 9V to 21V. If the input does not exceed 15V, ground DRV- for higher efficiency and remove the zener.

-24V LCD Power Supply

This circuit generates an adjustable negative voltage for powering small LCD displays, and will deliver 30mA at -24V with 80% efficiency (Figure 8). A simple autotransformer safely steps up the output voltage beyond the voltage breakdown rating of the internal power MOSFET. The autotransformer (tapped inductor) specified on the schematic is a miniature (0.25" diameter) toroid. This autotransformer approach is slightly better than a flyback transformer due to superior magnetic coupling and a reduction of turns.

Table 2. Component Suppliers

PRODUCTION METHOD	INDUCTORS	CAPACITORS
Surface Mount	Sumida USA: Phone (708) 956-0666 Japan: Phone (03) 3607-5111 FAX (03) 3607-5428 CD54-330 (33µH) CD54-100 (10µH) Coiltronics Phone (305) 781-8900 FAX (305) 782-4163 CTX 100 series	Matsuo USA: Phone (714) 969-2491 FAX (714) 960-6492 Japan: Phone (06) 332-0871 267 series
Miniature Through-Hole	Sumida USA: Phone (708) 956-0666 Japan: Phone (03) 3607-5111 FAX (03) 3607-5428 RCH654-330 (33µH) RCH108-330 (33µH)	Sanyo Os-Con USA: Phone (619) 661-6322 Japan: Phone (0720) 70-1005 FAX (0720) 70-1174 OS-CON series Low ESR Organic Semiconductor
Low-Cost Through-Hole	Renco Phone (516) 586-5566 FAX (516) 586-5562 RL 1284-33	Nichicon Phone (708) 843-7500 FAX (708) 843-2798 PL series Low ESR Electrolytics United Chemi-Con Phone (708) 696-2000 FAX (708) 640-6311 LXF series

For wide temperature applications using through-hole components, organic semiconductor capacitors are recommended (C1 and C2 in Figure 1). These capacitors maintain low ESR across their operating temperature range.

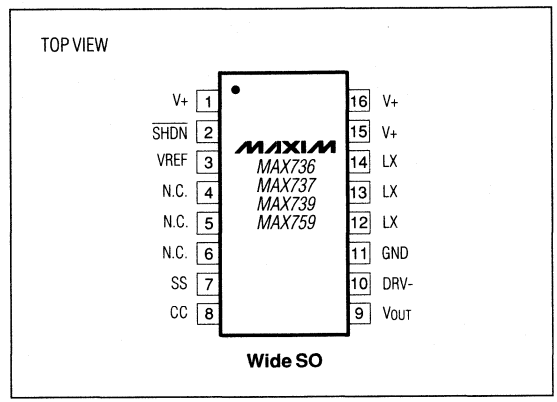
-5V, -12V, -15V, and Adjustable Inverting Current-Mode PWM Regulators

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX739CPD	0°C to +70°C	14 Plastic DIP
MAX739CWE	0°C to +70°C	16 Wide SO
MAX739C/D	0°C to +70°C	Dice*
MAX739EPD	-40°C to +85°C	14 Plastic DIP
MAX739EWE	-40°C to +85°C	16 Wide SO
MAX739MJD	-55°C to +125°C	14 CERDIP**
MAX759CPD	0°C to +70°C	14 Plastic DIP
MAX759CWE	0°C to +70°C	16 Wide SO
MAX759C/D	0°C to +70°C	Dice*
MAX759EPD	-40°C to +85°C	14 Plastic DIP
MAX759EWE	-40°C to +85°C	16 Wide SO
MAX759MJD	-55°C to +125°C	14 CERDIP**

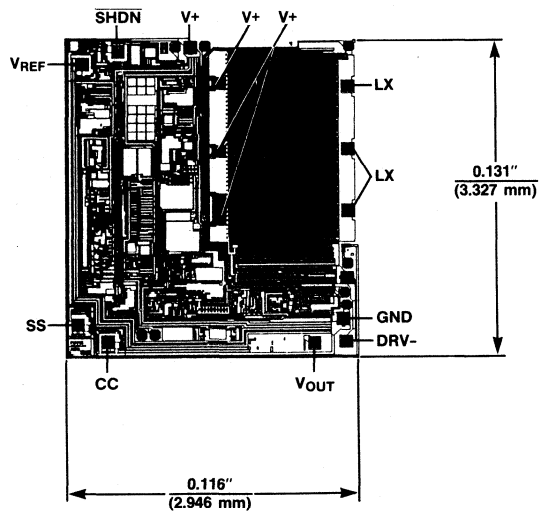
*Contact factory for dice specifications.
**Contact factory for availability and processing to MIL-STD-883.

Pin Configurations (continued)



Wide SO

Chip Topography



Note: Connect substrate to V+. Transistor count: 274

ADVANCE INFORMATION
All information in this data sheet is preliminary and subject to change.
7/92

MAXIM

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

General Description

The MAX741 is a highly versatile switch-mode power-supply (SMPS) controller IC that operates from an input supply as low as 2.5V.

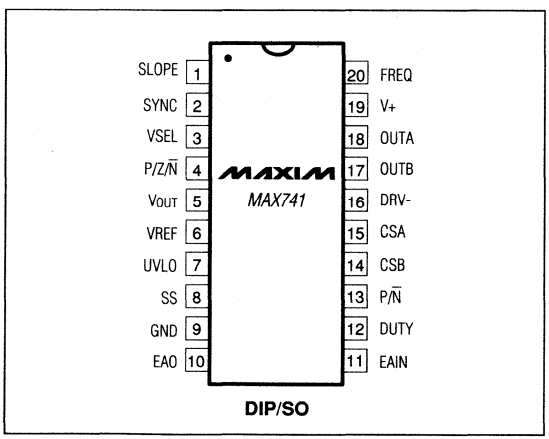
The MAX741 can be pin-programmed into hundreds of different SMPS configurations. The internal blocks (reference, error amplifier, etc.) are interconnected via analog switches, so they can be reconfigured into different architectures by applying trilevel data (V+, VREF, GND) to certain logic input pins. This pin-programming feature lends tremendous application flexibility. For example, the output stage can drive N-channel or P-channel MOSFETs (or bipolar transistors) in single-ended, complementary, or push-pull modes. The error amplifier can accommodate positive or negative feedback voltages. The output voltage can be adjusted with external resistors, or it can be set at any one of six preset values by switching in the appropriate laser-trimmed resistor-divider network.

The MAX741 is 100% tested as a complete system, including external components—not just a collection of individually tested functional blocks. This testing guarantees ±4% output voltage tolerance over temperature. For mainstream applications, these circuits can be designed directly into the system with little effort. At the same time, the MAX741 provides the power-supply designer the right inputs and controls to implement nearly any SMPS function.

Applications

Battery-Operated Equipment
Distributed Power Systems
Isolated Off-Line Supplies
On-Card DC-DC Converters

Pin Configuration



DIP/SO

Features

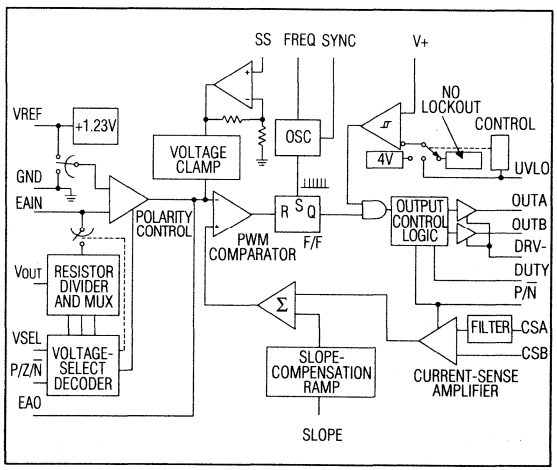
- ♦ **Pin-Programmable Architecture**
- ♦ **Operates on Supply Voltages from 2.5V**
- ♦ **Low Supply Current — 3.5mA Max**
- ♦ **Bootstrap Input for Low-Voltage Applications**
- ♦ **Current-Mode PWM Control**
- ♦ **Cycle-by-Cycle Current Limiting**
- ♦ **Adjustable Undervoltage Lockout and Soft-Start**
- ♦ **Oscillator Synchronization Input/Output**
- ♦ **Shutdown-Control Input**
- ♦ **Low-Noise, Fixed-Frequency Operation**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX741UCPP	0°C to +70°C	20 Plastic DIP
MAX741UCAP	0°C to +70°C	20 SSOP
MAX741UC/D	0°C to +70°C	Dice*
MAX741UEPP	-40°C to +85°C	20 Plastic DIP
MAX741UEAP	-40°C to +85°C	20 SSOP
MAX741UMJP	-55°C to +125°C	20 CERDIP**

Ordering Information continued on last page.
** Dice are tested at T_A = +25°C only.*
*** Contact factory for availability and processing to MIL-STD-883.*

Block Diagram



Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V+ to GND ..... +17V, -0.3V
Oscillator Output Voltage (SYNC) ..... -0.3V to (V+ + 0.3V)
MOSFET Driver Supply Voltage (DRV- to V+) ..... +0.3V, -17V
Feedback Voltage (V_{OUT} to GND) ..... ±50V
Auxiliary Input Voltages (SLOPE, SS, VSEL, P/Z/$\overline{N}$, EAIN, DUTY, P/$\overline{N}$, CSA, CSB, FRQ to GND) .....-0.3V to (V+ + 0.3V)
Peak Output Current (I_{OUTA} or I_{OUTB}) 1.0A
Reference Current (I_{VREF}) 2.5mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 10.00mW/°C above +70°C) 800mW
SSOP (derate 8.00mW/°C above +70°C) 600mW
Operating Temperature Ranges:
MAX741_C_ ..... 0°C to +70°C
MAX741_E_ ..... -40°C to +85°C
MAX741_MJP ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply-Voltage Range		2.7		15.5	V
Start-Up Supply Voltage	T_A = +25°C, UVLO = V+		1.8		V
Shutdown-Mode Supply Current	FRQ = 0V, T_A = +25°C		50	150	µA
Reference Voltage		1.17	1.23	1.29	V
Reference-Voltage Line Regulation	V+ = 2.75V to 15.5V		0.5		mV/V
Reference-Voltage Load Regulation	I_{LOAD} = 0µA to 300µA, T_A = +25°C, MAX741N only		1.4	10	mV
Oscillator Frequency	FRQ = V+, T_A = +25°C	110	145	170	kHz
	FRQ = VREF, T_A = +25°C		140		
SYNC Output Low Voltage	I_{OL} = 25µA, used as clock output		0.2		V
SYNC Output High Voltage	I_{OH} = 25µA, used as clock output		4.8		V
SYNC Input Current	V_{IH} = V+		1.0		mA
	V_{IL} = 0V		-1.0		
Error-Amplifier Input Bias Current	VCM = 0V to VREF, P/Z/$\overline{N}$ = VREF		0.005	10	µA
Error-Amplifier Open-Loop Gain	EAO = 2V to 3V		2000		V/V
Output Voltage Low	OUTA or OUTB, T_A = +25°C, I_{OL} = 50mA		0.65	0.95	V
	I_{OL} = 50mA, DRV- = -10V		-9.85	-9.50	
Output Voltage High	OUTA or OUTB, T_A = +25°C, I_{OH} = -50mA	4.10	4.35		V
	I_{OH} = -50mA, DRV- = -10V	4.50	4.70		
Output Rise or Fall Time	OUTA or OUTB, T_A = +25°C, C_{LOAD} = 1nF (Note 2)		50	100	ns
UVLO Threshold	Adjustable mode, measured at UVLO (Note 2)	0.435 x VREF	0.45 x VREF	0.465 x VREF	V

ELECTRICAL CHARACTERISTICS – MAX741U

(Step-Up Circuit of Figure 1 (TBD), V+ = 5V, T_A = T_{MIN} to T_{MAX}, I_{LOAD} = 0mA, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Initial Accuracy	Fixed modes, referred to V_{OUT}, V+ = 3.3V, VSEL = V+ (Note 3)	4.80	5.00	5.20	V
	VSEL = VREF, T_A = +25°C	11.52	12.00	12.48	
	VSEL = 0V, T_A = +25°C	14.40	15.00	15.60	
	Adjustable mode, referred to error-amplifier input	1.18	1.23	1.28	
Supply Current	VSEL = V+ = 3.3V (Note 1)		1.6	3.5	mA

ELECTRICAL CHARACTERISTICS – MAX741N

(Inverting Circuit of Figure 2 (TBD), V+ = 5V, T_A = T_{MIN} to T_{MAX}, I_{LOAD} = 0mA, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Initial Accuracy	Fixed modes, referred to V_{OUT}, VSEL = V+ (Note 3)	-5.20	-5.00	-4.80	V
	VSEL = VREF, T_A = +25°C	-12.48	-12.00	-11.52	
	VSEL = 0V, T_A = +25°C	-15.60	-15.00	-14.40	
	Adjustable mode, R1 = 50kΩ, R2 = 50kΩ	-5.4	-5.2	-5.0	
Supply Current	VSEL = V+ = 12V (Note 1)		2.2	4.0	mA

ELECTRICAL CHARACTERISTICS – MAX741D

(Step-Down Circuit of Figure 3 (TBD), V+ = 5V, T_A = T_{MIN} to T_{MAX}, I_{LOAD} = 0mA, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Initial Accuracy	Fixed modes, referred to V_{OUT}, VSEL = V+ (Note 3)	4.80	5.00	5.20	V
	Adjustable mode, referred to error-amplifier input	1.18	1.23	1.28	
Supply Current	VSEL = V+ (Note 1)		2.8	4.0	mA

Note 1: Total supply current under actual operating conditions, including currents drawn by components.
Note 2: Guaranteed, but not 100% tested.
Note 3: Output Voltage Initial Accuracy tests include the effects of the error-amplifier input offset voltage.

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

Pin Description

PIN	NAME	FUNCTION
1	SLOPE	Sets slope compensation for AC stability. Normally a 50kΩ to 1MΩ resistor connected to ground. Required for continuous-conduction mode operation.
2	SYNC	SYNC output at the oscillator frequency. Also functions as a clock input when driven externally. Capacitive loads reduce oscillator frequency up to 25%. When using an external clock, the clock's high time corresponds to power switch-off time.
3	VSEL	Voltage Select (VSEL) and P/Z/$\overline{N}$ are decoded to determine the output voltage. See Table 2 under *Output Voltage Selection*. Fixed Output / Adjustable Output V+ = 5V Output / V+ = Positive Output VREF = 12V Output / VREF = Not Allowed GND = 15V Output / GND = Negative Output
4	P/Z/$\overline{N}$	See VSEL (pin 3). V+ = Positive Output (P) VREF = Adjustable Mode (Z) GND = Negative Output (N)
5	V_{OUT}	Output Voltage connection to internal resistor dividers. Leave open-circuit in adjustable mode.
6	VREF	Voltage-Reference Output that can source 300µA for external loads. Bypass with 1µF minimum.
7	UVLO	Undervoltage Lock-Out disables IC when V+ is less than the UVLO threshold. V+ = No Lockout 0.47V+ to 0.07V+ = adjustable threshold GND = 4V threshold
8	SS	Soft-Start and current-limit adjust. A DC voltage applied here sets the maximum peak switch-current limit. An RC network reduces surge currents on start-up. Connect a 150kΩ resistor from VREF to SS and 0.1µF from SS to GND for a 15ms soft-start time. Always connect from 50kΩ to 1MΩ between VREF and SS.
9	GND	Ground
10	EAO	Error-Amplifier Output
11	EAIN	Error-Amplifier Input
12	DUTY	Duty-Cycle Adjust when DUTY = V+: push-pull mode, 50% max duty cycle DUTY = V+ and FREQ = REF: push-pull mode, 85% max duty cycle DUTY = VREF: complementary, 50% max duty cycle DUTY = GND and FREQ = V+: complementary, 85% max duty cycle DUTY = GND and FREQ = REF: complementary mode, 95% max duty cycle
13	P/$\overline{N}$	N-Channel/P-Channel – selects current-sense amplifier output polarity and controls OUTA and OUTB polarity when in push-pull mode. V+ = N-Channel (CS inputs sense around GND) GND = P-Channel (CS inputs sense around V+)
14	CSA	Current-sense amp "A" input. Connects to signal side of current-sense resistor. Signal passes through a 1st-order LP filter.
15	CSB	Current-sense amp "B" input. Connect to V_{IN} in buck and inverting circuits. Connect to GND in step-up circuits. CSB should be bypassed with 0.1µF located close to CSB and GND when in the buck or inverting power-supply modes.

Pin Description (continued)

PIN	NAME	FUNCTION
16	DRV-	Negative Drive Bootstrap Supply Voltage Input accepts a DC bias voltage as the negative supply rail for the drivers at EXTA and EXTB. Used for driving P-channel MOSFETs. Observe *Absolute Maximum Ratings* carefully. When V+ > 14V, use 10Ω in series between OUTA and gate of power FET.
17	OUTB	Output B MOSFET Driver drives P-Channel or PNP transistors in complementary modes. See Table 3. When V+ > 14V, use 10Ω in series between OUTB and gate of power FET.
18	OUTA	Output A MOSFET Driver drives N-channel or NPN transistors in complementary modes.
19	V+	Positive Supply Voltage +2.5V to +16V. Bypass with at least 0.1µF close to V+ and GND pins of IC.
20	FREQ	Frequency/Shutdown Control sets oscillator frequency or forces a non-operating shutdown mode. When tied to VREF, a 22kΩ pull-up resistor from FREQ to V+ is required to ensure start-up. V+ = 145kHz with 85% duty cycle VREF = 140kHz with 95% duty cycle GND = Shutdown Mode

Application Circuits

Inverting Converter 12V to -5.2V at 1.5A

Figure 4's circuit is designed to supply a fixed -5.2V at 1.5A for ECL applications. The input supply range is from 7.6V to 15V and should be bypassed with a low-ESR aluminum electrolytic, such as Nichicon PL series or Sanyo Os-Con series. Bypass capacitors must be placed directly at the V+ and GND pins.

The undervoltage lockout is set to 7.57V with an external voltage divider. This function protects the switching device from damage when the supply voltage is too low for operation. With the pin programming chosen, the regulator operates at a 145kHz switching frequency with an 85% duty cycle. The SYNC pin can be driven for other switching frequencies when desired. Table 1 shows this circuit's efficiency for different input voltages and load currents.

To minimize output ripple, use low-ESR aluminum electrolytic capacitors, since ripple is predominantly a

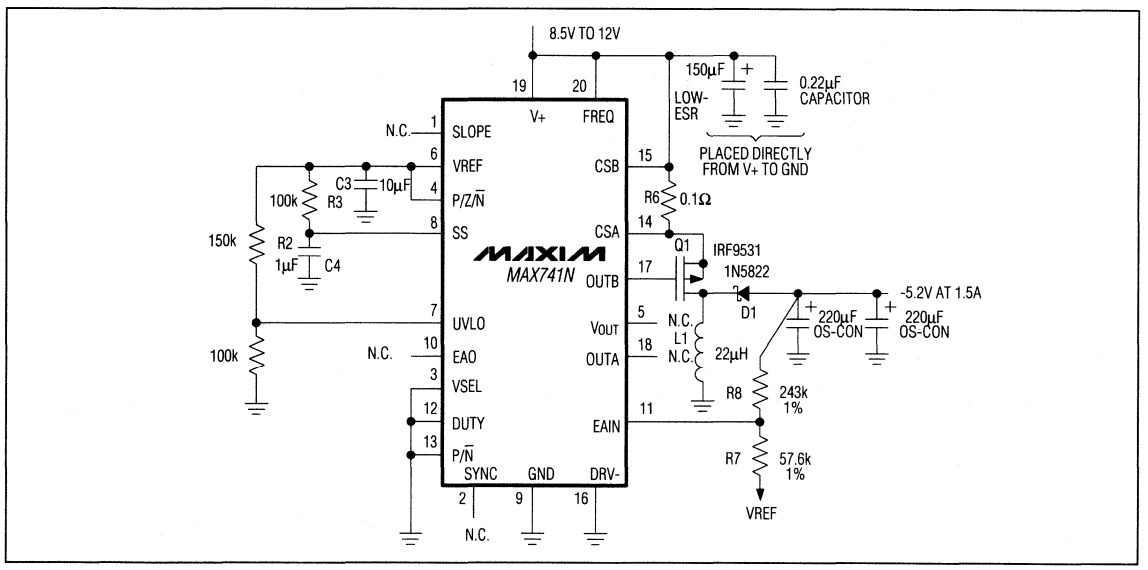


Figure 4. 12V to -5.2V at 1.5A ECL Power Supply

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

function of inductor current causing an IR-drop across the ESR of the capacitor. An additional L-C filter can add another 20dB ripple rejection.

Table 1. ECL Supply Efficiency

V_{IN} (V)	I_{OUT} (A)	EFFICIENCY (%)
12	0.1	73
8.5	0.5	81.5
10	0.5	83
12	0.5	85
8.5	1	78
10	1	81
12	1	82

Table 2. Output Voltage

VSEL	P/Z/$\overline{N}$	OUTPUT	EAIN IMPEDANCE (Ω)
V+	V+	5V	>1k
V+	VREF	Adj. Positive	>50M HiZ
V+	GND	-5V	>13k
VREF	V+	12V	>6.5k
VREF	VREF	Prohibited	NA
VREF	GND	-12V	>13k
GND	V+	15V	>6.5k
GND	VREF	Adj. Negative	>50M HiZ
GND	GND	-15V	>11k

Table 3. Output Stage Programming

DUTY	P/$\overline{N}$	FREQ	OUTA	OUTB	MODE
V+	V+	V+, VREF	N	P	Push-pull
V+	GND	V+, VREF	N	P	Push-pull
V+	V+	GND	GND	GND	Shutdown
V+	GND	GND	V+	V+	Shutdown
VREF	V+	V+, VREF	N	P	Complementary output 50%
VREF	GND	V+, VREF	N	P	Complementary output 50%
VREF	X	GND	GND	V+	Shutdown
GND	V+	V+, VREF	N	P	Complementary output 85% or 95%
GND	GND	V+, VREF	N	P	Complementary output 85% or 95%
GND	X	GND	GND	V+	Shutdown

N = Drives N-Channels (On = V+)
P = Drives P-Channels (On = GND)
X = Don't Care

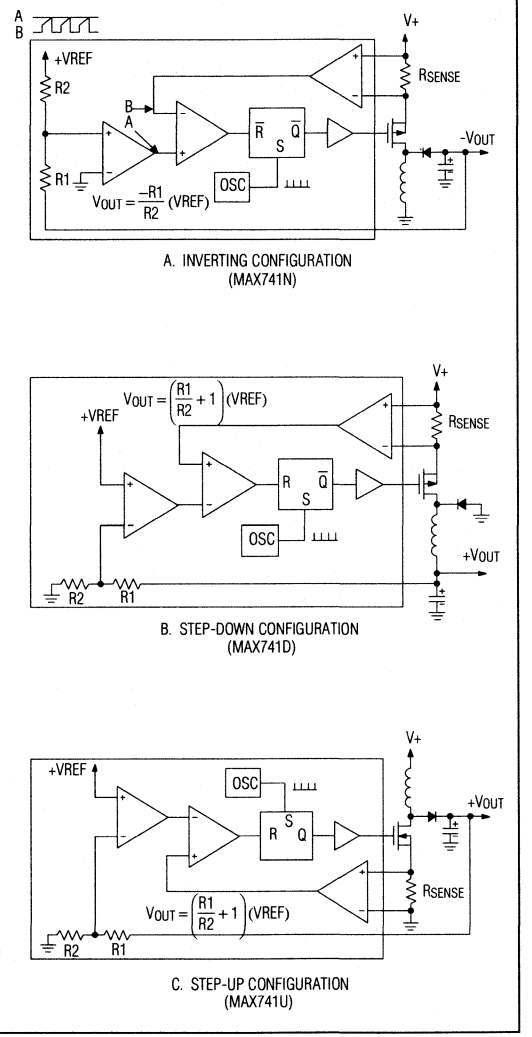


Figure 5. Configurations Used to Guarantee Closed-Loop Electrical Characteristics

+5V Stepdown Converter

Figure 7 shows a 10W to 15W stepdown converter. C1A, B, and C should be placed close to the IC's V+ and GND pins. Nichicon PL series capacitors are recommended for commercial temperature range use. Sanyo Os-Con series capacitors are recommended for use at temperatures less than 0°C. Surface-mount solid tantalum capacitors are also suitable for use over the extended temperature range. GND and V+ connections should be nodal (star connection).

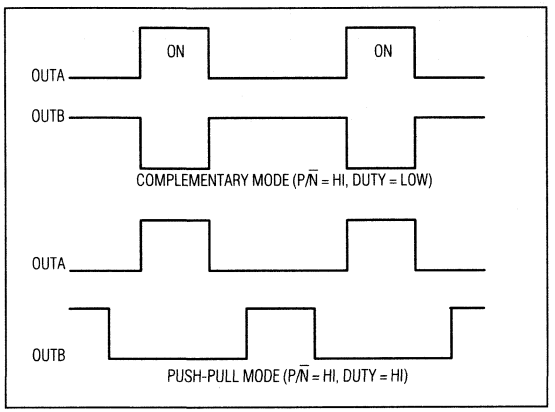


Figure 6. Push-Pull and Complementary Waveforms

Step-Up Converter (+5V to +12V/+15V)

This simple boost converter (Figure 8) uses logic-level FETs and has its power-stage transfer function programmed for operation down to +4.5V, optimizing the circuit for +5V supply operation. This circuit also accepts input voltages up to 10V and is easily modified for other output voltages. Nominal output current is 0mA to 400mA, which can be extended by increasing the output filter capacitance, reducing the sense resistor and inductor value (and scaling the slope compensation resistor to match), and heatsinking the power MOSFET. The operating temperature range is 0°C to +105°C, limited by the output filter capacitors. For extended low temperature operation, increase the output filter capacitance or use wide temerature range types such as organic semiconductor capacitors. C2 is placed close to V+ and GND; C1, C3, and C4 are low-ESR capacitors.

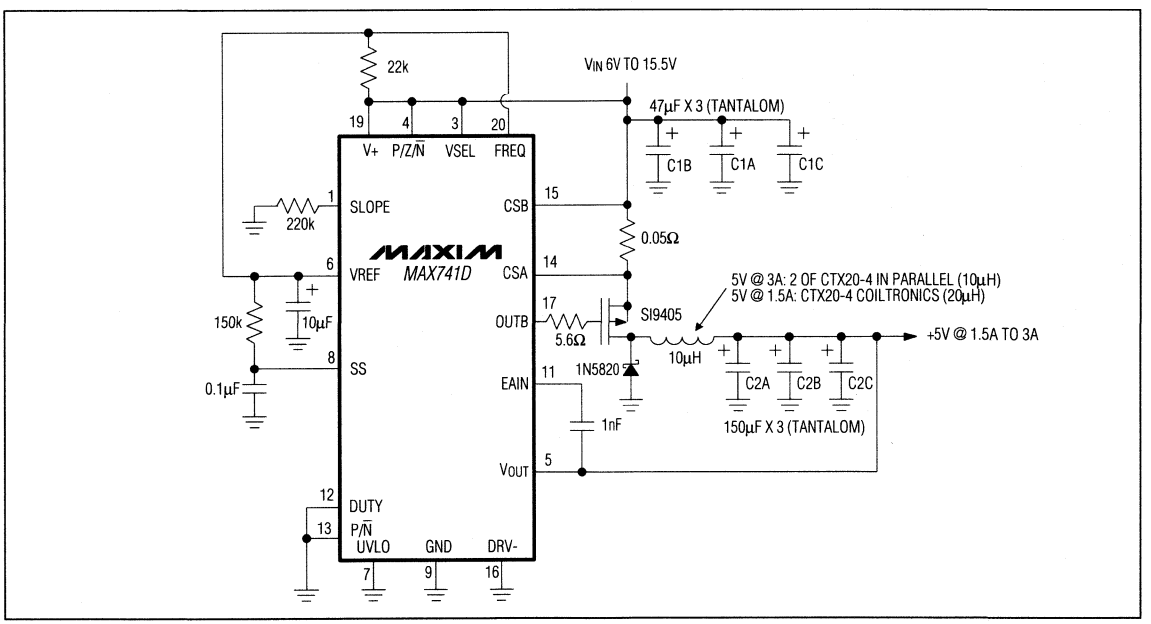


Figure 7. 6V to 15.5V Input Buck Converter Supplies 5V at 3 Amps

Pin-Programmed, Low-Voltage, Current-Mode SMPS Controller

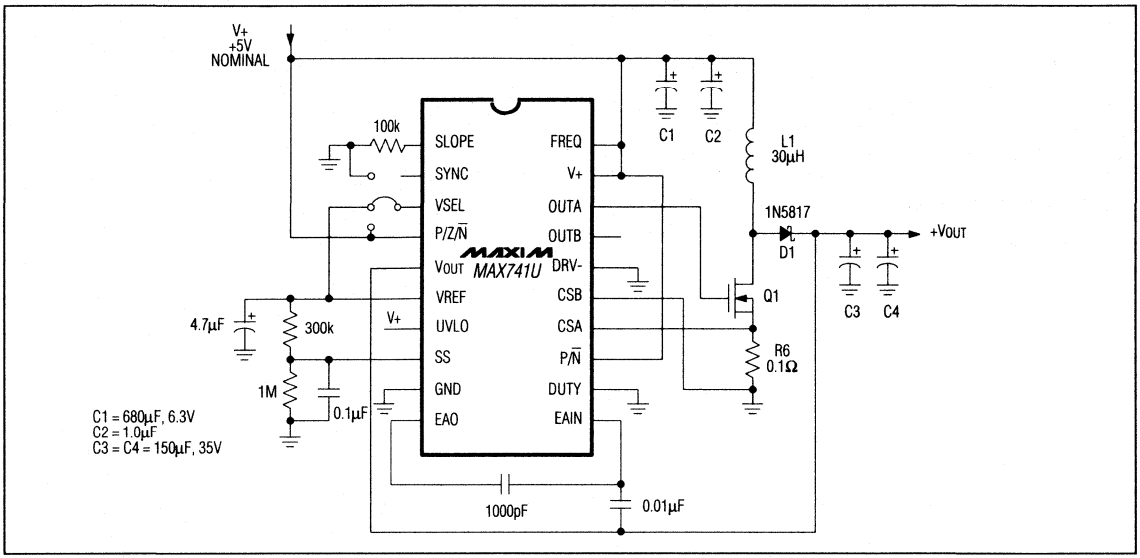


Figure 8. Step-Up Converter Provides +12V or +15V from 5V Input at 400mA Load

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX741DCPP	0°C to +70°C	20 Plastic DIP
MAX741DCAP	0°C to +70°C	20 SSOP
MAX741DC/D	0°C to +70°C	Dice*
MAX741DEPP	-40°C to +85°C	20 Plastic DIP
MAX741DEAP	-40°C to +85°C	20 SSOP
MAX741DMJP	-55°C to +125°C	20 CERDIP**
MAX741NCPP	0°C to +70°C	20 Plastic DIP
MAX741NCAP	0°C to +70°C	20 SSOP
MAX741NC/D	0°C to +70°C	Dice*
MAX741NEPP	-40°C to +85°C	20 Plastic DIP
MAX741NEAP	-40°C to +85°C	20 SSOP
MAX741NMJP	-55°C to +125°C	20 CERDIP**

** Dice are tested at T_A = +25°C only.*
*** Contact factory for availability and processing to MIL-STD-883.*

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

+5V-Output, Step-Up, Current-Mode PWM DC-DC Converter

General Description

The MAX751 is a +5V-output, CMOS, step-up, switch-mode DC-DC converter. Minimum input start-up voltage is 1.2V. From a 2.7V supply, the output current is guaranteed to be 150mA. Battery-saving features include 85% typical full-load efficiency, 2mA operating quiescent supply current, and 35µA shutdown supply current. The shutdown mode can be directly controlled by a microprocessor via the logic-compatible $\overline{SHDN}$ pin.

The MAX751 is tested in-circuit, so output power specifications are guaranteed over all line, load, and temperature ranges. The typical operating circuit uses tiny surface-mounted components, including a miniature 22µH inductor, and fits into less than $0.5in^2$.

The MAX751 uses current-mode pulse-width modulation (PWM) control to provide precise output regulation and low subharmonic noise. A fixed 170kHz oscillator frequency facilitates ripple filtering and allows for the use of tiny external capacitors.

For higher-current solutions, refer to the MAX731/MAX752 data sheet and evaluation kit (MAX731EVKIT-DIP). The MAX751 can be evaluated using the MAX731EVKIT-DIP.

Applications

Local +5V Supply in +3V - Only Systems

Cellular Phones

RF Transmitter Supply

Palmtop and Notebook Computers

Battery-Powered and Hand-Held Instruments

Features

- ♦ **+5V Preset Output**
- ♦ **Guaranteed 150mA Output Current**
- ♦ **1.2V Minimum Start-Up Supply Voltage**
- ♦ **85% Typical Efficiencies at Full Load**
- ♦ **Small 22µH Inductor - No Component Design Required**
- ♦ **2mA Quiescent Current**
- ♦ **35µA Logic-Controlled Shutdown Mode**
- ♦ **Overcurrent and Soft-Start Protection**
- ♦ **170kHz High-Frequency Current-Mode PWM**
- ♦ **8-Pin DIP and SO Packages**

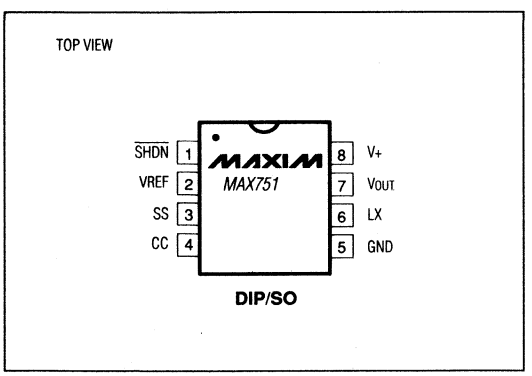
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX751CPA	0°C to +70°C	8 Plastic DIP
MAX751CSA	0°C to +70°C	8 SO
MAX751C/D	0°C to +70°C	Dice*
MAX751EPA	-40°C to +85°C	8 Plastic DIP
MAX751ESA	-40°C to +85°C	8 SO
MAX751MJA	-55°C to +125°C	8 CERDIP**

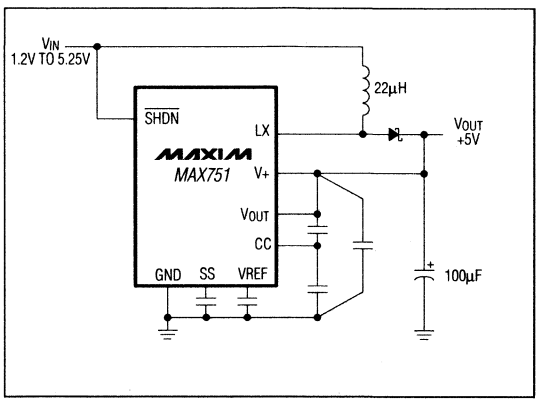
** Contact factory for dice specifications.*

*** Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



Typical Operating Circuit



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

Adjustable, Negative-Output Inverting Current-Mode PWM Regulator

General Description

The MAX755 is a CMOS inverting switch-mode regulator with an internal power MOSFET. It operates from a 2.7V to 11V input and generates an adjustable negative output. 1W output power is guaranteed when powered from a +4.5V input. Quiescent supply current is typically 1.6mA, and a shutdown mode reduces this to 10µA. These power-conserving features along with high efficiency and an application circuit that lends itself to miniaturization, make the MAX755 excel in a broad range of on-card and portable-equipment applications.

The MAX755 employs a high-performance current-mode pulse-width modulation (PWM) control scheme to provide tight output-voltage regulation and low subharmonic noise. The fixed-frequency oscillator is factory-trimmed to 160kHz, allowing for easy noise filtering. The regulator is production tested in an actual application circuit, and output accuracy is guaranteed to within ±5% over all specified conditions of line, load, and temperature.

The input-to-output differential of the MAX755 is limited to $V_{IN} + |V_{OUT}| \leq 11.5V$.

For a similar device with wider input voltage range, refer to the MAX759 data sheet. For fixed -5V parts, refer to the MAX735 and MAX739 data sheets. For fixed -12V and -15V versions, see the MAX736/MAX737 data sheet. For lower-power applications, refer to the MAX635/MAX636/MAX637 data sheet.

Applications

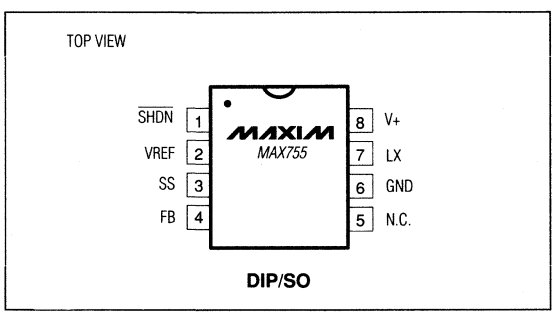
Negative LCD Driver

Board-Level DC-DC Conversion

Battery-Powered Equipment

Computer Peripherals

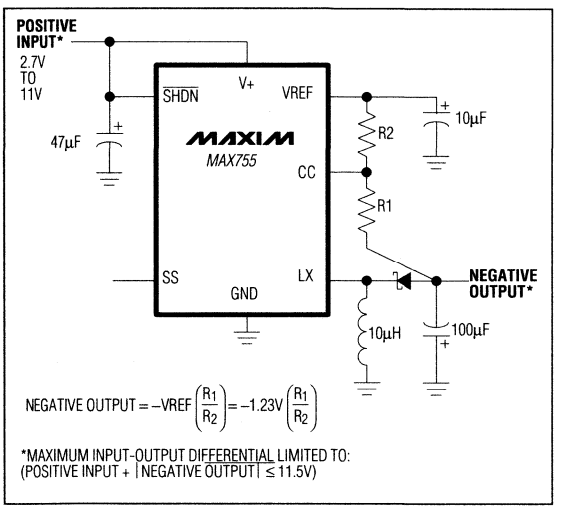
Pin Configuration



Features

- ♦ **Converts +2.7V to +11V Input to Adjustable Negative Output (MAX755)**
- ♦ **1W Guaranteed Output Power ($V_{IN} \geq 4.5V$)**
- ♦ **78% Typical Efficiency**
- ♦ **1.6mA Quiescent Current**
- ♦ **10µA Shutdown Mode**
- ♦ **160kHz Fixed-Frequency Oscillator**
- ♦ **Current-Mode PWM – Low Noise and Jitter**
- ♦ **Soft-Start**
- ♦ **Simple Application Circuit**

Typical Operating Circuit



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

Switched-Capacitor Voltage Converters

General Description

The MAX1044 and ICL7660 are monolithic, CMOS switched-capacitor voltage converters that invert, double, divide, or multiply input voltage. They are pin compatible with the industry-standard ICL7660. Operation is guaranteed to 10V with no external diode over the full temperature range. The MAX1044 has a BOOST pin that raises the oscillator frequency above the audio band and also reduces external capacitor size.

The MAX1044/ICL7660 combine low quiescent current with high efficiency. Oscillator control circuitry and four power MOS switches are included on-chip. Applications include generating a -5V supply from a +5V logic supply to power analog circuitry. When used as doublers, these devices generate 6V from a single 3V lithium cell, or 3V from a single 1.5V alkaline cell. For applications requiring more power, the MAX660 can deliver up to 100mA with a voltage drop of less than 0.65V.

Applications

-5V Supply from +5V Logic Supply

Personal Communication Equipment

Op-Amp Power Supplies

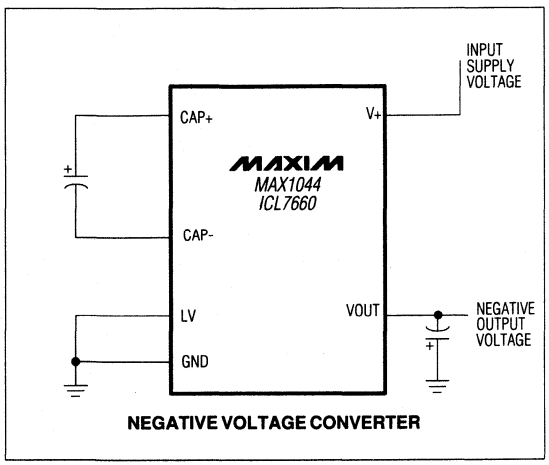
EIA/TIA-232E and EIA/TIA-562 Power Supplies

Data-Acquisition Systems

Hand-Held Instruments

Panel Meters

Typical Operating Circuit



NEGATIVE VOLTAGE CONVERTER

Features

- ♦ **1.5V to 10.0V Operating Supply Voltage Range**
- ♦ **95% Min Power-Conversion Efficiency**
- ♦ **Invert, Double, Divide, or Multiply Input Voltage**
- ♦ **BOOST Pin Increases Switching Frequencies (MAX1044)**
- ♦ **No-Load Supply Current - 200μA Max at 5V**
- ♦ **No External Diode Required for Higher Voltage Operation**

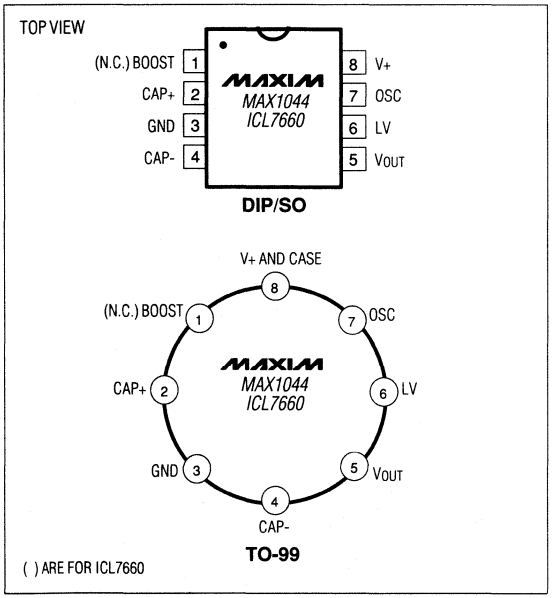
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1044CPA	0°C to +70°C	8 Plastic DIP
MAX1044CSA	0°C to +70°C	8 SO
MAX1044CTV	0°C to +70°C	8 TO-99
MAX1044C/D	0°C to +70°C	Dice*
MAX1044EPA	-40°C to +85°C	8 Plastic DIP
MAX1044ESA	-40°C to +85°C	8 SO
MAX1044ETV	-40°C to +85°C	8 TO-99

Ordering Information continued on last page.

** Contact factory for dice specifications.*

Pin Configurations



Switched-Capacitor Voltage Converters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to GND, or GND to V_{OUT}) 10.5V
Input Voltage on Pins 1, 6, and 7
(Note 1) ..... $-0.3V \le V_{IN} \le (V+ + 0.3V)$
LV Input Current (Note 1) 20µA
Output Short-Circuit Duration (V+ ≤ 5.5V) ..... Continuous
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW
TO-99 (derate 6.67mW/°C above +70°C) 533mW
Operating Temperature Ranges:
MAX1044/ICL7660C_ _ ..... 0°C to +70°C
MAX1044/ICL7660E_ _ ..... -40°C to +85°C
MAX1044/ICL7660M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: Connecting any input terminal to voltages greater than V+ or less than ground may cause latchup. Do not apply any inputs from sources operating from external supplies before device power-up.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V+ = 5.0V, LV pin = 0V, I_{LOAD} = 0mA, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MAX1044			ICL7660			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	$R_L = \infty$, pins 1 and 7 no connection, LV open	T_A = +25°C		30	200		110	175	µA
		T_A = 0°C to +70°C			200			225	
		T_A = -40°C to +85°C			200			250	
		T_A = -55°C to +125°C			200			250	
	$R_L = \infty$, pins 1 and 7 = V+ = 3V			10					
Supply Voltage Range (Note 1)	R_L = 10kΩ, LV open					3.0		10.0	V
	R_L = 10kΩ, LV to GND		1.5		10	1.5		3.5	
Output Resistance	I_L = 20mA, f_{OSC} = 5kHz, LV open	T_A = +25°C		65	100		55	100	Ω
		0°C to +70°C			130			120	
		-40°C to +85°C			130			140	
		-55°C to +125°C (Note 2)			150			150	
	f_{OSC} = 27kHz (ICL7660), f_{OSC} = 1kHz (MAX1044), V+ = 2V, I_L = 3mA, LV to GND	T_A = +25°C			325			250	
		T_A = 0°C to +70°C			325			300	
		T_A = -40°C to +85°C			325			300	
		T_A = -55°C to +125°C			400			400	
Oscillator Frequency	C_{OSC} = 1pF, LV to GND (Note 3)	V+ = 5V	5				10		kHz
		V+ = 2V	1						
Power Efficiency	R_L = 5kΩ, T_A = +25°C, f_{OSC} = 5kHz, LV open		95	98		95	98		%
Voltage Conversion Efficiency	$R_L = \infty$, T_A = +25°C, LV open		97.0	99.9		99.0	99.9		%
Oscillator Sink or Source Current	V_{OSC} = 0V or V+, LV open	Pin 1 = 0V			3				µA
		Pin 1 = V+			20				
Oscillator Impedance	T_A = +25°C	V+ = 2V		1.0			1.0		MΩ
		V+ = 5V		100			100		kΩ

Note 1: The Maxim ICL7660 and MAX1044 can operate without an external output diode over the full temperature and voltage ranges. The Maxim ICL7660 can also be used with the external output diode D_X when replacing the Intersil ICL7660. Tests performed with DX out of circuit.
Note 2: Maxim ICL7660A and MAX1044 only.
Note 3: f_{OSC} is tested with C_{OSC} = 100pF to minimize the effects of test fixture capacitance loading. The 1pF frequency is correlated to this 100pF test point, and is intended to simulate pin 7's capacitance when the device is plugged into a test socket with no external capacitor. For this test, the LV pin is connected to GND for comparison to the original manufacturer's device, which automatically connects this pin to GND for (V+ + 3V).

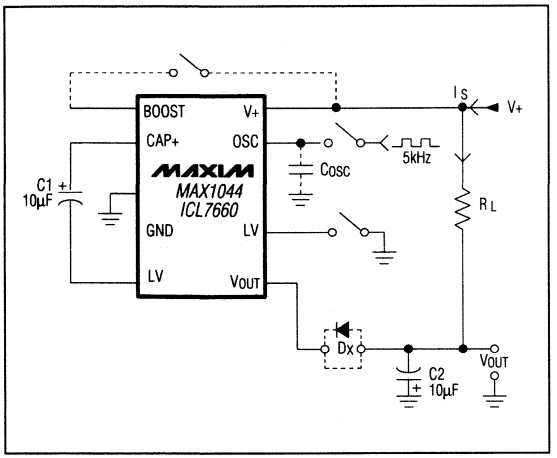


Figure 1. Maxim ICL7660 and MAX1044 Test Circuit (C_1 and C_2 should be increased to 100µF if C_{OSC} exceeds 10pF). Note: D_X not required with Maxim ICL7660 or MAX1044.

_ Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX1044MJA	-55°C to +125°C	8 CERDIP**
MAX1044MTV	-55°C to +125°C	8 TO-99**
ICL7660CPA	0°C to +70°C	8 Plastic DIP
ICL7660CSA	0°C to +70°C	8 SO
ICL7660CTV	0°C to +70°C	8 TO-99
ICL7660C/D	0°C to +70°C	Dice*
ICL7660IPA	-20°C to +85°C	8 Plastic DIP
ICL7660ISA	-20°C to +85°C	8 SO
ICL7660IJA	-20°C to +85°C	8 CERDIP
ICL7660ITV	-20°C to +85°C	8 TO-99
ICL7660EPA	-40°C to +85°C	8 Plastic DIP
ICL7660ESA	-40°C to +85°C	8 SO
ICL7660EJA	-40°C to +85°C	8 CERDIP
ICL7660MTV	Order ICL7660AMTV	
ICL7660AMJA	-55°C to +125°C	8 CERDIP**
ICL7660AMTV	-55°C to +125°C	8 TO-99**

** Contact factory for dice specifications.*

***Contact factory for availability and processing to MIL-STD-883.*

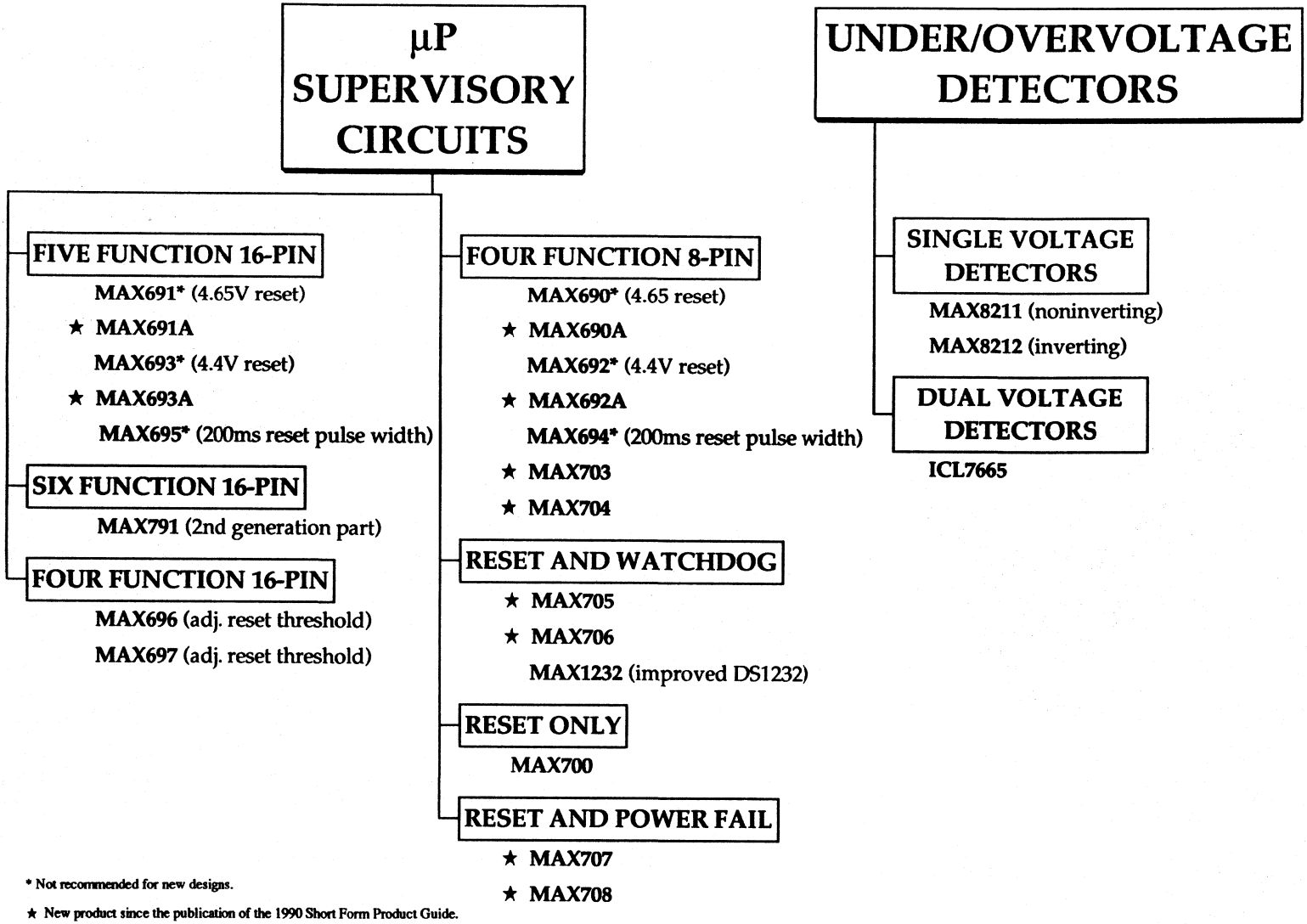
µP Supervisory Circuits

5

* Advance Information – first page of data sheet in preparation.

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ Write Protect	Power-Fail Comparator	Manual Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Battery-On Output	Price† 1000-up ($)
MAX690	4.65	35	1.6	✔		✔						3.27
MAX690A	4.65	140	1.6	✔		✔						3.33
MAX691	4.65	35/adj.	1.6/adj.	✔	✔	✔		✔	✔	✔	✔	3.55
MAX691A	4.65	140/adj.	1.6/adj.	✔	✔	✔		✔	✔	✔	✔	3.55
MAX692	4.40	35	1.6	✔		✔						3.27
MAX692A	4.40	140	1.6	✔		✔						3.33
MAX693	4.40	35/adj.	1.6/adj.	✔	✔	✔		✔	✔	✔	✔	3.55
MAX693A	4.40	140/adj.	1.6/adj.	✔	✔	✔		✔	✔	✔	✔	3.61
MAX694	4.65	140	1.6	✔		✔						3.27
MAX695	4.65	140/adj.	1.6/adj.	✔	✔	✔		✔	✔	✔	✔	3.55
MAX696	Adj.	35/adj	1.6/adj.	✔		✔		✔	✔	✔	✔	3.55
MAX697	Adj.	35/adj.	1.6/adj.		✔	✔		✔	✔	✔		3.58
MAX700	4.65/adj.	200	-				✔			✔		2.17
MAX703	4.65	140	-	✔		✔	✔					1.38
MAX704	4.40	140	-	✔		✔	✔					1.38
MAX705	4.65	140	1.6			✔	✔	✔				1.02*
MAX706	4.40	140	1.6			✔	✔	✔				1.02*
MAX707	4.65	140	-			✔	✔			✔		0.88*
MAX708	4.40	140	-			✔	✔			✔		0.88*
MAX791	4.65	140	1	✔	✔	✔	✔	✔	✔	✔	✔	††
MAX1232	4.50/4.75	250	0.15/0.60/1.2				✔			✔		1.71
MAX1259	-	-	-	✔		✔						3.74

* 25,000 pc. price, factory direct
† Prices provided are for design guidance and are FOB USA (unless otherwise noted). International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.



* Not recommended for new designs.

★ New product since the publication of the 1990 Short Form Product Guide.

19-4333; Rev 0; 4/92

MAXIM

Microprocessor Supervisory Circuits

General Description

The MAX690A/MAX692A reduce the complexity and number of components required for power-supply monitoring and battery-control functions in microprocessor (µP) systems. They significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX690A/MAX692A provide four functions:

1. A reset output during power-up, power-down, and brownout condtions.
2. Battery-backup switching for CMOS RAM, CMOS µP, or other low-power logic.
3. A reset pulse if the optional watchdog timer has not been toggled within 1.6sec.
4. A 1.25V threshold detector for power-fail warning or low-battery detection, or to monitor a power supply other than +5V.

The MAX690A and MAX692A differ only in their reset voltage threshold levels. The MAX690A generates a reset pulse when the supply voltage drops below 4.65V, and the MAX692A generates a reset below 4.40V.

Both parts are available in 8-pin DIP and SO packages. The MAX690A is pin compatible with the MAX690 and MAX694. The MAX692A is pin compatible with the MAX692.

Applications

Battery-Powered Computers and Controllers

Intelligent Instruments

Automotive Systems

Critical µP Power Monitoring

Features

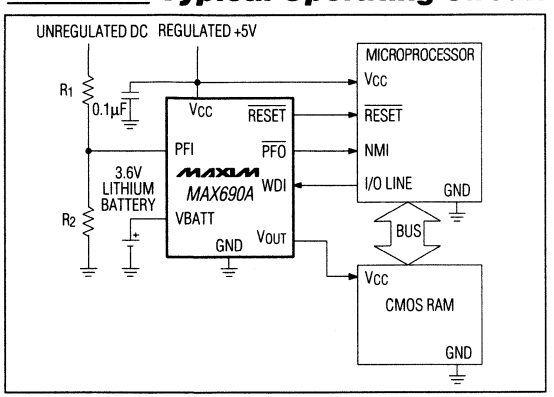
- ♦ **Precision Supply-Voltage Monitor:**
  4.65V for MAX690A
  4.40V for MAX692A
- ♦ **Reset Time Delay - 200ms**
- ♦ **Watchdog Timer - 1.6sec Timeout**
- ♦ **Battery-Backup Power Switching**
- ♦ **200µA Quiescent Supply Current**
- ♦ **50nA Quiescent Supply Current in Battery Backup Mode**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **8-Pin SO and DIP Packages**
- ♦ **Guaranteed $\overline{\text{RESET}}$ Assertion to V_{CC} = 1V**

Ordering Information

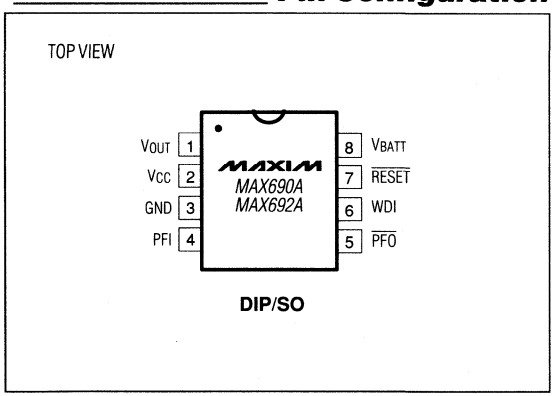
PART	TEMP. RANGE	PIN-PACKAGE
MAX690ACPA	0°C to +70°C	8 Plastic DIP
MAX690ACSA	0°C to +70°C	8 SO
MAX690AC/D	0°C to +70°C	Dice*
MAX690AEPA	-40°C to +85°C	8 Plastic DIP
MAX690AESA	-40°C to +85°C	8 SO
MAX690AMJA	-55°C to +125°C	8 CERDIP**
MAX692ACPA	0°C to +70°C	8 Plastic DIP
MAX692ACSA	0°C to +70°C	8 SO
MAX692AC/D	0°C to +70°C	Dice*
MAX692AEPA	-40°C to +85°C	8 Plastic DIP
MAX692AESA	-40°C to +85°C	8 SO
MAX692AMJA	-55°C to +125°C	8 CERDIP**

** Dice are tested at T_A = +25°C only.*
***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



Pin Configuration



5

Microprocessor Supervisory Circuits

ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- V_{BATT} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} 200mA
- V_{BATT} 50mA
- GND 20mA

Output Current
- V_{OUT} ..... Short-Circuit Protected for up to 10sec
- All Other Outputs 20mA

Rate of Rise, V_{CC}, V_{BATT} 100V/µs

Continuous Power Dissipation
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX69_AC__ ..... 0°C to +70°C
- MAX69_AE__ ..... -40°C to +85°C
- MAX69_AMJA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The input voltage limits on PFI and WDI may be exceeded provided the current into these pins is limited to less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.5V, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range, V_{CC}, V_{BATT} (Note 2)		MAX69_AC		1.0		5.5	V
		MAX69_AE/AM		1.2		5.5	
Supply Current (Excluding I_{OUT})	I_{SUPPLY}	MAX69_AC			200	350	µA
		MAX69_AE/AM			200	500	
I_{SUPPLY} in Battery-Backup Mode (Excluding I_{OUT})		V_{CC} = 0V, V_{BATT} = 2.8V	T_A = +25°C		0.05	1.0	µA
			T_A = T_{MIN} to T_{MAX}			5.0	
V_{BATT} Standby Current (Note 3)		5.5V > V_{CC} > V_{BATT} +0.2V	TA = +25°C	-0.1		+0.02	µA
			T_A = T_{MIN} to T_{MAX}	-1.0		+0.02	
V_{OUT} Output		I_{OUT} = 5mA		V_{CC} - 0.05	V_{CC} - 0.025		V
		I_{OUT} = 50mA		V_{CC} - 0.5	V_{CC} - 0.25		
V_{OUT} in Battery-Backup Mode		I_{OUT} = 250µA, V_{CC} < V_{BATT} - 0.2V		V_{BATT} - 0.1	V_{BATT} - 0.02		V
Battery Switch Threshold, V_{CC} to V_{BATT}		VCC < V_{RT}	Power-up		20		mV
			Power-down		-20		
Battery Switchover Hysteresis					40		mV
$\overline{RESET}$ Threshold	V_{RT}	MAX690A		4.50	4.65	4.75	V
		MAX692A		4.25	4.40	4.50	
$\overline{RESET}$ Threshold Hysteresis					40		mV
$\overline{RESET}$ Pulse Width	t_{RS}			140	200	280	ms
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800µA		V_{CC} - 1.5			V
		I_{SINK} = 3.2mA				0.4	
		MAX69_AC; V_{CC} = 1.0V, I_{SINK} = 50µA				0.3	
		MAX69_AE/AM; V_{CC} = 1.2V, I_{SINK} = 100µA				0.3	

ELECTRICAL CHARACTERISTICS (continued)

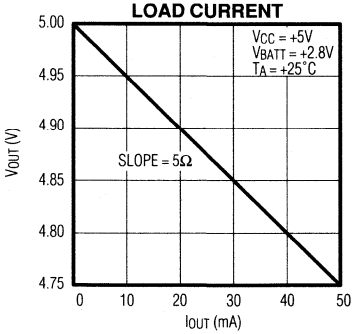
(V_{CC} = +4.75V to +5.5V, V_{BATT} = 2.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Watchdog Timeout	t_{WD}			1.00	1.60	2.25	sec
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = (0.8) (V_{CC})		50			ns
WDI Input Threshold (Note 4)		V_{CC} = 5V	Logic Low			0.8	V
			Logic High	3.5			
WDI Input Current		WDI = V_{CC}			50	150	µA
		WDI = 0V		-150	-50		
PFI Input Threshold		V_{CC} = 5V		1.20	1.25	1.30	V
PFI Input Current				-25	0.01	25	nA
$\overline{PFO}$ Output Voltage		I_{SOURCE} = 800µA		V_{CC} - 1.5			V
		I_{SINK} = 3.2mA				0.4	

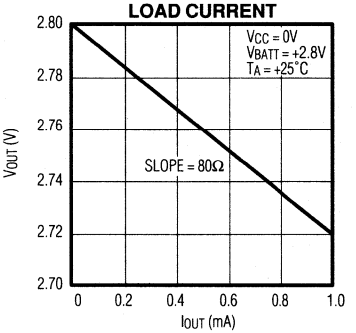
Note 2: Either V_{CC} or V_{BATT} can go to 0V, if the other is greater than 2.0V.
Note 3: "+" = battery-charging current, "-" = battery-discharging current.
Note 4: WDI is guaranteed to be in an intermediate, non-logic level state if WDI is floating and V_{CC} is in the operating voltage range. WDI is internally biased to 35% of V_{CC} with an input impedance of 50kΩ.

Typical Operating Characteristics

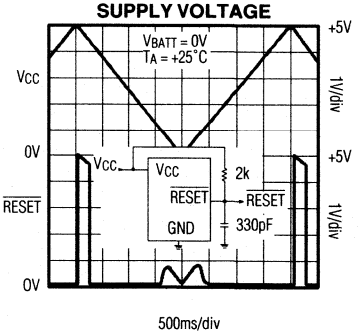
OUTPUT VOLTAGE vs. LOAD CURRENT



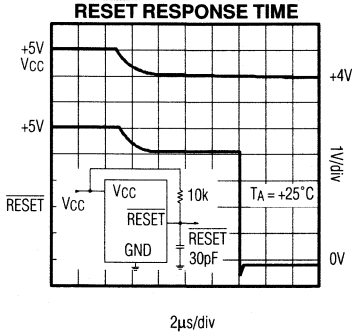
OUTPUT VOLTAGE vs. LOAD CURRENT



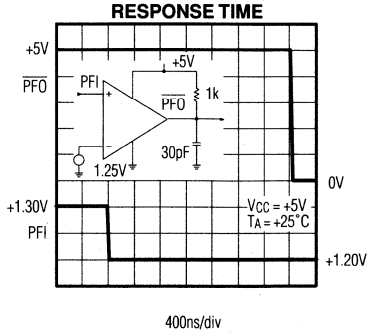
MAX690A RESET OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



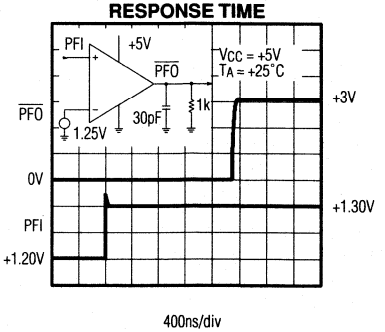
MAX690A RESET RESPONSE TIME



POWER-FAIL COMPARATOR RESPONSE TIME



POWER-FAIL COMPARATOR RESPONSE TIME



Microprocessor Supervisory Circuits

Pin Description

PIN	NAME	FUNCTION
1	V_{OUT}	Supply Output for CMOS RAM. When V_{CC} is above the reset threhold, V_{OUT} connects to V_{CC} through a P-channel MOSFET switch. When V_{CC} is below the reset threshold, the higher of V_{CC} or V_{BATT} will be connected to V_{OUT}.
2	V_{CC}	+5V Supply Input
3	GND	Ground
4	PFI	Power-Fail Comparator Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	$\overline{PFO}$	Power-Fail Output. When PFI is less than 1.25V, $\overline{PFO}$ goes low; otherwise $\overline{PFO}$ stays high.
6	WDI	Watchdog Input. If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and $\overline{RESET}$ is triggered. If WDI is left floating or connected to a high-impedance three-state buffer, the watchdog feature is disabled. The internal watchdog timer clears whenever $\overline{RESET}$ is low, WDI is three-stated, or WDI sees a rising or falling edge.
7	$\overline{RESET}$	Reset Output. Whenever $\overline{RESET}$ is triggered, it pulses low for 200ms. It stays low when V_{CC} is below the reset threshold (4.65V in the MAX690A and 4.4V in the MAX692A) and remains low for 200ms after V_{CC} rises above the reset threshold. A watchdog timeout also triggers $\overline{RESET}$.
8	V_{BATT}	Backup-Battery Input. When V_{CC} falls below the reset threshold, V_{BATT} will be switched to V_{OUT} if V_{BATT} is 20mV greater than V_{CC}. When V_{CC} rises to 20mV above V_{BATT}, V_{OUT} will be reconnected to V_{CC}. The 40mV hysteresis prevents repeated switching if V_{CC} falls slowly.

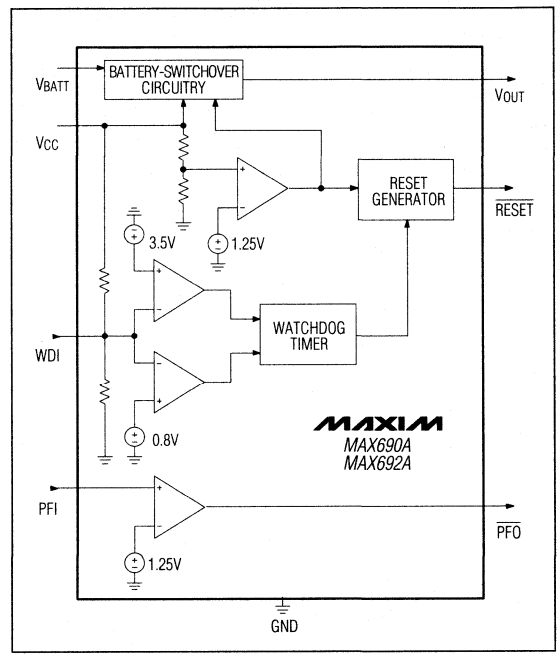


Figure 1. Block Diagram

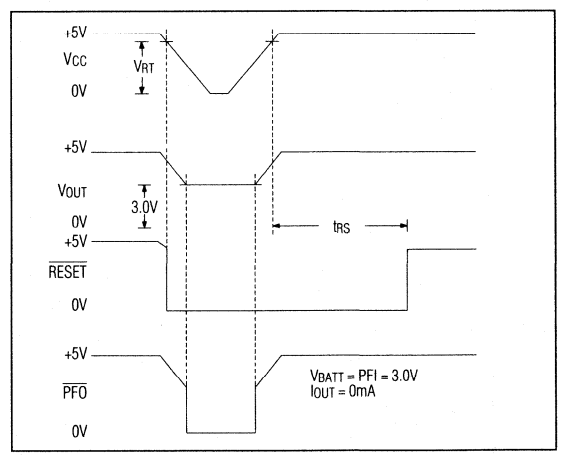


Figure 2. Timing Diagram

Detailed Description

RESET Output

A microprocessor's (µP's) reset input starts the µP in a known state. When the µP is in an unknown state, it should be held in reset. The MAX690A/MAX692A's $\overline{RESET}$ output ensures that the µP powers up at a known state, and prevents code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is guaranteed to be a logic low. As V_{CC} rises, $\overline{RESET}$ remains low. When V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for a time equal to the reset pulse width; after this interval, $\overline{RESET}$ goes high (Figure 2). If a brownout condition occurs (if V_{CC} dips below the reset threshold), $\overline{RESET}$ is triggered. Each time $\overline{RESET}$ is triggered, it stays low for the reset pulse width interval. Any time V_{CC} goes below the reset threshold, the internal timer restarts the pulse. If a brownout condition interrupts a

previously initiated reset pulse, the reset pulse continues for another 200ms. On power-down, once V_{CC} goes below the threshold, $\overline{RESET}$ is guaranteed to be logic low until V_{CC} droops below 1V.

$\overline{RESET}$ is also triggered by a watchdog timeout. If a high or low is continuously applied to the WDI pin for 1.6sec, $\overline{RESET}$ pulses low. As long as $\overline{RESET}$ is asserted, the watchdog timer remains clear. When $\overline{RESET}$ comes high, the watchdog resumes timing and must be serviced within 1.6sec. If WDI is tied high or low, a $\overline{RESET}$ pulse is triggered every 1.8sec (t_{WD} plus t_{RS}).

Watchdog Input

The watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec, a $\overline{RESET}$ pulse is triggered. The internal 1.6sec timer is cleared by either a $\overline{RESET}$ pulse or by open circuiting the WDI input. As long as $\overline{RESET}$ is asserted or the WDI input is open circuited, the timer remains cleared and does not count. As soon as $\overline{RESET}$ is released or WDI is driven high or low, the timer starts counting. It can detect pulses as short as 50ns.

Power-Fail Comparator

The PFI input is compared to an internal 1.25V reference. If PFI is less than 1.25V, $\overline{PFO}$ goes low. The power-fail comparator is intended for use as an undervoltage detector to signal a failing power supply; it need not be dedicated to this function though, as it is completely separate from the rest of the MAX690A/MAX692A circuitry. The external voltage divider drives PFI to sense the unregulated DC input to the +5V regulator (see *Typical Operating Circuit*). The voltage-divider ratio can be chosen such that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. $\overline{PFO}$ then triggers an interrupt which signals the µP to prepare for power-down.

To conserve backup-battery power, the power-fail detector comparator is turned off and $\overline{PFO}$ is forced low when V_{BATT} connects to V_{CC}.

Backup-Battery Switchover

In the event of a brownout or power failure, it may be necessary to preserve the contents of RAM. With a backup battery installed at V_{BATT}, the MAX690A/MAX692A automatically switch RAM to backup power when V_{CC} fails.

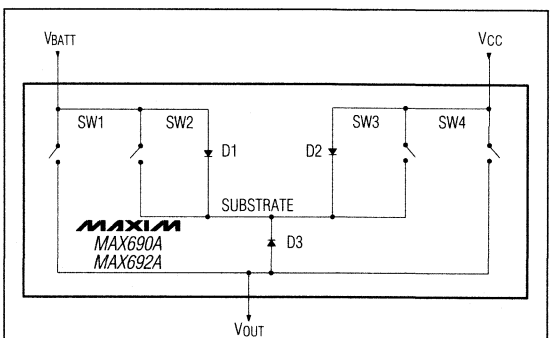
As long as V_{CC} exceeds the reset threshold, V_{OUT} connects to V_{CC} through a 5Ω PMOS power switch. Once V_{CC} falls below the reset threshold, V_{CC} or V_{BATT} (whichever is higher) switches to V_{OUT}. Unlike the MAX690/MAX692, the MAX690A/MAX692A don't always connect V_{BATT} to V_{OUT} when V_{BATT} is greater than V_{CC}. V_{BATT} connects to V_{CC} (through an 80Ω switch) only when V_{CC} is below the reset threshold **AND** V_{BATT} is greater than V_{CC}.

When V_{CC} exceeds the reset threshold, it is connected to the MAX690A/MAX692A substrate, regardless of the voltage applied to V_{BATT} (Figure 3). During this time, the diode (D1) between V_{BATT} and the substrate will conduct current from V_{BATT} to V_{CC} if V_{BATT} is 0.6V or greater than V_{CC}.

When V_{BATT} connects to V_{OUT}, backup mode is activated and the internal circuitry is powered from the battery (Table 1). When V_{CC} is just below V_{BATT}, the current drawn from V_{BATT} is typically 30µA. When V_{CC} drops to more than 1V below V_{BATT}, the internal switchover comparator shuts off and the supply current falls to less than 1µA.

Table 1. Input and Output Status in Battery-Backup Mode

SIGNAL	STATUS
V_{CC}	Disconnected from V_{OUT}.
V_{OUT}	Connected to V_{BATT} through an internal 80Ω PMOS switch.
V_{BATT}	Connected to V_{OUT}. Current drawn from the battery is less than 1µA as long as $V_{CC} < V_{BATT}$ - 1V.
PFI	Power-fail comparator is disabled.
$\overline{PFO}$	Logic low
$\overline{RESET}$	Logic low
WDI	Watchdog timer is disabled.



CONDITION	SW1/SW2	SW3/SW4
V_{CC} > Reset Threshold	Open	Closed
V_{CC} < Reset Threshold and $V_{CC} > V_{BATT}$	Open	Closed
V_{CC} < Reset Threshold and $V_{CC} < V_{BATT}$	Closed	Open

RESET THRESHOLD = 4.65V IN MAX690A; RESET THRESHOLD = 4.4V IN MAX692A.

Figure 3. Backup-Battery Switchover Block Diagram

Applications Information

Using a SuperCap™ as a Backup Power Source

SuperCaps are capacitors with extremely high capacitance values, on the order of 0.1F. Figure 4 shows a SuperCap used as a backup power source. Do not allow the SuperCap's voltage to exceed the maximum reset threshold by more than 0.6V. In Figure 4's circuit, the SuperCap rapidly charges to within a diode drop of VCC. However, after a long time, the diode leakage current will pull the SuperCap voltage up to VCC. When using a SuperCap with the MAX690A, VCC may not exceed 4.75V + 0.6V = 5.35V.

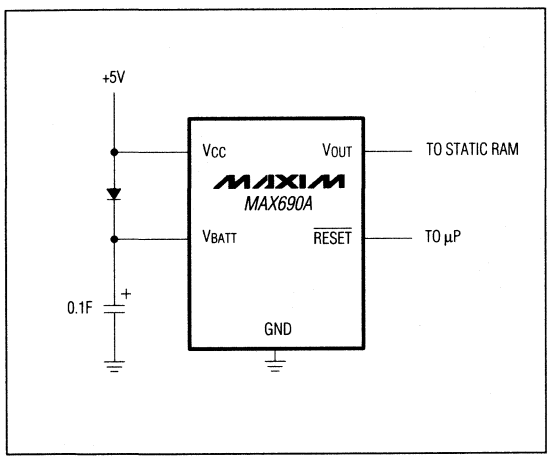


Figure 4. Using a SuperCap as a Backup Power Source with a MAX690A and a +5V ±5% Supply

Use the SuperCap circuit of Figure 5 with a MAX692A and a ±10% supply. This circuit ensures that the SuperCap only charges to VCC - 0.5V. At the maximum VCC of 5.5V, the SuperCap charges up to 5.0V, only 0.5V above the maximum reset threshold—well within the requisite 0.6V.

Allowable Backup Power-Source Batteries

Lithium batteries work very well as backup batteries due to very low self-discharge rates and high energy density. Single lithium batteries with open-circuit voltages of 3.0V to 3.6V are ideal. Any battery with an open-circuit voltage less than the minimum reset threshold plus 0.3V can be connected directly to the VBATT input of the MAX690A/MAX692A with no additional circuitry (see the

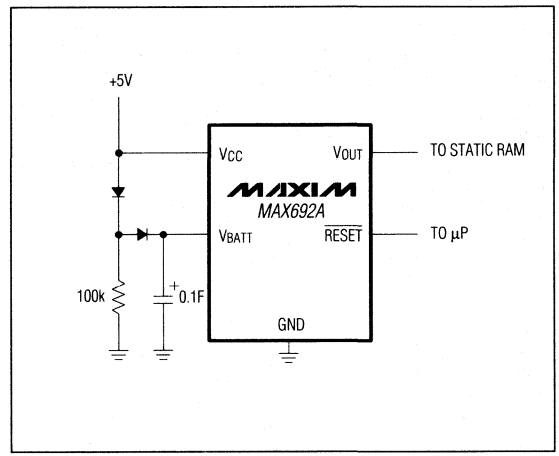


Figure 5. Using a SuperCap™ as a Backup Power Source with the MAX692A and a +5V ±10% Supply

Typical Operating Circuit). However, batteries with open-circuit voltages that are greater CANNOT be used for backup, as current is sourced into the substrate through the diode (D1 in Figure 3) when VCC is close to the reset threshold.

Table 2. Allowable Backup-Battery Voltages
(see *Using a SuperCap as a Backup Power Source* section for use with a SuperCap)

PART NO.	MAXIMUM BACKUP-BATTERY VOLTAGE (V)
MAX690A	4.80
MAX692A	4.55

Using the MAX690A/MAX692A Without a Backup Power Source

If a backup power source is not used, ground VBATT and connect VOUT to VCC. Since there is no need to switch over to any backup power source, VOUT does not need to be switched. A direct connection to VCC eliminates any voltage drops across the switch which may push VOUT below VCC.

Replacing the Backup Battery

The backup battery can be removed while VCC remains valid, without danger of triggering RESET. As long as VCC stays above the reset threshold, battery-backup mode cannot be entered. In other switchover ICs where battery-backup mode is entered whenever VBATT gets close to VCC, an unconnected VBATT pin accumulates leakage charge and triggers RESET in error.

SuperCap™ is a trademark of Baknor Industries.

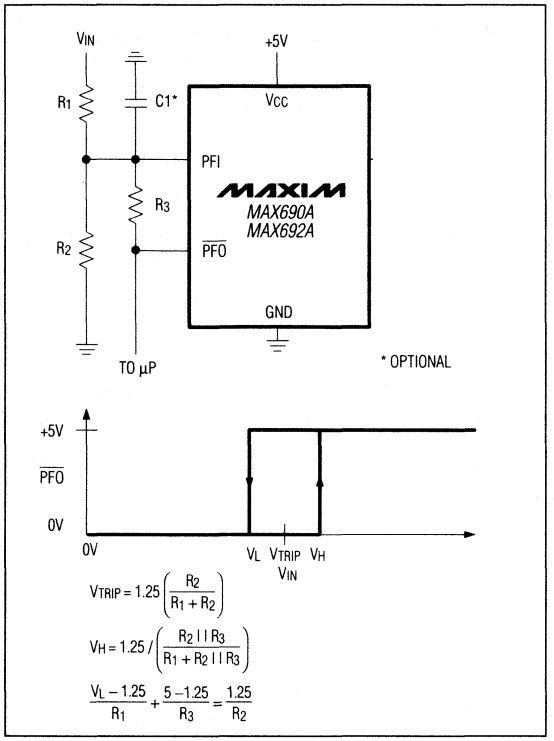


Figure 6. Adding Hysteresis to the Power-Fail Comparator

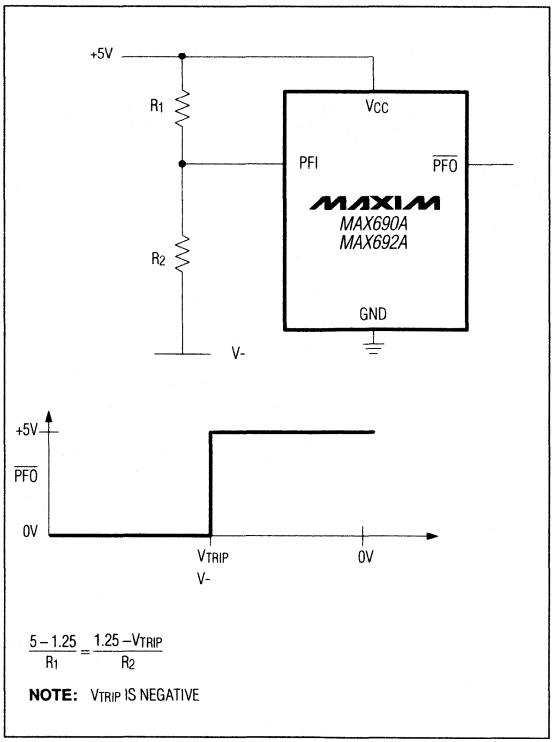


Figure 7. Monitoring a Negative Voltage

Adding Hysteresis to the Power-Fail Comparator

Hysteresis adds a noise margin to the power-fail comparator and prevents repeated triggering of PFO when V_{IN} is close to its trip point. Figure 6 shows how to add hysteresis to the power-fail comparator. Select the ratio of R_1 and R_2 such that PFI sees 1.25V when V_{IN} falls to its trip point (V_{TRIP}). R_3 adds the hysteresis. It will typically be an order of magnitude greater than R_1 or R_2 (about 10 times either R_1 or R_2). The current through R_1 and R_2 should be at least 1µA to ensure that the 25nA (max) PFI input current does not shift the trip point. R_3 should be larger than 10kΩ so it does not load down the $\overline{PFO}$ pin. Capacitor C1 adds additional noise rejection.

Monitoring a Negative Voltage

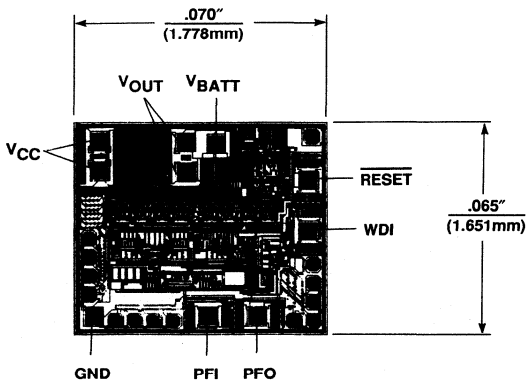
The power-fail comparator can be used to monitor a negative supply rail using the circuit of Figure 7. When the negative rail is good (a negative voltage of large magnitude), $\overline{PFO}$ is low. When the negative rail is degraded (a negative voltage of lesser magnitude), $\overline{PFO}$ goes high. This circuit's accuracy is affected by the PFI threshold tolerance, the V_{CC} line, and the resistors.

Microprocessor Supervisory Circuits

Maxim µP Supervisory Products

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	$\overline{CE}$ Write Protect	Power-Fail Comparator	Manual Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Batt On Output	Pins
MAX690A	4.65	140	1.6	yes	no	yes	no	no	no	no	no	8 DIP, SO
MAX691A	4.65	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes	16 DIP, SO
MAX692A	4.40	140	1.6	yes	no	yes	no	no	no	no	no	8 DIP, SO
MAX693A	4.40	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes	16 DIP, SO
MAX696	adj.	35/adj.	1.6/adj.	yes	no	yes	no	yes	yes	yes	yes	16 DIP, SO
MAX697	adj.	35/adj.	1.6/adj.	no	yes	yes	no	yes	yes	yes	no	16 DIP, SO
MAX700	4.65/adj.	200	NA	no	no	no	yes	yes	no	yes	no	8 DIP, SO
MAX703	4.65	140	NA	yes	no	yes	yes	no	no	no	no	8 DIP, SO
MAX704	4.40	140	NA	yes	no	yes	yes	no	no	no	no	8 DIP, SO
MAX705	4.65	140	1.6	no	no	yes	yes	yes	no	no	no	8 DIP, SO
MAX706	4.40	140	1.6	no	no	yes	yes	yes	no	no	no	8 DIP, SO
MAX707	4.65	140	NA	no	no	yes	yes	no	no	yes	no	8 DIP, SO
MAX708	4.40	140	NA	no	no	yes	yes	no	no	yes	no	8 DIP, SO
MAX1232	4.50/4.75	250	150/600/ 1200ms	no	no	no	yes	no	no	yes	no	8 DIP, SO

Chip Topography



SUBSTRATE MUST BE LEFT UNCONNECTED;
TRANSISTOR COUNT: 573.

MAX692A

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

Microprocessor Supervisory Circuits

General Description

The MAX691A/MAX693A microprocessor (µP) supervisors are pin-compatible upgrades to the MAX691, MAX693, and MAX695. The MAX691A/MAX693A improve performance with a 70µA supply current and 10ns chip-enable propagation delay. They feature write protection of CMOS RAM or EEPROM, separate watchdog outputs, backup-battery switchover, and $\overline{RESET}$ and RESET outputs that are valid with V_{CC} down to 1V. The MAX691A has a 4.65V typ reset threshold voltage, and the MAX693A's reset threshold is 4.40V typ.

Applications

Computers

Controllers

Intelligent Instruments

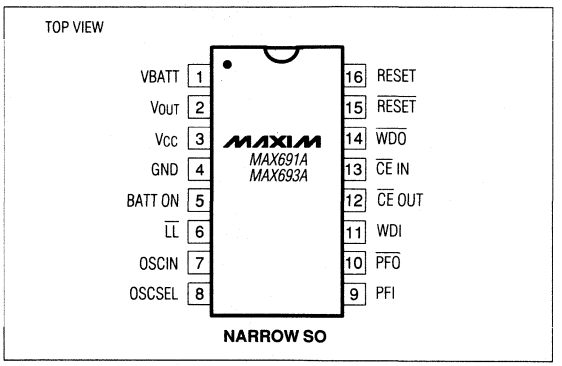
Automotive Systems

Critical µP Power Monitoring

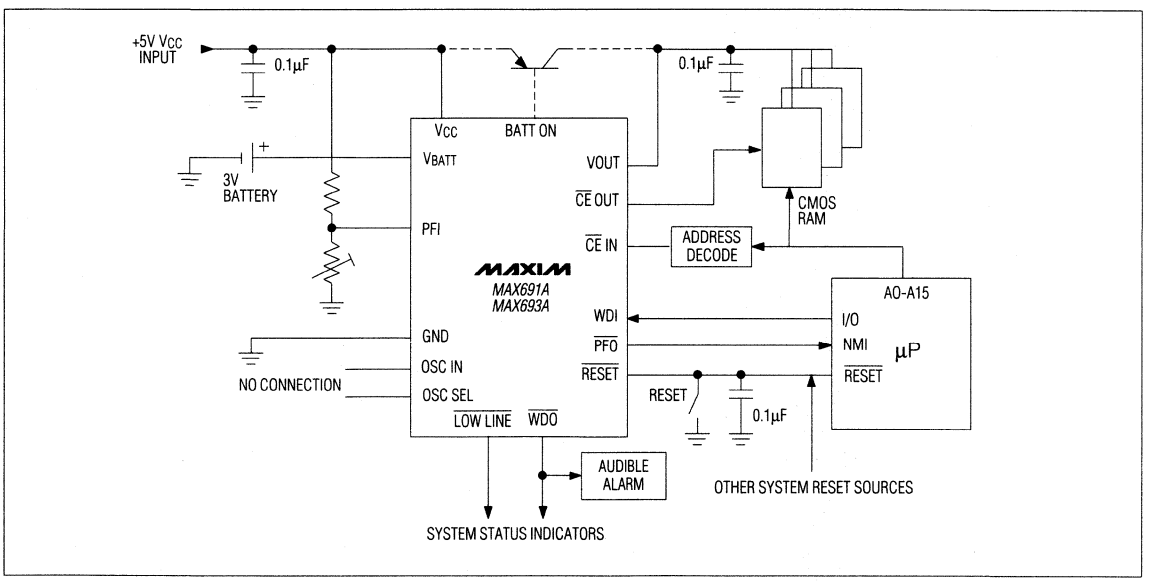
Features

- **200ms typ Power OK/Reset Time Delay**
- **Fixed 1.6sec or Adjustable Watchdog Timeout Period**
- **1µA Standby Current**
- **On-Board Gating of Chip-Enable Signals**
- **10ns Chip-Enable Gate Delay**
- **Max-Cap Compatible**
- **Reset Assertion to $V_{CC} \leq 1V$**
- **Voltage Monitor for Power-Fail or Low-Battery Warning**
- **Available in 16-pin Narrow SO and Plastic Dip Packages**

Pin Configuration



Typical Operating Circuit



5

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

Low-Cost, µP Supervisory Circuits

General Description

The MAX703/MAX704 microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in uP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX703/MAX704 provide four functions:

1) A reset output during power-up, power-down, and brownout condition,.
2) Battery-backup switchover,
3) Power-fail or battery monitoring,
4) An active-low manual reset input.

Two supply-voltage monitor levels are available: The MAX703 generates a reset pulse when the supply voltage drops below 4.65V, while the MAX704 generates a reset pulse below 4.40V. Both parts are available in 8-pin DIP and SO packages.

Features

- ♦ **Guaranteed $\overline{\text{RESET}}$ Valid at V_{CC} = 1V**
- ♦ **Precision Supply-Voltage Monitor**
  4.65V in MAX703
  4.40V in MAX704
- ♦ **200ms Reset Time Delay**
- ♦ **Debounced TTL-/CMOS-Compatible Manual Reset Input**
- ♦ **200µA Quiescent Current**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**
- ♦ **Battery-Backup switchover**

Applications

Computers

Controllers

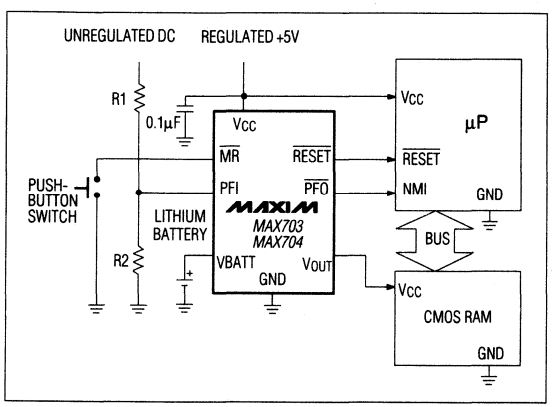
Intelligent Instruments

Automotive Systems

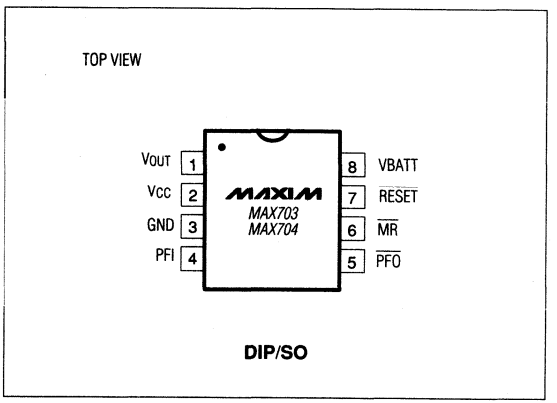
Critical µP Monitoring

5

Typical Operating Circuit



Pin Configuration



19-4334; Rev 1; 6/92

MAXIM

Low-Cost, µP Supervisory Circuits

General Description

The MAX705-MAX708 microprocessor (µP) supervisory circuits reduce the complexity and number of components required to monitor power-supply and battery functions in µP systems. These devices significantly improve system reliability and accuracy compared to separate ICs or discrete components.

The MAX705/MAX706 provide four functions:

1) A reset output during power-up, power-down, and brownout conditions.
2) An independent watchdog output that goes low if the watchdog input has not been toggled within 1.6 seconds.
3) A 1.25V threshold detector for power-fail warning, low-battery detection, or for monitoring a power supply other than +5V.
4) An active-low manual reset input.

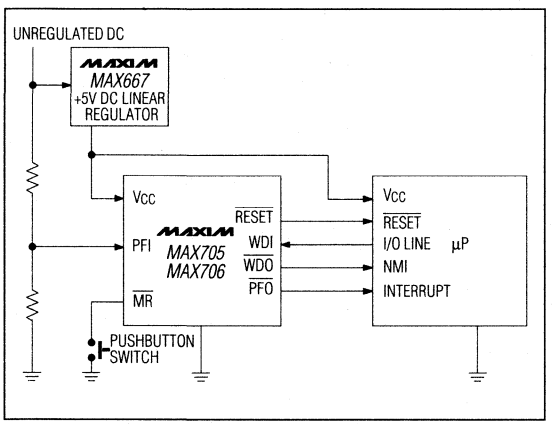
The MAX707/MAX708 are the same as the MAX705/MAX706, except an active-high reset is substituted for the watchdog timer.

Two supply-voltage monitor levels are available: The MAX705/MAX707 generate a reset pulse when the supply voltage drops below 4.65V, while the MAX706/MAX708 generate a reset pulse below 4.40V. All four parts are available in 8-pin DIP and SO packages.

Applications

Computers
Controllers
Intelligent Instruments
Automotive Systems
Critical µP Power Monitoring

Typical Operating Circuit



Features

- ♦ **Guaranteed $\overline{\text{RESET}}$ Valid at Vcc = 1V**
- ♦ **Precision Supply-Voltage Monitor**
  4.65V in MAX705/MAX707
  4.40V in MAX706/MAX708
- ♦ **200ms Reset Pulse Width**
- ♦ **Debounced TTL-/CMOS-Compatible Manual Reset Input**
- ♦ **Independent Watchdog Timer – 1.6sec Timeout (MAX705/MAX706)**
- ♦ **Active-High Reset Output (MAX707/MAX708)**
- ♦ **200µA Quiescent Current**
- ♦ **Voltage Monitor for Power-Fail or Low-Battery Warning**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX705CPA	0°C to +70°C	8 Plastic DIP
MAX705CSA	0°C to +70°C	8 SO
MAX705C/D	0°C to +70°C	Dice*
MAX705EPA	-40°C to +85°C	8 Plastic DIP
MAX705ESA	-40°C to +85°C	8 SO
MAX705MJA	-55°C to +125°C	8 CERDIP**

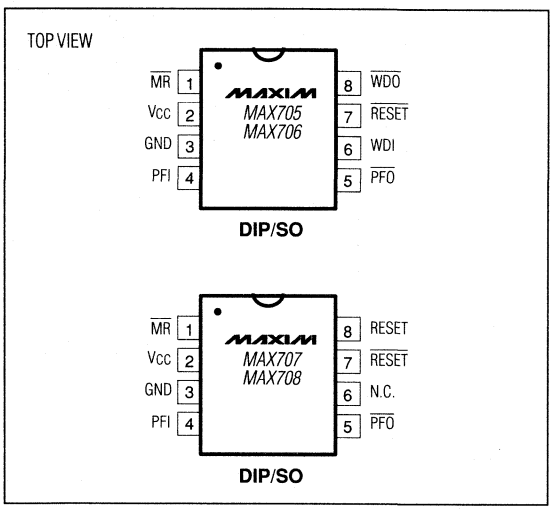
Ordering Information continued on last page.

** Dice are specified at T_A = +25°C.*

***Contact factory for availability and processing to MIL-STD-883.*

5

Pin Configurations



ABSOLUTE MAXIMUM RATINGS

Terminal Voltage (with respect to GND)
- V_{CC} ..... -0.3V to 6.0V
- All Other Inputs (Note 1) ..... -0.3V to (V_{CC} + 0.3V)

Input Current
- V_{CC} 20mA
- GND 20mA

Output Current (all outputs) 20mA

Continuous Power Dissipation
- Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
- SO (derate 5.88mW/°C above +70°C) 471mW
- CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
- MAX70_C__ ..... 0°C to +70°C
- MAX70_E__ ..... -40°C to +85°C
- MAX70_MJA ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +160°C

Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The input voltage limits on PFI and $\overline{MR}$ can be exceeded if the input current is less than 10mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	MAX70_C	1.0		5.5	V
		MAX70_E/M	1.2		5.5	
Supply Current	I_{SUPPLY}	MAX70_C		200	350	µA
		MAX70_E/M		200	500	
Reset Threshold (Note 2)	V_{RT}	MAX705/MAX707	4.50	4.65	4.75	V
		MAX706/MAX708	4.25	4.40	4.50	
Reset Threshold Hysteresis (Note 2)				40		mV
Reset Pulse Width (Note 2)	t_{RS}		140	200	280	ms
$\overline{RESET}$ Output Voltage		I_{SOURCE} = 800µA	V_{CC} - 1.5			V
		I_{SINK} = 3.2mA			0.4	
		MAX70_C, V_{CC} = 1V, I_{SINK} = 50µA			0.3	
		MAX70_E/M, V_{CC} = 1.2V, I_{SINK} = 100µA			0.3	
RESET Output Voltage		MAX707/MAX708, I_{SOURCE} = 800µA	V_{CC} - 1.5			V
		MAX707/MAX708, I_{SINK} = 1.2mA			0.4	
Watchdog Timeout Period	t_{WD}	MAX705/MAX706	1.00	1.60	2.25	sec
WDI Pulse Width	t_{WP}	V_{IL} = 0.4V, V_{IH} = (V_{CC}) (0.80)	50			ns
WDI Input Threshold Low		MAX705/MAX706, V_{CC} = +5V			0.8	V
High			3.5			
WDI Input Current		MAX705/MAX706, WDI = V_{CC}		50	150	µA
		MAX705/MAX706, WDI = 0V	-150	-50		
$\overline{WDO}$ Output Voltage		MAX705/MAX706, I_{SOURCE} = 800µA	V_{CC} - 1.5			V
		MAX705/MAX706, I_{SINK} = 1.2mA			0.4	
$\overline{MR}$ Pull-Up Current		$\overline{MR}$ = 0V	100	250	600	µA
$\overline{MR}$ Pulse Width	t_{MR}		150			ns
$\overline{MR}$ Input Threshold Low					0.8	V
High			2.0			
$\overline{MR}$ to Reset Out Delay (Note 2)	t_{MD}				250	ns

ELECTRICAL CHARACTERISTICS (continued)

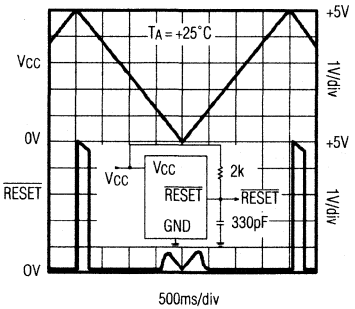
(V_{CC} = +4.75V to +5.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PFI Input Threshold		V_{CC} = +5V	1.20	1.25	1.30	V
PFI Input Current			-25.00	0.01	25.00	nA
$\overline{PFO}$ Output Voltage		I_{SOURCE} = 800µA	V_{CC} - 1.5			V
		I_{SINK} = 3.2mA			0.4	

Note 2: Applies to both $\overline{RESET}$ in the MAX705-708 and RESET in the MAX707/MAX708.

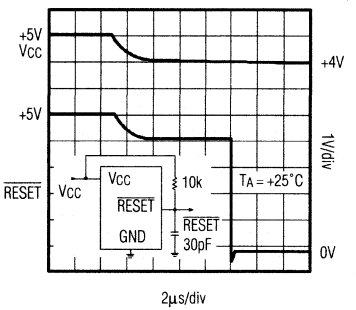
Typical Operating Characteristics

MAX705/MAX707
$\overline{RESET}$ OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



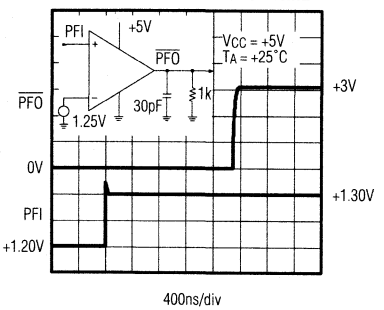
500ms/div

MAX705/MAX707
$\overline{RESET}$ RESPONSE TIME



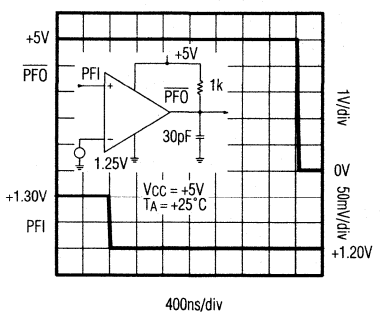
2µs/div

POWER-FAIL COMPARATOR DE-ASSERTION RESPONSE TIME



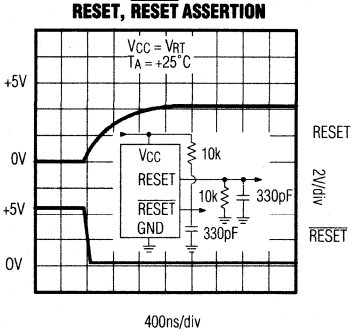
400ns/div

POWER-FAIL COMPARATOR ASSERTION RESPONSE TIME



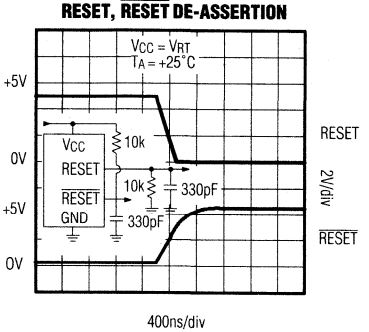
400ns/div

MAX707
RESET, $\overline{RESET}$ ASSERTION



400ns/div

MAX707
RESET, $\overline{RESET}$ DE-ASSERTION



400ns/div

Low-Cost, µP Supervisory Circuits

Pin Description

PIN		NAME	FUNCTION
MAX705/ MAX706	MAX707/ MAX708		
1	1	$\overline{MR}$	Manual Reset Input triggers a reset pulse when pulled below 0.8V. This active-low input has an internal 250mA pull-up current. It can be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
2	2	V_{CC}	+5V Supply Input
3	3	GND	0V Ground Reference for all signals
4	4	PFI	Power-Fail Voltage Monitor Input. When PFI is less than 1.25V, $\overline{PFO}$ goes low. Connect PFI to GND or V_{CC} when not used.
5	5	$\overline{PFO}$	Power-Fail Output goes low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
6	–	WDI	Watchdog Input. If WDI remains high or low for 1.6 seconds, the internal watchdog timer runs out and $\overline{WDO}$ goes low (Figure 1). Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever $\overline{RESET}$ pulses, WDI is three-stated, or WDI sees a rising or falling edge.
-	6	N.C.	No Connect
7	7	$\overline{RESET}$	Active-Low Reset Output pulses low for 200ms when triggered, and stays low whenever V_{CC} is below the reset threshold (4.65V in the MAX705 and 4.40V in the MAX706). It remains low for 200ms after V_{CC} rises above the reset threshold or $\overline{MR}$ goes from low to high (Figure 3). A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
8	–	$\overline{WDO}$	Watchdog Output pulls low when the internal watchdog timer finishes its 1.6 second count, and does not go high again until the watchdog is cleared. $\overline{WDO}$ also goes low during low-line conditions. Whenever V_{CC} is below the reset threshold, $\overline{WDO}$ stays low; however, unlike $\overline{RESET}$, $\overline{WDO}$ does not have a minimum pulse width. As soon as V_{CC} rises above the reset threshold, $\overline{WDO}$ goes high with no delay.
–	8	RESET	Active-High Reset Output is the inverse of $\overline{RESET}$. Whenever $\overline{RESET}$ is high, RESET is low, and vice versa (Figure 2).

Detailed Description

Reset Output

A microprocessor's (µP's) reset input starts the µP in a known state. Whenever the µP is in an unknown state, it should be held in reset. The MAX705-MAX708 assert reset during power-up and prevent code execution errors during power-down or brownout conditions.

On power-up, once V_{CC} reaches 1V, $\overline{RESET}$ is a guaranteed logic low of 0.4V or less. As V_{CC} rises, $\overline{RESET}$ stays low. When V_{CC} rises above the reset threshold, an internal timer releases $\overline{RESET}$ after about 200ms. $\overline{RESET}$ pulses low whenever V_{CC} dips below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power-down, once V_{CC} falls below the reset threshold, $\overline{RESET}$ stays low and is guaranteed to be 0.4V or less until V_{CC} drops below 1V.

The MAX707/MAX708 active-high RESET output is simply the complement of the $\overline{RESET}$ output. Some µPs, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Timer

The MAX705/MAX706 watchdog circuit monitors the µP's activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec and WDI is not three-stated, $\overline{WDO}$ goes low. As long as $\overline{RESET}$ is asserted or the WDI input is three-stated, the watchdog timer will stay cleared and will not count. As soon as reset is released and WDI is driven high or low, the timer will start counting. Pulses as short as 50ns can be detected.

Typically, $\overline{WDO}$ will be connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the

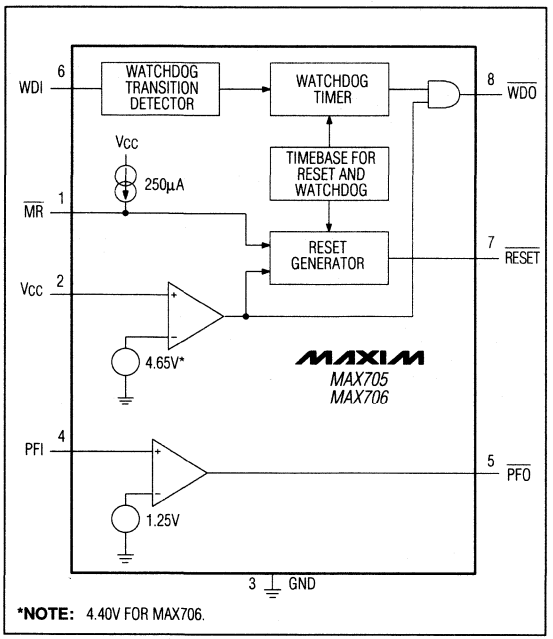


Figure 1. MAX705/MAX706 Block Diagram

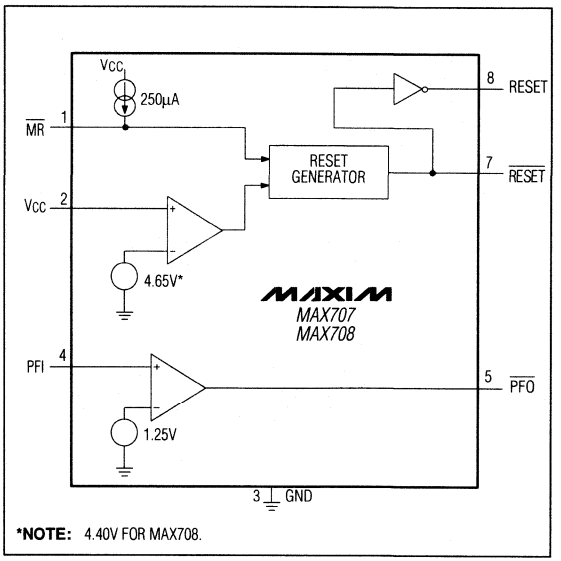


Figure 2. MAX707/MAX708 Block Diagram

reset threshold, $\overline{WDO}$ will go low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI interrupt, but $\overline{RESET}$ goes low simultaneously, and thus overrides the NMI interrupt.

If WDI is left unconnected, $\overline{WDO}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{WDO}$ goes low only when V_{CC} falls below the reset threshold, thus functioning as a low-line output.

Only the MAX705/MAX706 have a watchdog timer. The MAX707/MAX708 have an active-high reset output instead.

Manual Reset

The manual reset ($\overline{MR}$) input allows reset to be triggered by a pushbutton switch. The switch is effectively debounced by the 140ms minimum reset pulse width. $\overline{MR}$ is TTL/CMOS logic compatible, so it can be driven by an external logic line. $\overline{MR}$ can be used to force a watchdog timeout to generate a reset pulse in the MAX705/MAX706. Simply connect $\overline{WDO}$ to $\overline{MR}$.

Power-Fail Comparator

The power-fail comparator can be used for various purposes because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

To build an early-warning circuit for power failure, connect the PFI pin to a voltage divider (see *Typical Operating Circuit*). Choose the voltage divider ratio so that the voltage at PFI falls below 1.25V just before the +5V regulator drops out. Use $\overline{PFO}$ to interrupt the µP so it can prepare for an orderly power-down.

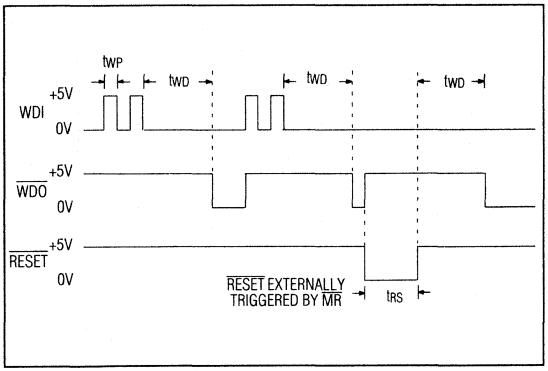


Figure 3. MAX705/MAX706 Watchdog Timing

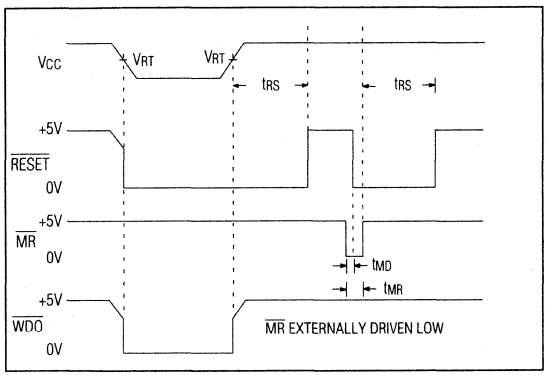


Figure 4. MAX705/MAX706 RESET, MR, and WDO Timing with WDI Three-Stated

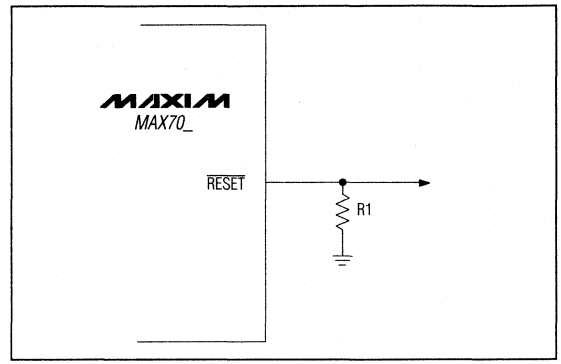


Figure 5. RESET Valid to Ground Circuit

Applications Information

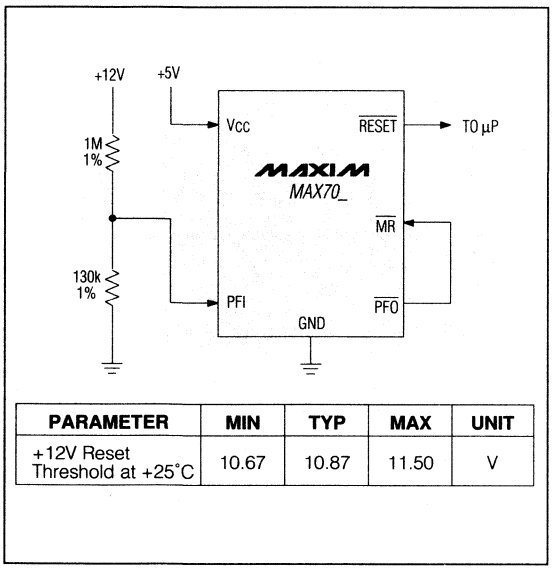
Ensuring a Valid RESET Output Down to VCC = 0V

When VCC falls below 1V, the MAX705-MAX708 RESET output no longer sinks current—it becomes an open circuit. High-impedence CMOS logic inputs can drift to undetermined voltages if left undriven. If a pull-down resistor is added to the RESET pin as shown in Figure 5, any stray charge or leakage currents will be drained to ground, holding RESET low. Resistor value (R1) is not critical. It should be about 100kΩ, large enough not to load RESET and small enough to pull RESET to ground.

Monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add hysteresis by connecting a resistor (with a value approximately 10 times the sum of the two resistors in the potential divider network) between PFI and PFO. A capacitor between PFI and GND will reduce the power-fail circuit's sensitivity to high-frequency noise on the line being monitored. RESET can be asserted on other voltages in addition to the +5V VCC line. Connect PFO to MR to initiate a RESET pulse when PFI drops below 1.25V. Figure 6 shows the MAX705-MAX708 configured to assert RESET when the +5V supply falls below the reset threshold, or when the +12V supply falls below approximately 11V.

Monitoring a Negative Voltage

The power-fail comparator can also monitor a negative supply rail (Figure 7). When the negative rail is good (a negative voltage of large magnitude), PFO is low, and when the negative rail is degraded (a negative voltage of lesser magnitude), PFO is high. By adding the resistors and transistor as shown, a high PFO triggers reset. As long as PFO remains high, the MAX705-MAX708 will keep reset asserted (RESET = low, RESET = high). Note that this circuit's accuracy depends on the PFI threshold tolerance, the VCC line, and the resistors.



PARAMETER	MIN	TYP	MAX	UNIT
+12V Reset Threshold at +25°C	10.67	10.87	11.50	V

Figure 6. Monitoring Both +5V and +12V

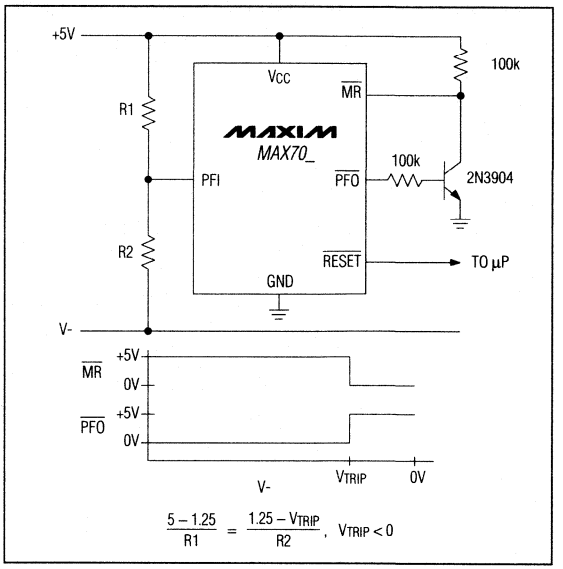


Figure 7. Monitoring a Negative Voltage

Table 1. Maxim µP Supervisory Products

Part Number	Nominal Reset Threshold (V)	Minimum Reset Pulse Width (ms)	Nominal Watchdog Timeout Period (sec)	Backup-Battery Switch	CE Write Protect	Power-Fail Comparator	Manual Reset Input	Watchdog Output	Low-Line Output	Active-High Reset	Batt-On Output
MAX690A	4.65	140	1.6	yes	no	yes	no	no	no	no	no
MAX691A	4.65	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX692A	4.40	140	1.6	yes	no	yes	no	no	no	no	no
MAX693A	4.40	140/adj.	1.6/adj.	yes	yes	yes	no	yes	yes	yes	yes
MAX696	adj.	35/adj.	1.6/adj.	yes	no	yes	no	yes	yes	yes	yes
MAX697	adj.	35/adj.	1.6/adj.	no	yes	yes	no	yes	yes	yes	no
MAX700	4.65/adj.	200	NA	no	no	no	yes	no	no	yes	no
MAX703	4.65	140	NA	yes	no	yes	yes	no	no	no	no
MAX704	4.40	140	NA	yes	no	yes	yes	no	no	no	no
MAX705	4.65	140	1.6	no	no	yes	yes	yes	no	no	no
MAX706	4.40	140	1.6	no	no	yes	yes	yes	no	no	no
MAX707	4.65	140	NA	no	no	yes	yes	no	no	yes	no
MAX708	4.40	140	NA	no	no	yes	yes	no	no	yes	no
MAX791	4.65	140	1	yes	yes	yes	yes	yes	yes	yes	yes
MAX1232	4.50/4.75	250	0.15/0.60/1.2	no	no	no	yes	no	no	yes	no
MAX1259	NA	NA	NA	yes	no	yes	no	no	no	no	no

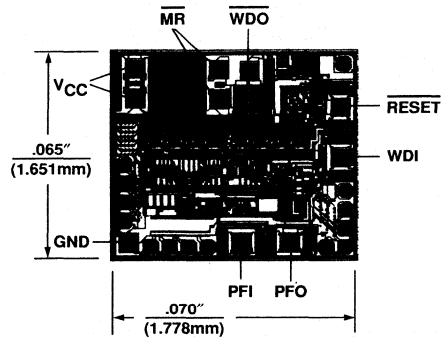
Low-Cost, µP Supervisory Circuits

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX706CPA	0°C to +70°C	8 Plastic DIP
MAX706CSA	0°C to +70°C	8 SO
MAX706C/D	0°C to +70°C	Dice*
MAX706EPA	-40°C to +85°C	8 Plastic DIP
MAX706ESA	-40°C to +85°C	8 SO
MAX706MJA	-55°C to +125°C	8 CERDIP**
MAX707CPA	0°C to +70°C	8 Plastic DIP
MAX707CSA	0°C to +70°C	8 SO
MAX707C/D	0°C to +70°C	Dice*
MAX707EPA	-40°C to +85°C	8 Plastic DIP
MAX707ESA	-40°C to +85°C	8 SO
MAX707MJA	-55°C to +125°C	8 CERDIP**
MAX708CPA	0°C to +70°C	8 Plastic DIP
MAX708CSA	0°C to +70°C	8 SO
MAX708C/D	0°C to +70°C	Dice*
MAX708EPA	-40°C to +85°C	8 Plastic DIP
MAX708ESA	-40°C to +85°C	8 SO
MAX708MJA	-55°C to +125°C	8 CERDIP**

** Dice are specified at T_A = +25°C.*
***Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



TRANSISTOR COUNT: 572;

SUBSTRATE MUST BE LEFT UNCONNECTED.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

Microprocessor Supervisory Circuit

General Description

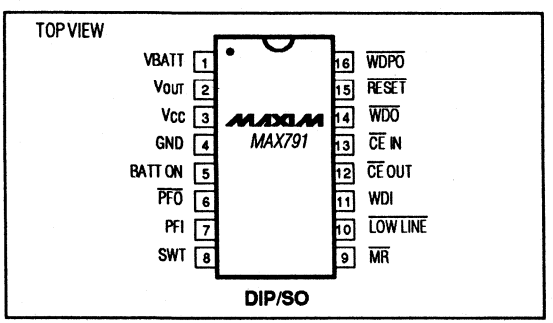
The MAX791 microprocessor (µP) supervisory circuit reduces the complexity and number of components needed to monitor power-supply and battery-control functions in µP systems by including µP reset, manual reset input, backup-battery switchover, watchdog timer, CMOS RAM write protection, software-readable low-battery detector, and power-fail warning.

The MAX791 features a 70µA supply current, 10ns clock-enable propagation delay, 250mA output current in VCC mode, and 25mA output current in battery-backup mode.

The MAX791 comes in 16-pin DIP and SO packages and provides a variety of functions:

1) $\overline{\text{RESET}}$ output is asserted during power-up, power-down, and brownout conditions, and is guaranteed to be in the correct state for VCC down to 1V
2) Manual reset input
3) A 1.28V threshold detector provides power-fail warning and low-battery detection, or monitors a power supply other than +5V
4) Two-stage power-fail warning – a separate low-line comparator compares VCC to a threshold 150mV the reset threshold
5) Backup-battery switchover for CMOS RAM, CMOS µPs, or other low-power logic
6) Software monitoring of backup-battery voltage
7) A watchdog fault output goes active if the optional watchdog timer (software monitor) has not been toggled within a specified time period
8) A preset or adjustable watchdog timeout period
9) Write protection of CMOS RAM or EEPROM
10) Pulsed watchdog output, to give advance warning impending reset caused by watchdog timeout.

Pin Configuration



Features

- **Guaranteed $\overline{\text{RESET}}$ Valid at VCC = 1V**
- **Precision 4.72V Voltage Monitoring**
- **200ms Power OK/Reset Time Delay**
- **Independent Watchdog Timer – Preset or Adjustable**
- **1µA Standby Current**
- **Battery-Backup Power Switching**
- **On-Board Gating of Chip-Enable Signals**
- **Voltage Monitor for Power-Fail or Low-Battery Warning**
- **Backup-Battery Monitor**

Applications

Computers

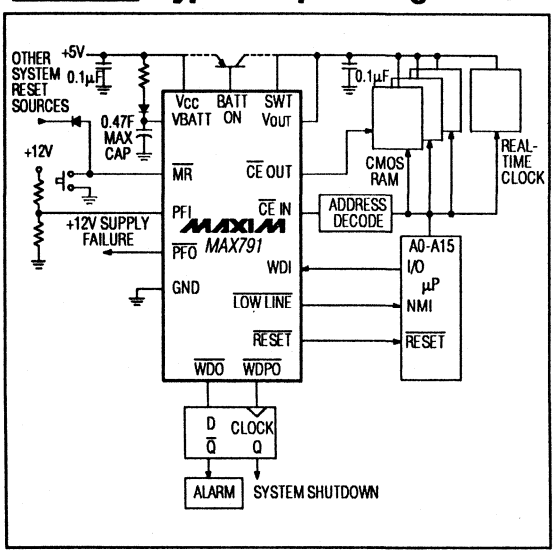
Controllers

Intelligent Instruments

Automotive System

Critical µP Power Monitoring

Typical Operating Circuit



* Advance Information – first page of data sheet in preparation.

Part Number	Description	Filter Type*	Filter Order**	Class	Cutoff-Frequency Range	Program Method	Price† 1000-up ($)
MAX270	Dual, lowpass	CH	4	Continuous	1.0kHz to 25kHz	µP bus/pin strap	6.95
MAX271	Dual + T/H, lowpass	CH	4	Continuous	1.0kHz to 25kHz	µP bus/pin strap	7.61
MAX274	Quad, band/lowpass	BT, BL, CH	8	Continuous	100Hz to 150kHz	Resistor	4.95
MAX275	Dual, band/lowpass	BT, BL, CH	4	Continuous	100Hz to 300kHz	Resistor	3.75
MF10	Dual, biquad	Universal	4	Switched capacitor	0.1Hz to 30kHz	Resistor	1.70
MAX260	Dual, biquad	Universal	4	Switched capacitor	0.01Hz to 7.5kHz	µP bus	6.49
MAX261	Dual, biquad	Universal	4	Switched capacitor	0.40Hz to 57kHz	µP bus	6.50
MAX262	Dual, biquad	Universal	4	Switched capacitor	1.00Hz to 140kHz	µP bus	7.49
MAX263	Dual, biquad	Universal	4	Switched capacitor	0.40Hz to 57kHz	Pin strap	6.89
MAX264	Dual, biquad	Universal	4	Switched capacitor	1.00Hz to 140kHz	Pin strap	7.50
MAX265	Dual, biquad	Universal	4	Switched capacitor	0.40Hz to 57kHz	Pin/resistor	6.49
MAX266	Dual, biquad	Universal	4	Switched capacitor	1.00Hz to 140kHz	Pin/resistor	7.50
MAX267	Dual, biquad	Universal	4	Switched capacitor	0.40Hz to 57kHz	Pin strap	6.50
MAX268	Dual, biquad	Universal	4	Switched capacitor	1.00Hz to 140kHz	Pin strap	7.00
MAX280	Single, lowpass	BT	5	Switched capacitor	DC to 20kHz	Clock, resistor, capacitor	3.99
MAX281	Single, lowpass	BL	5	Switched capacitor	DC to 20kHz	Clock, resistor, capacitor	3.99
MAX291	Single, lowpass	BT	8	Switched capacitor	0.1Hz to 25kHz	Clock	2.95
MAX292	Single, lowpass	BL	8	Switched capacitor	0.1Hz to 25kHz	Clock	2.95
MAX293	Single, lowpass	ET	8	Switched capacitor	0.1Hz to 25kHz	Clock	††
MAX294	Single, lowpass	ET	8	Switched capacitor	0.1Hz to 25kHz	Clock	††
MAX295	Single, lowpass	BT	8	Switched capacitor	0.1Hz to 50kHz	Clock	2.95
MAX296	Single, lowpass	BL	8	Switched capacitor	0.1Hz to 50kHz	Clock	2.95
MAX297	Single, lowpass	ET	8	Switched capacitor	0.1Hz to 50kHz	Clock	††
LTC1062	Single, lowpass	BT	5	Switched capacitor	DC to 20kHz	Clock, resistor, capacitor	5.19

* BT = Butterworth, BL = Bessel, CH = Chebyshev, EL = Elliptic, Universal = All Filter Types
** Order level achieved by cascading all filters in package.
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.

ACTIVE FILTERS

SWITCHED-CAPACITOR FILTERS

UNIVERSAL

µP PROG.

MAX260 (dual/7.5kHz/2P)

MAX261 (dual/57kHz/2P)

MAX262 (dual/140kHz/2P)

PIN PROG.

MAX263 (dual/57kHz/2P)

MAX264 (dual/140kHz/2P)

RESISTOR PROG

MAX265 (dual/57kHz/2P)

MAX266 (dual/140kHz/2P)

MF10 (dual/30kHz/2P)

BANDPASS PIN PROG.

MAX267 (dual/57kHz/2P)

MAX268 (dual/140kHz/2P)

CLK PROG. LOWPASS

MAX280 (20kHz/5P)

MAX281 (20kHz/5P)

★ **MAX291** (25kHz/8P)

★ **MAX292** (25kHz/8P)

★ **MAX293** (25kHz/8P)

★ **MAX294** (25kHz/8P)

★ **MAX295** (50kHz/8P)

★ **MAX296** (50kHz/8P)

★ **MAX297** (50kHz/8P)

LTC1062 (20kHz/5P)

CONTINUOUS FILTERS

LOWPASS 2nd ORDER

MAX270 (dual/1-25kHz/2P)

MAX271 (dual/1-25kHz/2P)

LOWPASS/BANDPASS

MAX274 (quad/200kHz/2P)

MAX275 (dual/400kHz/2P)

NOTE: #P = Number of poles (e.g. 4P = 4 poles = 4th order)

★ New product since the publication of the 1990 Short Form Product Guide.

19-4191; Rev. 1; 7/92

MAX274 Evaluation Kit & MAX274/275 Software Manuals Follow Data Sheet

MAXIM

4th- and 8th-Order Continuous-Time Active Filters

General Description

The MAX274 and MAX275 are continuous-time active filters consisting of independent cascadable 2nd-order sections. Each section can implement any all-pole bandpass or lowpass filter response, such as Butterworth, Bessel, and Chebyshev, and is programmed by four external resistors. The MAX274/MAX275 provide lower noise than switched-capacitor filters, as well as superior dynamic performance - both due to the continuous-time design. Since continuous-time filters do not require a clock, aliased and clock noise are eliminated with the MAX274/MAX275.

The MAX274 comprises four 2nd-order sections, permitting 8th-order filters to be realized. Center frequencies range up to 150kHz, and are accurate to within ±1% over the full operating temperature range. Total harmonic distortion (THD) is typically better than -89dB

The MAX275 comprises two 2nd-order sections, permitting 4th-order filters to be realized. Center frequencies range up to 300kHz, and are accurate to within ±0.9% over the full operating temperature range. Total harmonic distortion (THD) is typically better than -86dB

Both filters operate from a single +5V supply or from dual ±5V supplies

Applications

Low-Distortion Anti-Aliasing Filters
DAC Output Smoothing Filters
Modems
Audio/Sonar/Avionics Frequency Filtering
Vibration Analysis

Features

- **Continuous-Time Filter - No Clock, No Clock Noise**
- **Implement Butterworth, Chebyshev, Bessel and Other Filter Responses**
- **Lowpass, Bandpass Outputs**
- **Operate from a Single +5V Supply or Dual ±5V Supplies**
- **Design Software Available**
- **MAX274 Evaluation Kit Available**
- **8th-Order – Four 2nd-Order Sections (MAX274)**
  4th-Order – Two 2nd-Order Sections (MAX275)
- **Center-Frequency Range:**
  150kHz for MAX274
  300kHz for MAX275
- **Low Noise: -86dB THD Typical for MAX274**
  -89dB THD Typical for MAX275
- **Center-Frequency Accurate Over Temp:**
  within ±1% for MAX274
  within ±0.9% for MAX275

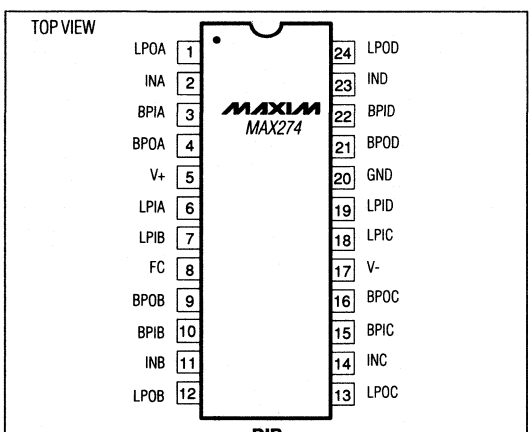
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX274ACNG	0°C to +70°C	24 Narrow Plastic DIP
MAX274BCNG	0°C to +70°C	24 Narrow Plastic DIP
MAX274ACWI	0°C to +70°C	28 Wide SO
MAX274BCWI	0°C to +70°C	28 Wide SO
MAX274BC/D	0°C to +70°C	Dice*

Ordering Information continued on last page

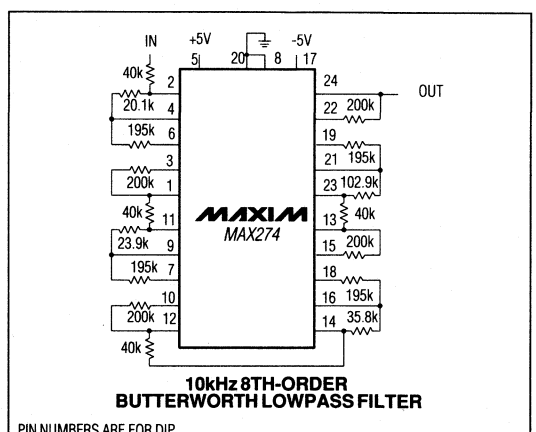
* *Contact factory for dice specifications.*

Pin Configurations



Pin Configurations continued on last page

Typical Operating Circuits



10kHz 8TH-ORDER BUTTERWORTH LOWPASS FILTER

PIN NUMBERS ARE FOR DIP.

Typical Operating Circuits continued on last page

4th- and 8th-Order Continuous-Time Active Filters

ABSOLUTE MAXIMUM RATINGS

V+ to V- ..... -0.3V, 12V
Input Voltage to GND (any input) ..... V- - 0.3V, V+ + 0.3V
Continuous Power Dissipation (T_A = +70°C)
MAX274
24-Pin Narrow Plastic DIP
(derate 13.33mW/°C above +70°C) ... 1067mW
28-Pin Wide SO (derate 12.50mW/°C above +70°) . 1000mW
24-Pin CERDIP (derate 12.50mW/°C above +70°C) . 1000mW
MAX275
20-Pin Plastic DIP(derate 11.11mW/°C above +70°C) 889mW
20-Pin Wide SO (derate 10.00mW/°C above +70°) .. 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) .. 889mW

Operating Temperature Ranges:
MAX27_ _C_ _ ..... 0°C to +70°C
MAX27_ _E_ _ ..... -40°C to +85°C
MAX27_ _MRG ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX274

(V+ = 5V, V- = -5V, test circuit A of Figure 1a, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS							
Maximum Operating Frequency					10		MHz
Center-Frequency Range	F_O	(Note 1)			100 to 150k		Hz
Center-Frequency Accuracy	F_O		MAX274A	-1.0		1.0	%
			MAX274B	-1.4		1.4	
Q Accuracy - Unadjusted			MAX274A	-10		10	%
			MAX274B	-15		15	
Q Accuracy - Adjusted		Scaled for bandwidth compensation			±2.8		%
F_O Temperature Coefficient	$\Delta F_O/\Delta T$	(Note 2)			-28		ppm/°C
Q Temperature Coefficient	$\Delta Q/\Delta T$	(Note 2)			160		ppm/°C
Wideband Noise	V_{NOISE}	LPO_, Figure 1a, test circuit B	1Hz to 10Hz		23		μV_{RMS}
			10Hz to 10kHz		120		
DC CHARACTERISTICS							
DC Lowpass Gain Accuracy	H_{OLP}	Assume ideal resistors	MAX274A	-2		2	%
			MAX274B	-3		3	
Offset Voltage at Outputs	V_{OS}	LPO_	MAX274A	-200		200	mV
			MAX274B	-300		300	
		BPO_	MAX274A	-40		40	
			MAX274B	-80		80	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$				20		µV/°C
Leakage Current at FC Pin	I_{FC}			-10		10	µA
DYNAMIC FILTER CHARACTERISTICS							
Signal-to-Noise plus Distortion	SINAD	F_{TEST} = 1kHz, Figure 1a, test circuit B	LPO_, V_{LPO} = 8Vp-p		-86		dB
		F_{TEST} = 10kHz, Figure 1a, test circuit C			-82		

ELECTRICAL CHARACTERISTICS (continued) – MAX274

(V+ = 5V, V- = -5V, test circuit A of Figure 1a, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing	V_{OUT}	LPO_ , BPO_ , R_{LOAD} = 5kΩ	±3.25	±4.50		V
Slew Rate	SR			10		V/µs
Gain-Bandwidth Product	GBW			7.5		MHz
POWER REQUIREMENTS						
Supply Voltage Range	V_{SUPP}	(Note 3)	±2.37		±5.50	V
Supply Current	I_C	For V+, V-		20	30	mA
Power-Supply Rejection Ratio	PSRR	V+ = 5V + 100mVp-p at 1kHz, V- = -5V		-30		dB

Note 1: Center frequencies (F_Os) below 100Hz are possible at reduced dynamic range.
Note 2: Assume no drift for external resistors.
Note 3: See Figure 9 for single-supply operation.

ELECTRICAL CHARACTERISTICS – MAX275

(V+ = 5V, V- = -5V, test circuit A of Figure 1b, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS							
Maximum Operating Frequency					10		MHz
Center-Frequency Range	F_O	(Note 1)			100 to 300k		Hz
Center-Frequency Accuracy	F_O		MAX275A	-0.9		0.9	%
			MAX275B	-1.4		1.4	
Q Accuracy – Unadjusted			MAX275A	-8		8	%
			MAX275B	-12		12	
Q Accuracy – Adjusted		Scaled for bandwidth compensation			±1		%
F_O Temperature Coefficient	$\Delta F_O/\Delta T$	(Note 2)			-24		ppm/°C
Q Temperature Coefficient	$\Delta Q/\Delta T$	(Note 2)			38		ppm/°C
Wideband Noise	V_{NOISE}	LPO_, test circuit B of Figure 1b,	1Hz to 10Hz		6		µVRMS
			10Hz to 10kHz		42		
DC CHARACTERISTICS							
DC Lowpass Gain Accuracy	H_{OLP}	Assume ideal resistors	MAX275A	-1		1	%
			MAX275B	-2		2	
Offset Voltage at Outputs	V_{OS}	LPO_	MAX275A	-125		125	mV
			MAX275B	-250		250	
		BPO_	MAX275A	-50		50	
			MAX275B	-100		100	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$				20		µV/°C
Leakage Current at FC Pin	I_{FC}			-10		10	µA
DYNAMIC FILTER CHARACTERISTICS							
Signal-to-Noise plus Distortion	SINAD	F_{TEST} = 1kHz, test circuit B of Figure 1b,	LPO_, V_{LPO} = 8Vp-p		-89		dB
		F_{TEST} = 10kHz, test circuit C of Figure 1b,			-83		

4th- and 8th-Order Continuous-Time Active Filters

ELECTRICAL CHARACTERISTICS (continued) – MAX275

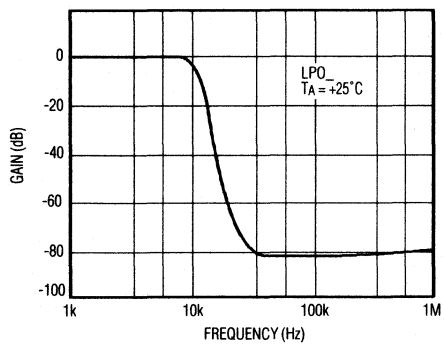
(V+ = 5V, V- = -5V, test circuit A of Figure 1b, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Swing	V_{OUT}	LPO_, BPO_, R_{LOAD} = 5kΩ	±3.25	±4.50		V
Internal Amplifier Slew Rate	SR			10		V/µs
Gain-Bandwidth Product	GBW			15		MHz
POWER REQUIREMENTS						
Supply Voltage Range	V_{SUPP}	(Note 3)	±2.37		±5.50	V
Supply Current	I_C	For V+, V-		10	24	mA
Power-Supply Rejection Ratio	PSRR	V+ = 5V + 100mVp-p at 1kHz, V- = -5V		-35		dB

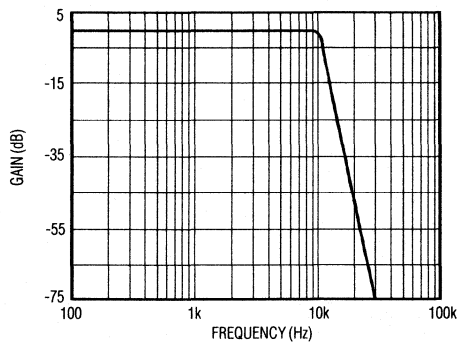
Note 1: Center frequencies (F_0s) below 100Hz are possible at reduced dynamic range.
Note 2: Assume no drift for external resistors.
Note 3: See Figure 9 for single-supply operation.

Typical Operating Characteristics–MAX274

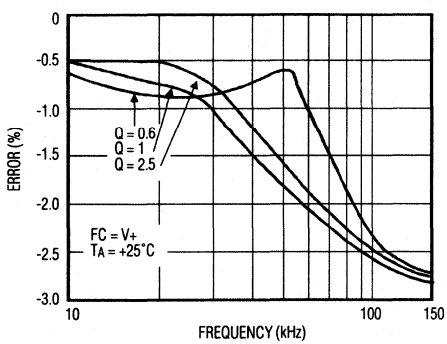
FILTER WIDEBAND RESPONSE USING TYPICAL OPERATING CIRCUIT



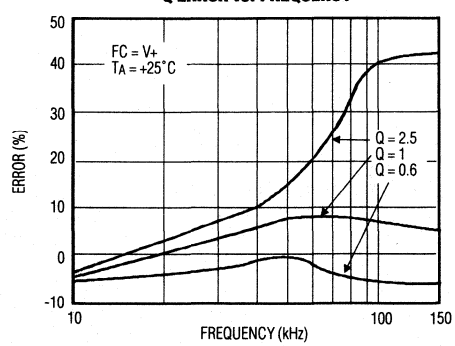
FILTER RESPONSE USING TYPICAL OPERATING CIRCUIT



F_0 ERROR vs. FREQUENCY

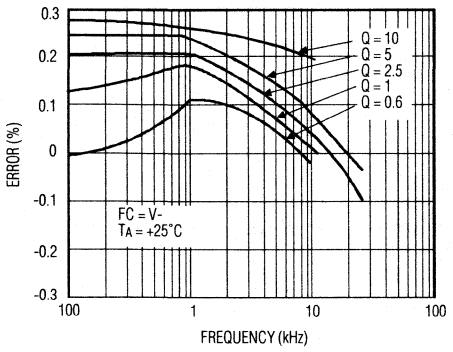


Q ERROR vs. FREQUENCY

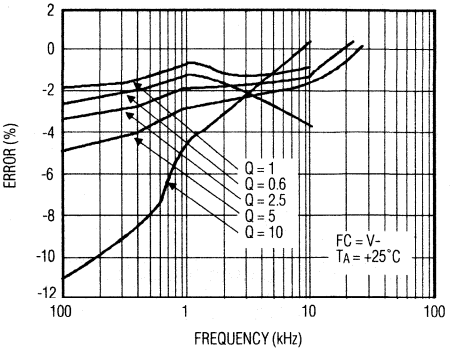


Typical Operating Characteristics–MAX274 (continued)

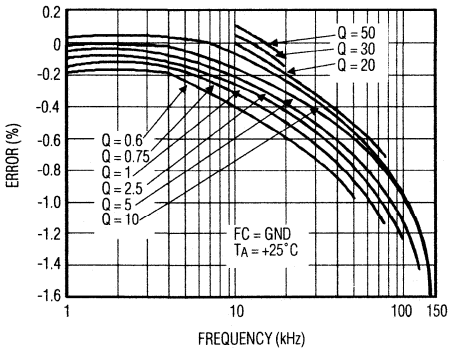
F_0 ERROR vs. FREQUENCY



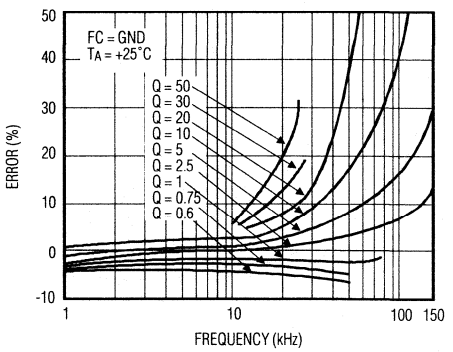
Q ERROR vs. FREQUENCY



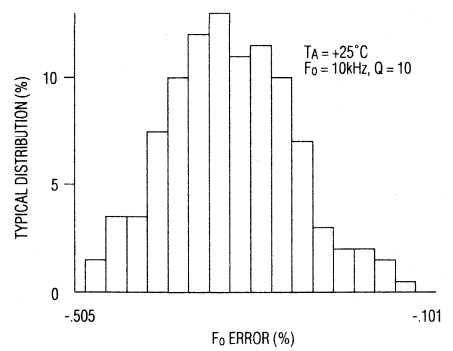
F_0 ERROR vs. FREQUENCY



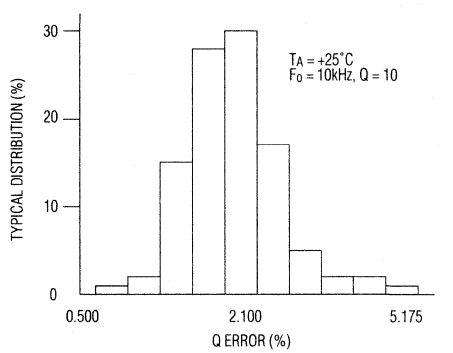
Q ERROR vs. FREQUENCY



TYPICAL DISTRIBUTION OF CENTER-FREQUENCY ERRORS



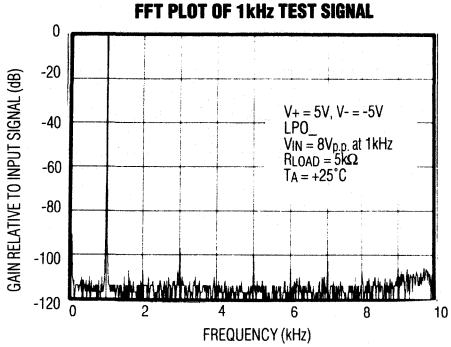
TYPICAL DISTRIBUTION OF Q ERRORS



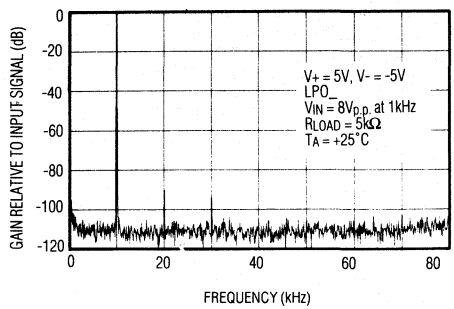
4th- and 8th-Order Continuous-Time Active Filters

Typical Operating Characteristics–MAX274 (continued)

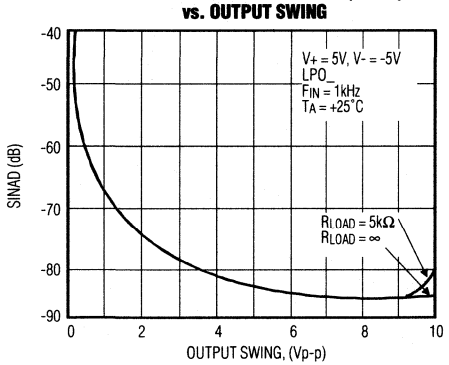
FFT PLOT OF 1kHz TEST SIGNAL



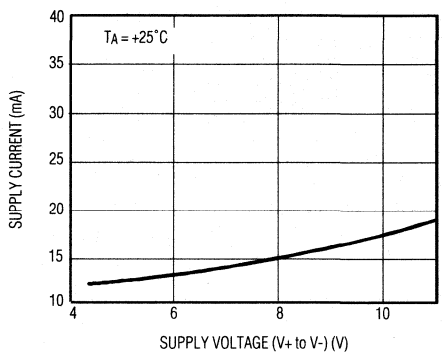
FFT PLOT OF 10kHz TEST SIGNAL



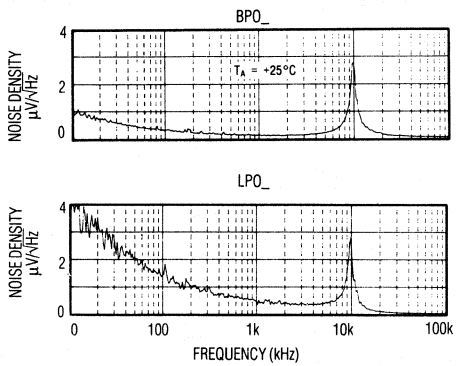
SIGNAL TO NOISE + DISTORTION (SINAD) vs. OUTPUT SWING



SUPPLY CURRENT vs. SUPPLY VOLTAGE

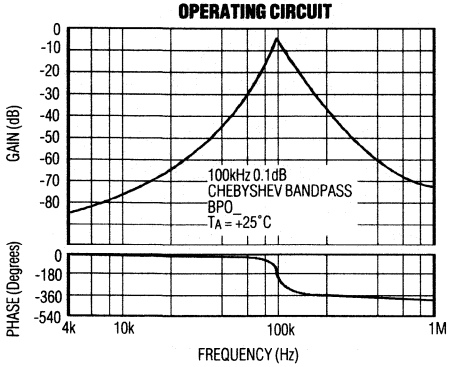


SPECTRAL NOISE DENSITY vs. FREQUENCY

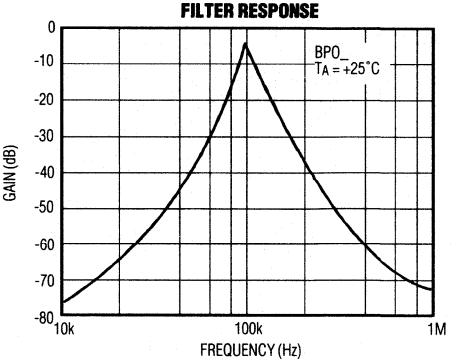


Typical Operating Characteristics–MAX275

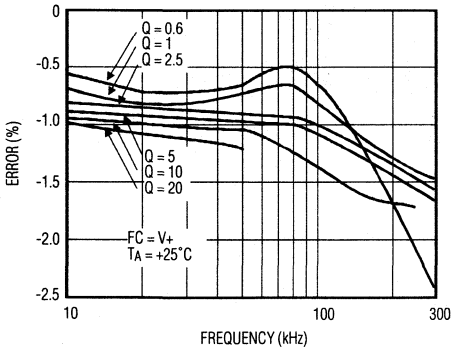
FILTER WIDEBAND RESPONSE USING TYPICAL OPERATING CIRCUIT



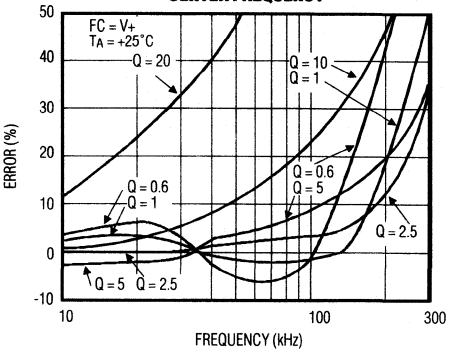
FILTER RESPONSE



CENTER-FREQUENCY ERROR vs. PROGRAMMED CENTER FREQUENCY



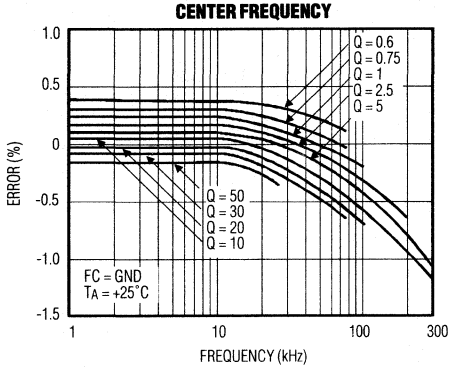
Q ERROR vs. PROGRAMMED CENTER FREQUENCY



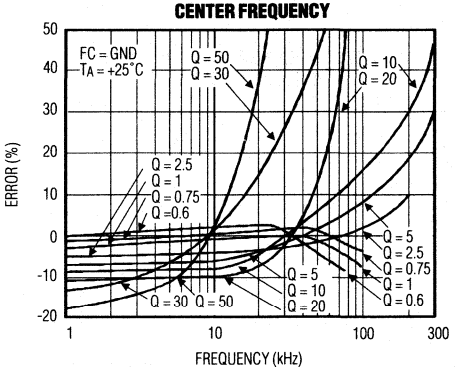
4th- and 8th-Order Continuous-Time Active Filters

Typical Operating Characteristics–MAX275 (continued)

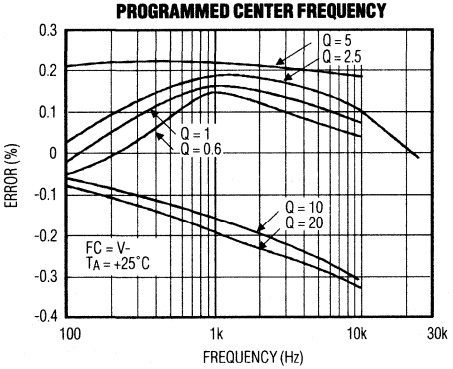
CENTER-FREQUENCY ERROR vs. PROGRAMMED CENTER FREQUENCY



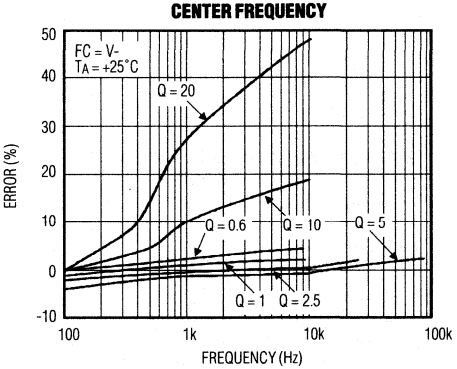
Q ERROR vs. PROGRAMMED CENTER FREQUENCY



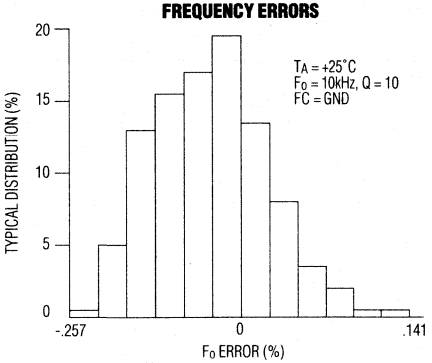
CENTER-FREQUENCY ERROR vs. PROGRAMMED CENTER FREQUENCY



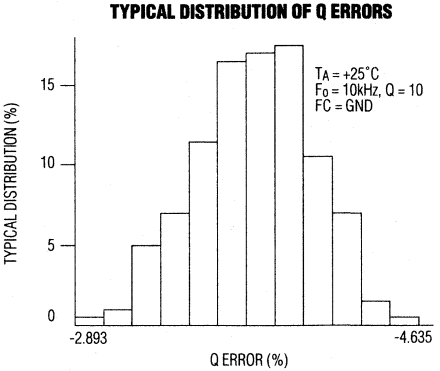
Q ERROR vs. PROGRAMMED CENTER FREQUENCY



TYPICAL DISTRIBUTION OF CENTER-FREQUENCY ERRORS

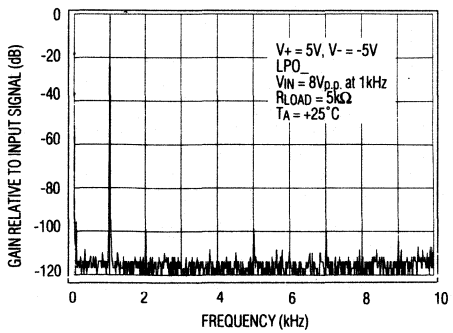


TYPICAL DISTRIBUTION OF Q ERRORS

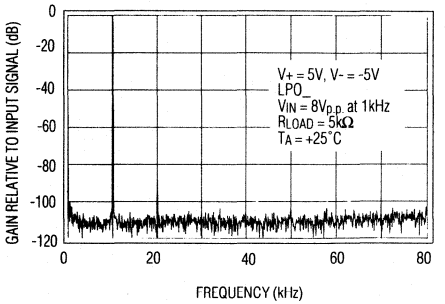


Typical Operating Characteristics–MAX275 (continued)

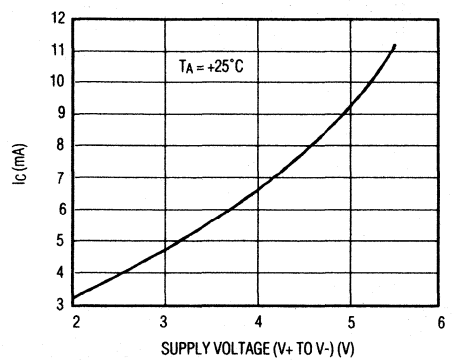
FFT PLOT OF 1kHz TEST SIGNAL



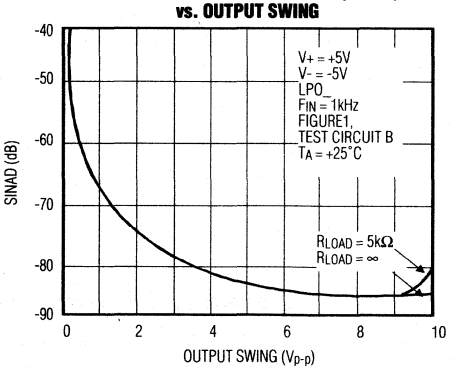
FFT PLOT OF 10kHz TEST SIGNAL



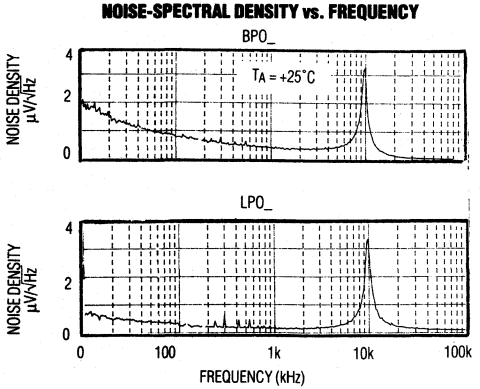
SUPPLY CURRENT vs. SUPPLY VOLTAGE



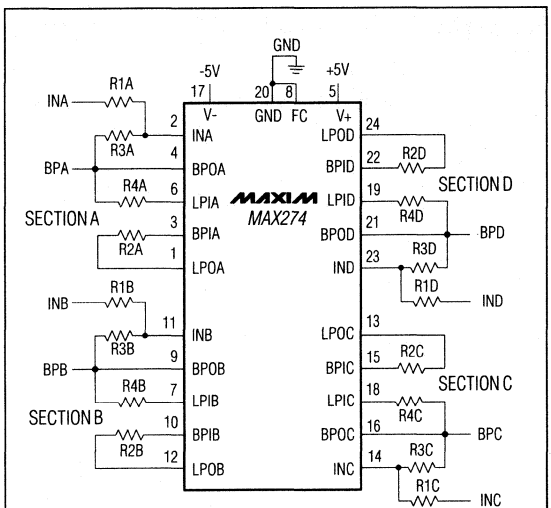
SIGNAL-TO-NOISE + DISTORTION (SINAD) vs. OUTPUT SWING



NOISE-SPECTRAL DENSITY vs. FREQUENCY



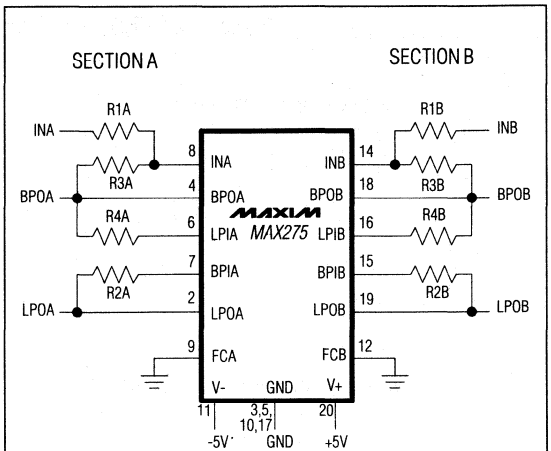
4th- and 8th-Order Continuous-Time Active Filters



PIN NUMBERS ARE FOR DIP.

TEST CIRCUIT	F_O (kHz)	Q	R1X (kΩ)	R2X (kΩ)	R3X (kΩ)	R4X (kΩ)	FC PIN
A	10	10	80	200	400	195	GND
B	10	0.707	40	200	28	195	GND
C	100	0.707	40	20	48	15	V+

Figure 1a. MAX274 Connection Diagram and Test Circuit



PIN NUMBERS ARE FOR DIP.

TEST CIRCUIT	F_O (kHz)	Q	R1X (kΩ)	R2X (kΩ)	R3X (kΩ)	R4X (kΩ)	FC PIN
A	10	10	80	200	400	195	GND
B	10	0.707	40	200	28	195	GND
C	100	0.707	40	20	48	14	V+

Figure 1b. MAX275 Connection Diagram and Test Circuit

Detailed Description

The MAX274 contains four identical 2nd-order filter sections while the MAX275 contains two sections. Figure 2 shows the state-variable topography employed in each filter section. This topography allows simultaneous lowpass and bandpass functions at separate outputs.

The MAX274/MAX275 employ a four-amplifier design, chosen for its relative insensitivity to parasitic capacitances and high bandwidth. The built-in capacitors and amplifiers, together with external resistors, form cascaded integrators with feedback to provide simultaneous lowpass and bandpass filtered outputs. To maximize bandwidth, the highpass (HP) node is not accessible. A 5kΩ resistor is connected in series with the input of the last stage amplifier to isolate the integration capacitor from external parasitic capacitances that could alter the filter's pole accuracy.

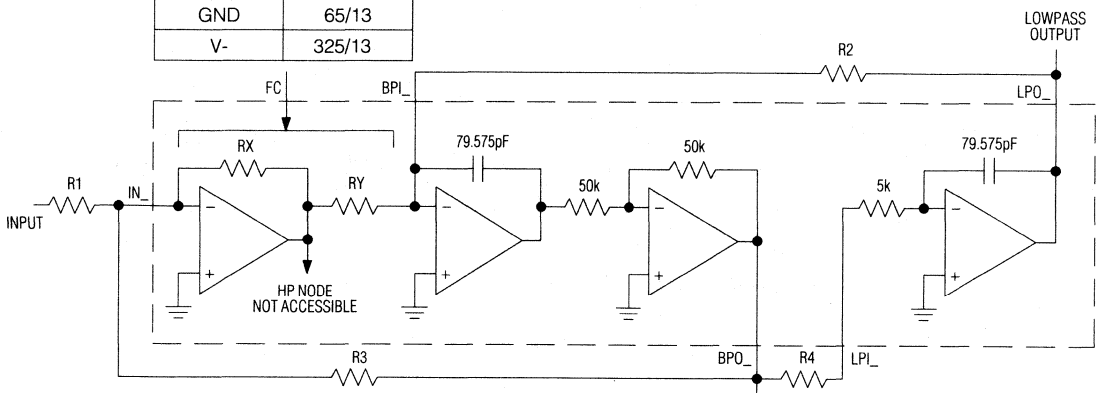
Although a notch output pin is not available, a notch can be created at the pole frequency by summing the input and bandpass output. See Creating a Notch Output Section

Filter Design Procedure

Figure 3 outlines the overall filter design procedure. Maxim's Filter Design Software is highly recommended. This software automatically calculates filter order, poles, and Qs based on the required filter shape, so no manual calculations are necessary. Menu-driven commands and on-screen filter response graphs take the user through the complete design process, including the selection of resistor values for implementing a filter with the MAX274/MAX275. See *Maxim Filter Design Software* section.

If designing without the filter software, see the filter design references listed at the end of this data sheet. These references provide numerical tables and equations needed to translate a desired filter response into order, poles, and Q. Once these three parameters have been calculated, see the next section, *Translating F_O/Q Pairs into MAX274/MAX275 Hardware (Resistor Selection).*

CONNECT FC TO:	RY/RX* (kΩ)
V+	13/52
GND	65/13
V-	325/13



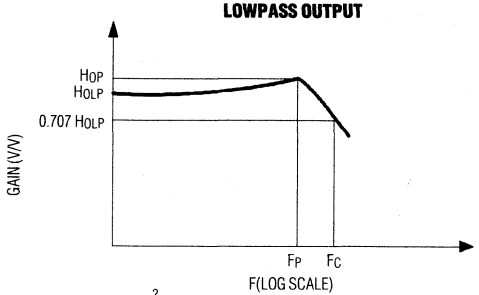
$$F_o\,(Hz) = \left(\sqrt{\frac{1}{(R2)\,(R4 + 5k\Omega)}}\right)(2 \times 10^9) \qquad H_{OBP} = \text{BP GAIN AT } F_o = \frac{R3}{R1}$$

$$Q = \left(\sqrt{\frac{1}{(R2)\,(R4 + 5k\Omega)}}\right)(R3)\left(\frac{RY}{RX}\right) \qquad H_{OLP} = \text{LP GAIN AT DC} = \left(\frac{R2}{R1}\right)\left(\frac{RX}{RY}\right)$$

EQUATIONS DO NOT INCLUDE COMPENSATION FACTORS THAT CORRECT SMALL ERRORS IN F_O AND Q DUE TO AMPLIFIER BANDWIDTH LIMITATIONS. SEE *TYPICAL OPERATING CHARACTERISTICS* FOR CORRECTION FACTORS.

* WHILE THE RATIO RY/RX IS ACCURATELY CONTROLLED, PROCESS VARIATIONS AND TEMPERATURE DRIFT RESULT IN UP TO ±30% VARIATION OF ACTUAL VALUES OF RX AND RY.

LOWPASS OUTPUT



$$G(S) = H_{OLP}\frac{{\omega_0}^2}{S^2 + S(\omega_0/Q) + {\omega_0}^2}$$

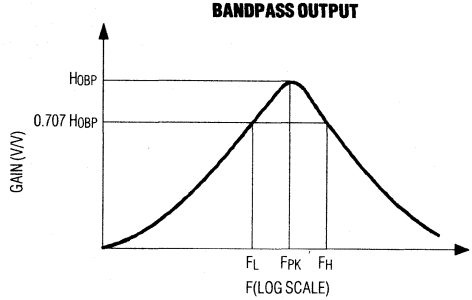
H_{OLP} = LOWPASS OUTPUT GAIN AT DC

$F_O = \omega_0/2\pi$ = POLE FREQUENCY

$$(F_C) = (F_O)\sqrt{\left(1 - \frac{1}{2Q^2}\right) + \sqrt{\left(1 - \frac{1}{2Q^2}\right)^2 + 1}}$$

$$F_P = F_O\sqrt{1 - \frac{1}{2Q^2}} \qquad H_{OP} = (H_{OLP})\frac{1}{\frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}}$$

BANDPASS OUTPUT



$$G(S) = H_{OBP}\frac{S(\omega_0/Q)}{S^2 + S(\omega_0/Q) + {\omega_0}^2}$$

H_{OBP} = BP GAIN AT $\omega = \omega_0$

$F_O = \omega_0/2\pi$ = THE CENTER FREQUENCY OF THE COMPLEX POLE PAIR. INPUT-OUTPUT PHASE SHIFT IS - 180° AT F_O.

F_{PK} = THE FREQUENCY AT WHICH BPO_ GAIN IS THE GREATEST (MAY NOT BE EQUAL TO F_O).

Q = THE QUALITY FACTOR OF THE COMPLEX POLE PAIR. ALSO THE RATIO OF F_O, TO -3dB (0.707) BANDWIDTH OF THE SECOND-ORDER BANDPASS RESPONSE.

$$Q = \frac{F_{PK}}{F_H - F_L}$$

Figure 2. Single 2nd-Order Filter Section

4th- and 8th-Order Continuous-Time Active Filters

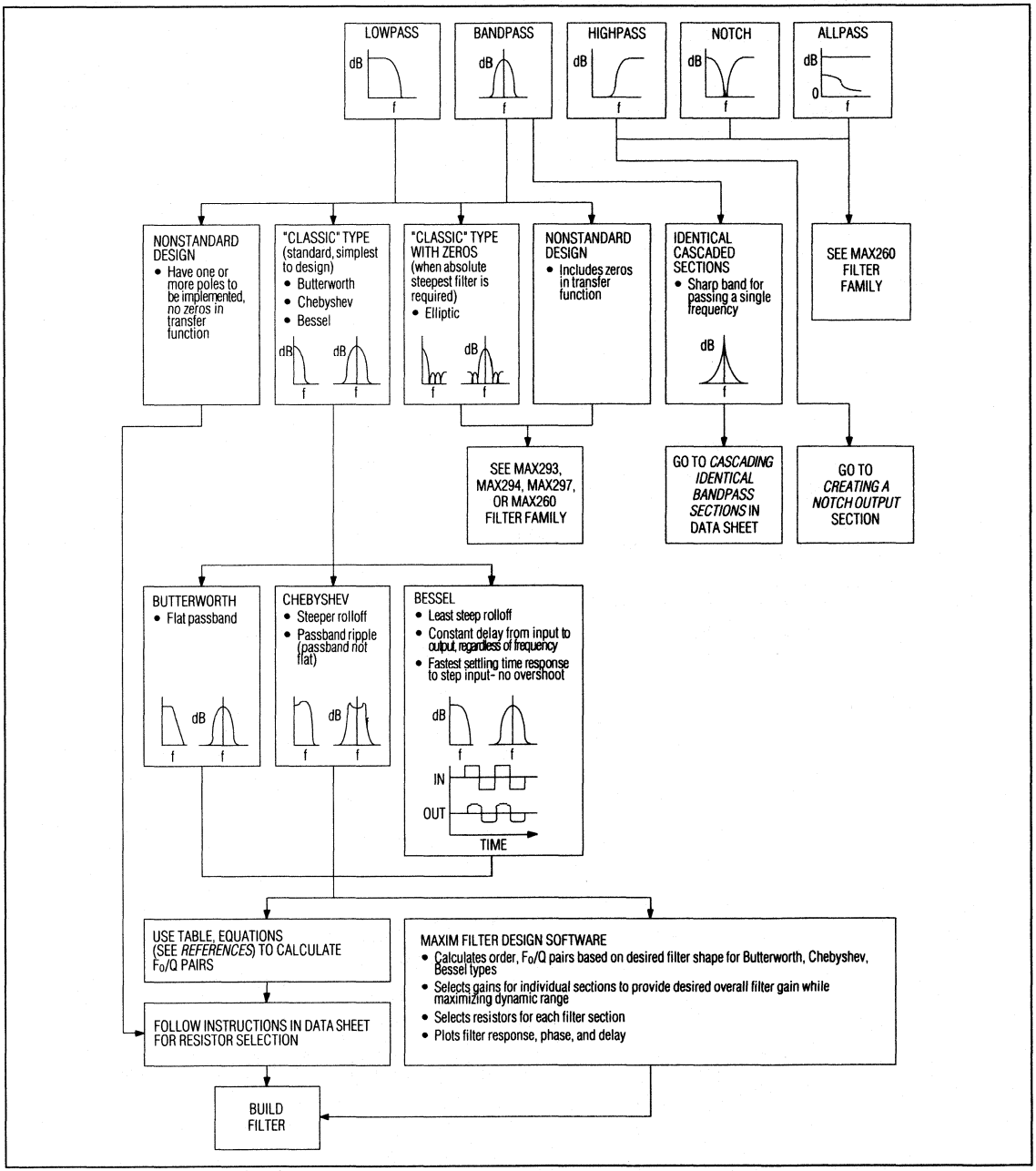


Figure 3. General Filter Design Flowchart

Translating Calculated F_o/Q Pairs into MAX274/MAX275 Hardware (Resistor Selection)

If the filter design procedure has been completed as outlined in Figure 3, with the exception of external resistor selection, follow these steps:

1. Check all F_o/Q pairs for realizability. The MAX274/MAX275 have limits on which F_o/Q values can be implemented. These limits are bound by finite amplifier gain-bandwidth and amplifier load drive capability (which limit the highest frequency F_o/highest Qs) as well as amplifier noise pickup and susceptibility to errors caused by stray capacitance (which sets a low-frequency limit on the poles). Refer to Figure 4 to be sure each F_o/Q pair is within the "realizable" portion of the graph. If filter Qs are too high, reduce them by increasing the filter order (that is, increase the number of poles in the overall filter).

High-frequency F_os (up to 400kHz) and high Qs outside of Figure 4's limits are also realizable, but F_o and Q will deviate significantly from the ideal. Adjust resistor values by prototyping.

To implement F_os less than 100Hz, see *High-Value Resistor Transformation* section.

2. Calculate resistor values for each section (F_o/Q pair). Calculate resistor values using graphs and equations in steps A through D of this section. Begin by estimating required values according to the graphs; then use the given equations to derive a precise value.

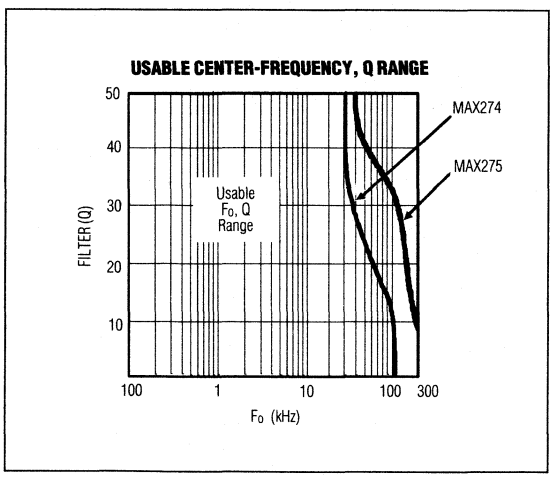


Figure 4. Usable F_o, Q Range. See Translating Fo/Q Pairs into Hardware (Resistor Selection).

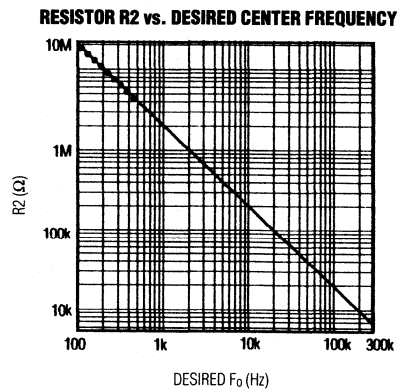
Resistor values should not exceed 4MΩ because parasitic capacitances shunting such high values cause excessive F_o/Q errors. Values lower than 5kΩ for R2 and R3 are not recommended due to limited amplifier output drive capability. For cases where larger values are unavoidable (as in low-frequency sections) refer to the *High-Value Resistor Transformation* section.

The Frequency Control (FC) pin is connected to V+, GND, or V- and scales R3 and R1 to accomodate a wide range of gains and Q values. Different FC settings may be chosen for each section. Refer to the *FC Pin Connection* section.

The steps for calculating resistor values are given below.

STEP A. CALCULATE R2.

$$R2 = \frac{(2 \times 10^9)}{F_o}$$



• • • USE RESISTOR "T-NETWORK" TO REDUCE VALUE
(SEE *HIGH-VALUE RESISTOR TRANSFORMATION* SECTION)

Resistors R2 and R4 set the center frequency.

STEP B. CALCULATE R4.

$$R4 = R2 - 5k\Omega$$

R4 may be less than 5kΩ because an internal series 5kΩ resistor limits BPO_ loading

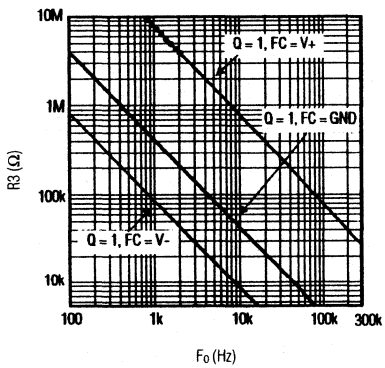
4th- and 8th-Order Continuous-Time Active Filters

STEP C. CALCULATE R3.

R3 sets the Q for the section. R3 values are plotted assuming Q = 1; since R3 is proportional to Q, multiply the graph's value by the desired Q.

Given Q, three choices exist for R3, depending on the FC setting. Choose a setting that provides a reasonable resistor value (5kΩ < R3 < 4MΩ). R3 > 4MΩ may be used if unavoidable – refer to the *High-Value Resistor Transformation* section for an explanation of resistor "Ts."

RESISTOR R3 vs. CENTER FREQUENCY



• • • USE RESISTOR "T-NETWORK" TO REDUCE VALUE (SEE *HIGH-VALUE RESISTOR TRANSFORMATION* SECTION)

Scale R3 to desired Q

$$R3 = \frac{(Q)\ (2X10^9)}{F_o} X \left(\frac{RX}{RY}\right)$$

CONNECT FC TO:	RX/RY
V+	4/1
GND	1/5
V-	1/25

STEP D. CALCULATE R1.

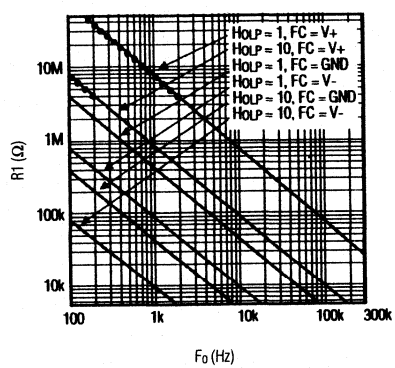
R1 sets the gain. If individual section gains have not yet been calculated, refer to *Cascaded Filter Gain Optimization, Ordering of Sections.*

R1 is inversely proportional to LP gain. R1 values for gains of 1 and 10 are plotted; scale R1 according to desired gain.

Lowpass Filters:

The FC pin setting was chosen in Step C (or from previous section calculations).

LP GAIN
RESISTOR R1 vs. FREQUENCY



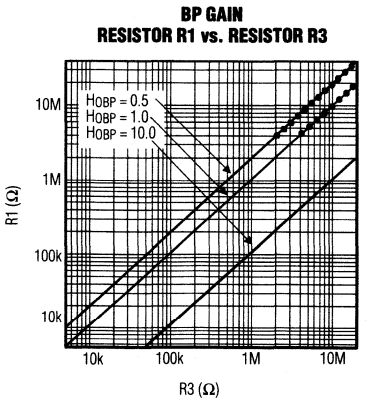
• • • USE RESISTOR "T-NETWORK" TO REDUCE VALUE (SEE *HIGH-VALUE RESISTOR TRANSFORMATION* SECTION)

$$R1 = \frac{(2)\ (10^9)}{(F_o)\ (H_{OLP})} X \left(\frac{RX}{RY}\right)$$

CONNECT FC TO:	RX/RY
V+	4/1
GND	1/5
V-	1/25

where H_{OLP} is the gain at LPO_ at DC.

Bandpass Filters:



• • • USE RESISTOR "T-NETWORK" TO REDUCE VALUE
(SEE *HIGH-VALUE RESISTOR TRANSFORMATION* SECTION)

$$R1 = \frac{R3}{H_{OBP}}$$

where H_{OBP} is the gain at BPO_ at F_O.

3. Recalculate resistor values to compensate for filter amplifier bandwidth errors. Some of the *Typical Operating Characteristics* graphs show deviations in F_O and Q compared with expected values, due to gain rolloff of the internal amplifiers. If desired, correct these deviations by recalculating values R1- R4.

4. Build a filter prototype. Build and test all filter designs! Refer to the Prototyping, PC-Board Layout section of this data sheet.

For applications that require high accuracy (for example, those with filter sections containing Qs greater than 10) or those that use a ground plane, a final prototype tuning procedure is recommended. Build a prototype filter; then adjust resistor values of each section until desired accuracy is achieved.

High-Value Resistor Transformation

High-value resistors (greater than 4MΩ) used in the MAX274/MAX275 filter circuit introduce excessive F_O and Q errors. To reduce the impedance of these feedback paths while maintaining equivalent feedback current, use the resistor "T" method shown in Figure 5.

F_Os less than 100Hz can be realized using T-networks. T-networks provide the equivalent of large resistor values for R2, R3, and R4, necessary for low-frequency filters; however, T-networks reduce dynamic range by attenuating the input signal level. Note that parasitic capacitances across these high resistor values affect the filter response at high frequencies. For best results, build a prototype and check its performance thoroughly.

Odd Number of Poles

For lowpass designs containing an odd number of poles, add an RC lowpass filter after the final filter section. The value of RC should be:

$$RC = 1/2\pi F_O$$

where F_O is the desired real pole frequency. If required, buffer the RC with an op amp.

In many cases it may be advantageous to simply increase the filter order by 1, and implement it with an additional 2nd-order section.

FC Pin Connection

Connect FC to GND for all applications, except where resistor values fall below 5kΩ (at high F_Os, low Qs). In these cases connect FC to V+. For low F_Os and high Qs, connect FC to V- to keep the value of R1 and R3 below 4MΩ.

F_O and Q errors are significantly higher when FC is connected to V+ or V- (see Typical Operating Characteristics). Adjusting resistor values compensates for these errors, since the errors are repeatable from part to part. Note that noise increases threefold when FC is connected to V+.

Cascading Identical Sections for Simplest Bandpass

If designing a bandpass filter where a single frequency (or a very narrow band of frequencies) must be passed, several 2nd-order sections with identical F_Os and Qs may be cascaded. The resulting Q (selectivity) of the filter is a function of the individual sections' Qs and the number of sections cascaded:

$$Q_t = \frac{Q}{\sqrt{2^{1/n} - 1}}$$

where Qt is the overall cascaded filter Q, Q is the Q of each individual section, and N is the number of sections.

4th- and 8th-Order Continuous-Time Active Filters

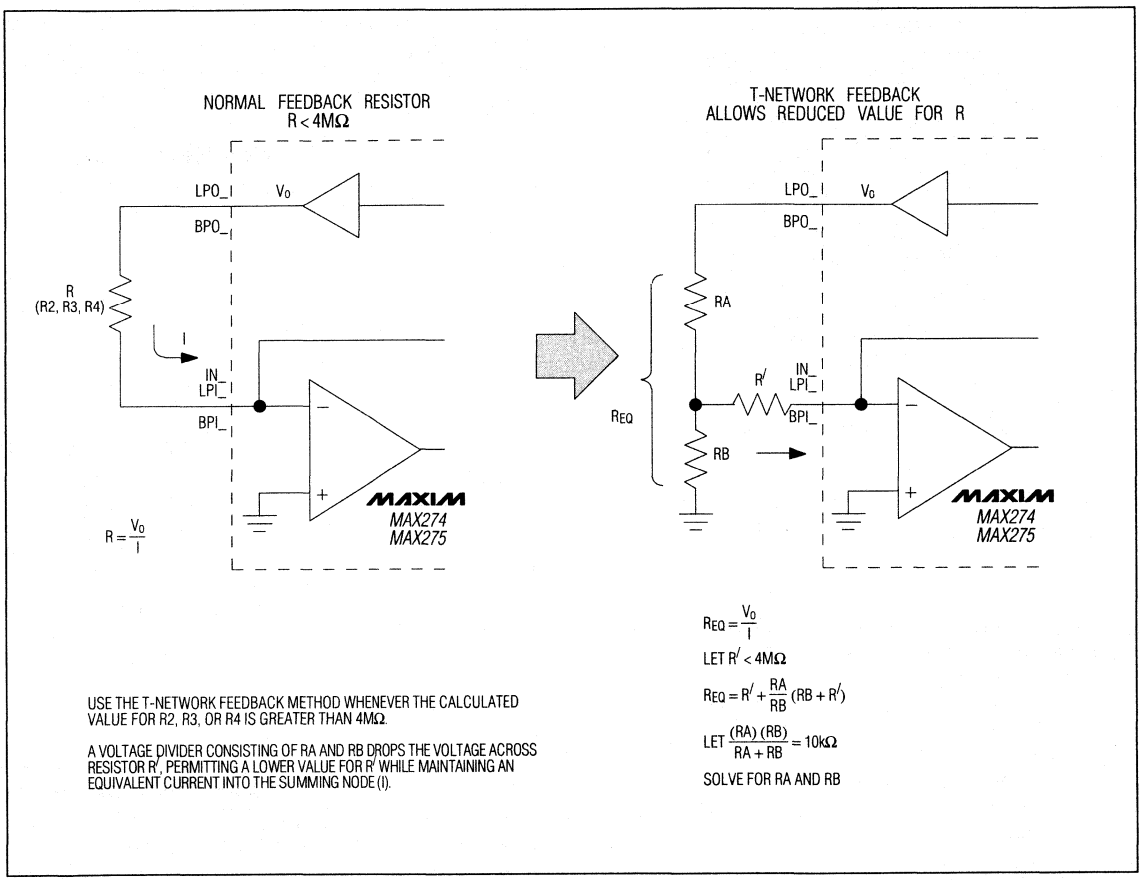


Figure 5. Resistor T-Networks Reduce Resistor Values

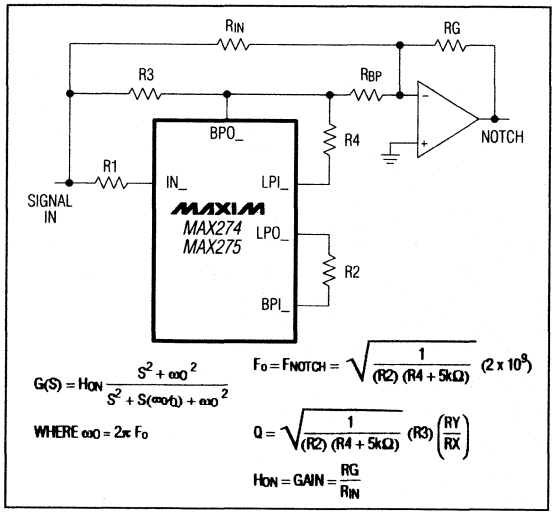


Figure 6a. Creating a Notch Output

Creating a Notch Output

A notch (zero) can be created in the filter response by summing the input signal with BPO_ using an external op amp (Figure 6a). The notch will have the poles and Q characteristics of the 2nd-order section, as well as a zero at the pole frequency (transfer function given in Figure 6a). H_{OBP} (BP gain at F_0) must be accurately set to unity so the input signal summed with BPO_ cancels precisely at the pole frequency. The notch's maximum attenuation is therefore a function of the accuracy of R1, R3, R_{IN}, and R_{BP}.

A notch can be used to create a null within the passband of a lowpass filter to reject specific frequencies (see *Applications* section).

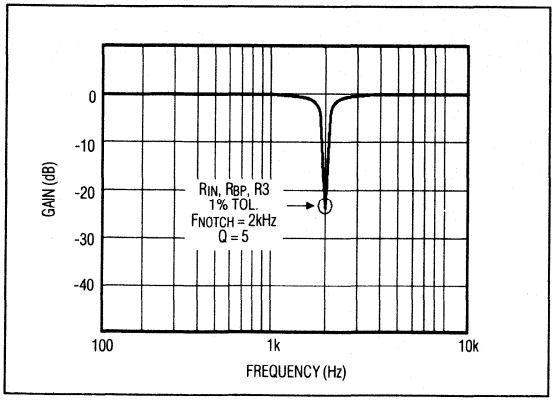


Figure 6b. Notch Response

Cascaded Filter Gain Optimization, Ordering of Sections

Gains across the individual sections in a filter may be set an infinite number of ways, as long as the total gain from filter input to output is correct. Often, gains cannot be equally divided among sections, since different F_0s and Qs create gain peaks and valleys at different frequencies for each section.

The goal in choosing gains is to prevent section outputs from swinging beyond the ±3.25V limit (using ±5V supplies) while the full input signal is applied. On the other hand, if section gains are set too low and only a small proportion of output range is used, the noise factor increases. An optimal gain distribution between sections allows each section to swing as close to ±3.25V as possible in a wide range of frequencies.

Check the unused output (BPO_ or LPO_), and the internal HP node for overvoltage, since clipping at any node will cause distortion at the outputs. The HP node is not available for probing (Figure 2); however, its gain may approach RX / R1. Low R1 values and connecting FC to V+ (which sets RX as high as 64kΩ) may cause this node to clip.

Maxim's Filter Design Software allows optimum gain by plotting output gains of each successive cascaded filter section, including the internal node. Gains may be adjusted manually and sections reordered for the best overall dynamic range.

To optimize gain without the help of software, begin by ordering the sections from lowest Q to highest Q. Divide gains equally between sections, setting each section gain to:

$$H_O = A^{(1/N)}$$

where A = overall filter gain

$H_O = H_{OBP}$ for bandpass designs (gain at F_0)

$H_O = H_{OLP}$ for lowpass designs (gain at DC)

N = total number of sections

This approach offers a good first-pass solution to clipping problems in the high Q sections by keeping gains low in the first (low Q) sections. The gains may then be adjusted in hardware to maximize overall dynamic range.

4th- and 8th-Order Continuous-Time Active Filters

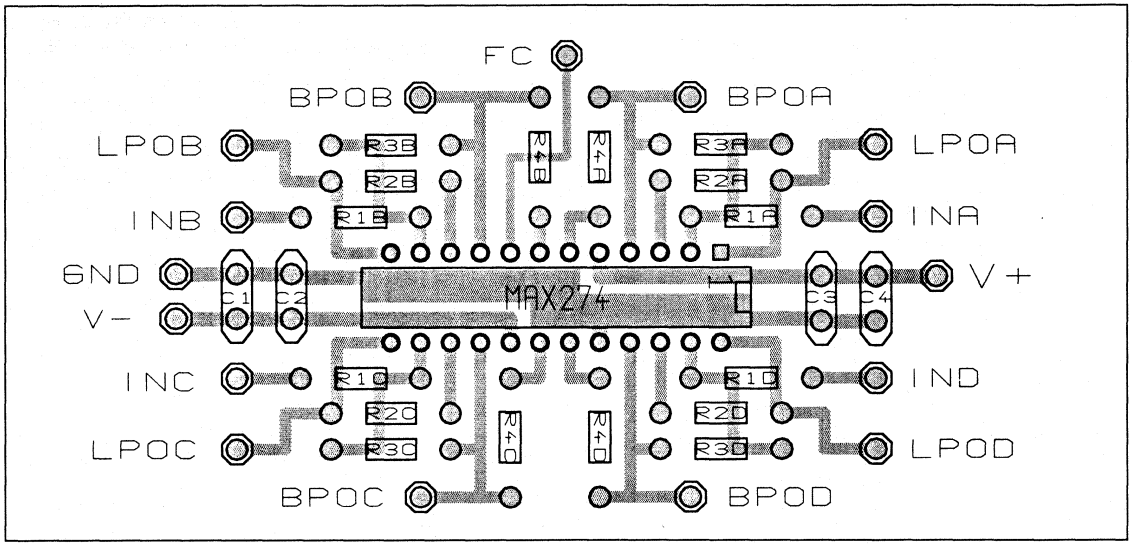


Figure 7a. MAX274 Suggested PC-Board Layout for DIP

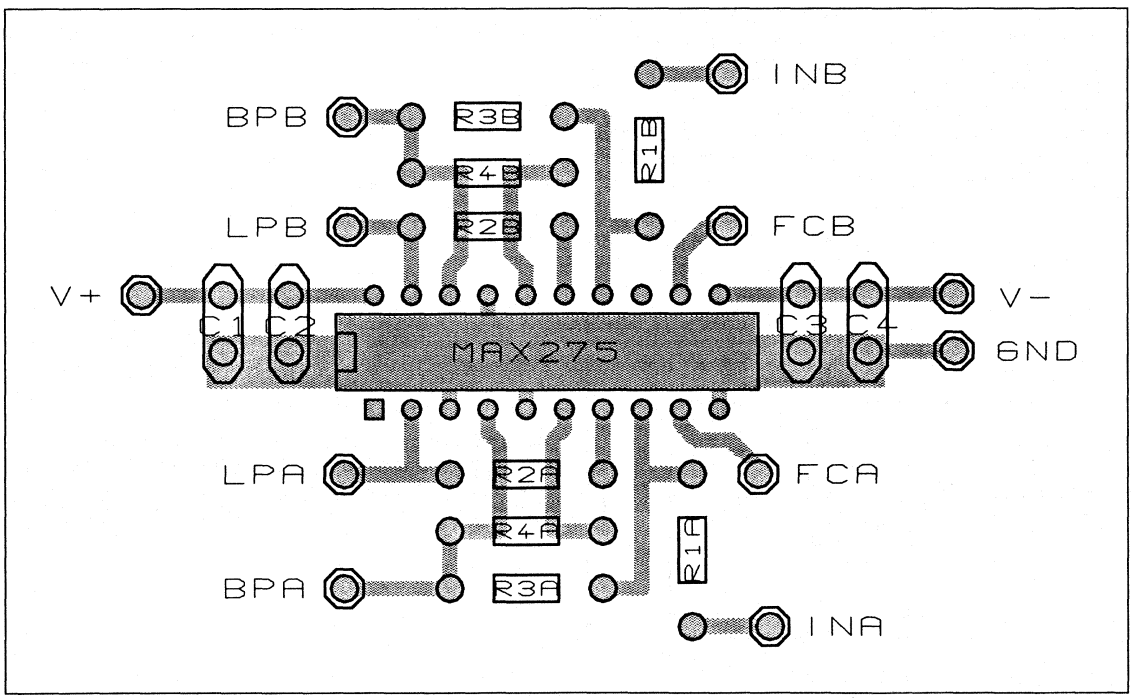


Figure 7b. MAX275 Suggested PC-Board Layout for DIP

Resistors

Aside from accuracy, the most important criterion for resistor selection is parasitic capacitance across the resistor. Typical capacitance should be less than 1pF. Precision wire-wound resistors exhibit several picofarads, as well as unacceptable inductance – DO NOT USE THESE. Capacitance effectively reduces the resistance at high frequencies (especially when using high-value resistors), and causes phase shifts in feedback loops. Do not mount resistors in sockets. Socket capacitance appearing across resistors is often several picofarads, and will cause significant errors in F_0 and Q. Metal-film resistors minimize noise better than carbon types.

Prototyping, PC-Board Layout

For highest accuracy filters, build the filter prototype on a PC board with a layout as similar as possible to the final production circuit. If a ground plane will be used in production, build prototype filters on a copper board. Do not use push-in type breadboards for prototyping – pin-to-pin capacitance is too high. For faster prototyping, the MAX274 evaluation kit includes a PC-board circuit to test designs.

Layout-sensitive errors, though repeatable from part to part, vary according to resistor placement, trace routing, and ground-plane layout. For highest accuracy, use the recommended layout provided in Figures 7a and 7b. Keep all traces, especially LPI_ and BPI_ , as short as possible. LPI_ and BPI_ are particularly sensitive to ground capacitance, and may cause errors in Q. If a ground plane is used, tune the prototype filter by adjusting resistor values to cancel errors caused by ground capacitance.

Prevent capacitive coupling between pins. Coupling between BPI_ and BPO_ can cause F_0 errors; capacitance across resistors connecting IN and BPO_ (R3), BPI_ and LPO_ (R2), and BPO_ and LPI_ (R4) cause F_0 and Q errors. Minimize these errors with "tight" (shortest trace) layout practices.

Measuring F_0 and Q

For multiple-order filters, measure each section individually, before cascading, to verify correct F_0 and Q. For best results, measure BPO_ with a spectrum analyzer. F_0 is the frequency at which the input and BPO_ are 180° out of phase. Q is the ratio of F_{PK} to BPO_'s - 3dB bandwidth (Figure 2), where F_{PK} is the frequency at which BPO_ gain is the greatest (which may not be equal to F_0).

Filter F_0 and Q Accuracy

F_0 sensitivity to external resistor tolerance is 1:1 – for example, use of 1% tolerant resistors for R2 and R4 adds ±1% error to F_0 (which should be added to the ±1% tolerance of the MAX274/MAX275, guaranteed over temperature). Q errors are of greater magnitude, since they are a function of the internal resistor divider (controlled by the FC pin) and also involve R3. Typical Q error distributions are given in the *Typical Operating Characteristics*; additional Q errors associated with resistor tolerances are a function of R2, R3, and R4, and must be calculated according to the values used.

DC Offset Removal

Figures 8a and 8b show methods for removing the DC offset voltage at LPO_. The first method shows adjustable DC nulling signals injected into either BPI_ or the filter input. R_{TRIM} must be adjusted until DC offset is nulled at the LPO_ (Figure 8a). Figure 8b shows a trimless solution for lowpass filters that removes DC offset by AC coupling the LPO_ output, while allowing a DC path through R from the input. At DC and low frequencies, the output is equal to the prefiltered signal input (across R); at higher frequencies, C conducts and the output equals the signal at LPO_. The external RC pole should be set at least one frequency decade lower than the overall filter F_0. A low offset amplifier can buffer the output signal, if desired. For bandpass filters, a simple buffered RC highpass filter at the output removes DC offset.

Noise and Distortion

Noise-spectral density is shown in the *Typical Operating Characteristics*. The noise frequency distribution is shaped by the filter gain and response (higher Q section will have a proportionally higher noise peak around the pole frequency), as well as by amplifier 1/f noise. With FC set to V+, noise is 3 times greater than if set to GND or V-; therefore, avoid this setting for noise-sensitive applications. The noise density graphs from the *Typical Operating Characteristics* can be scaled to any gain or Q for an accurate noise estimation.

The MAX274/MAX275 can drive 5kΩ loads to typically within ±500mV of the supply rails with negligible distortion. The outputs can drive up to 100pF; however, filters with high F_0s and Qs will undergo some phase shift (1° at 100kHz driving 130pF, F_0 = 100kHz, Q = 10 section).

4th- and 8th-Order Continuous-Time Active Filters

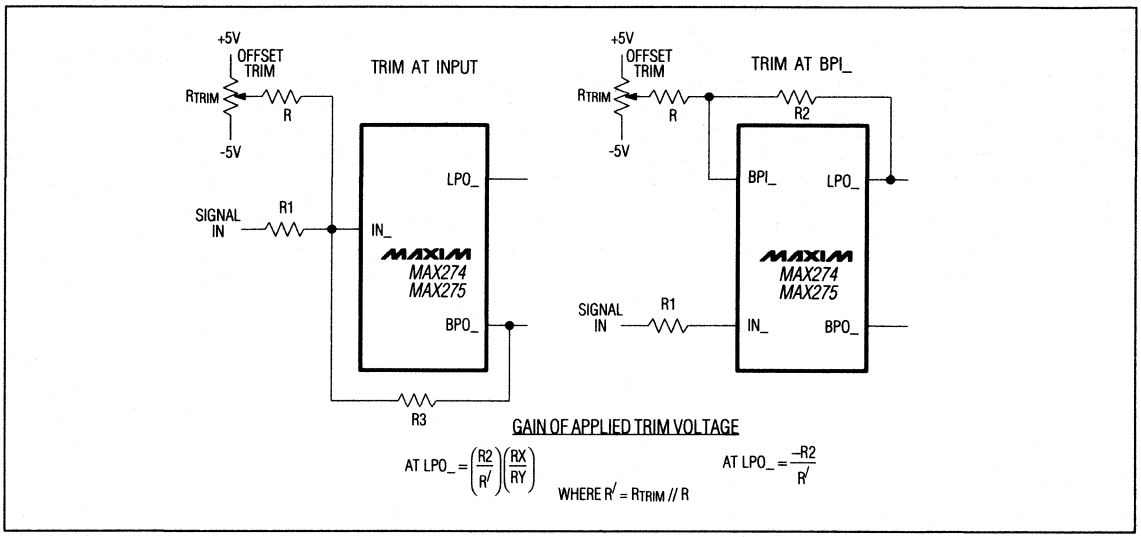


Figure 8a. Trimmed Offset Removal

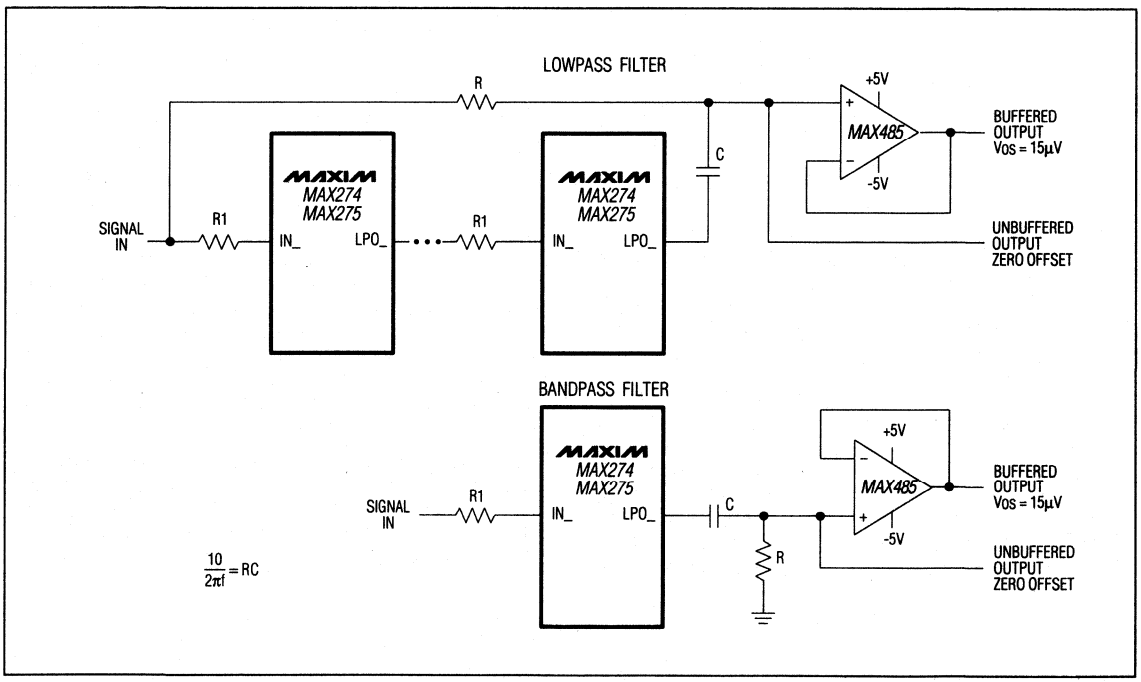


Figure 8b. Trimless Offset Removal

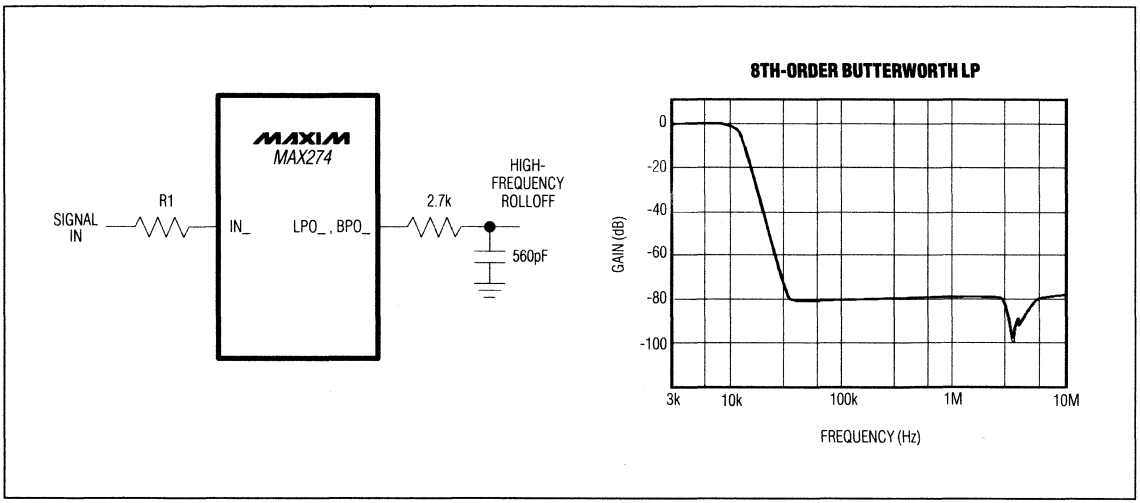


Figure 10. External RC Lowpass for High-Frequency Rolloff

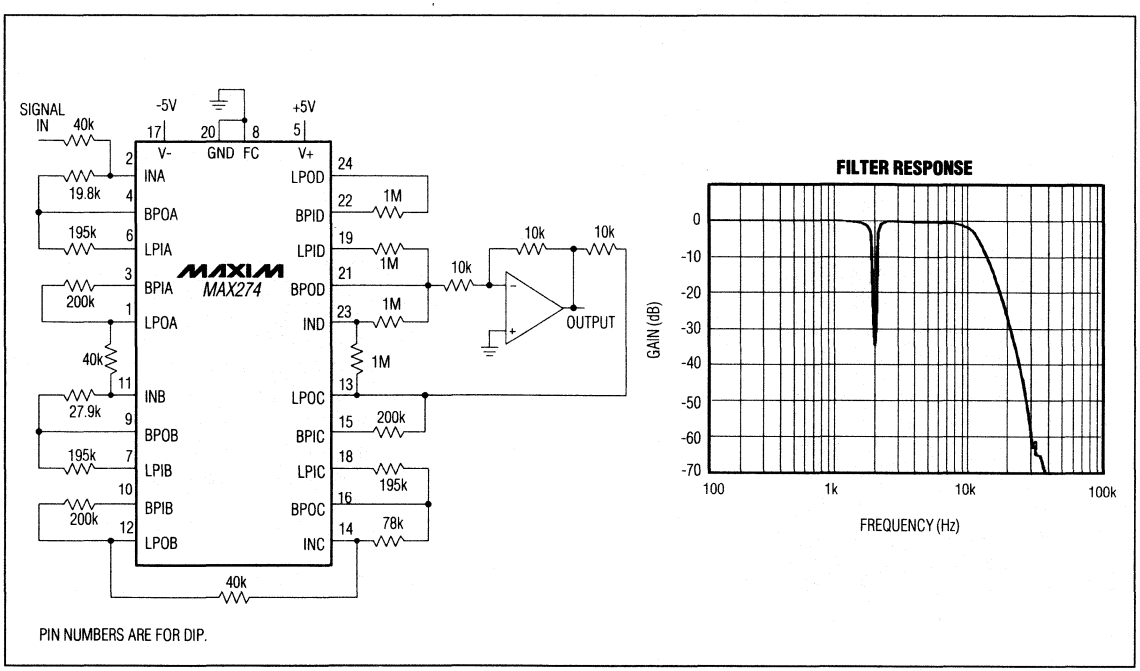


Figure 11. 10kHz 6th-Order Butterworth Lowpass Filter with 2kHz Notch (MAX274)

4th- and 8th-Order Continuous-Time Active Filters

Applications (continued)

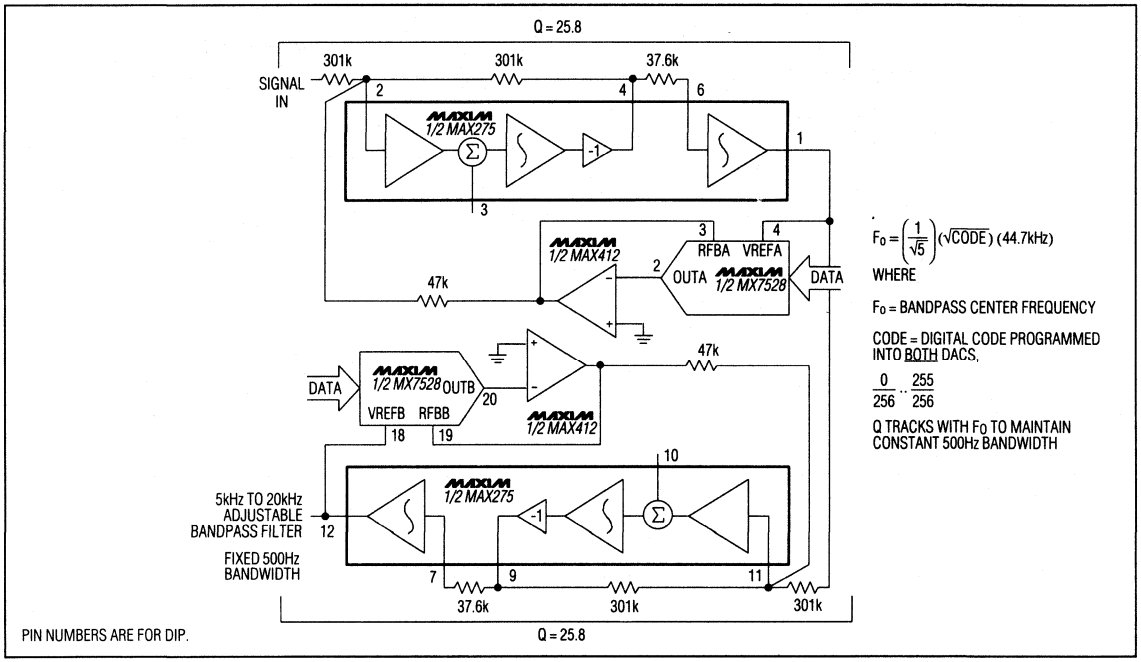
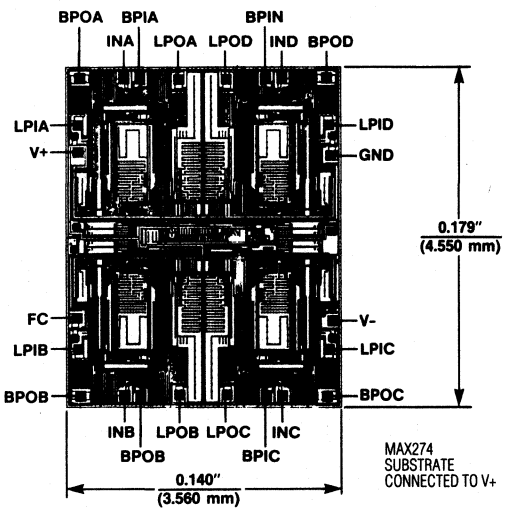
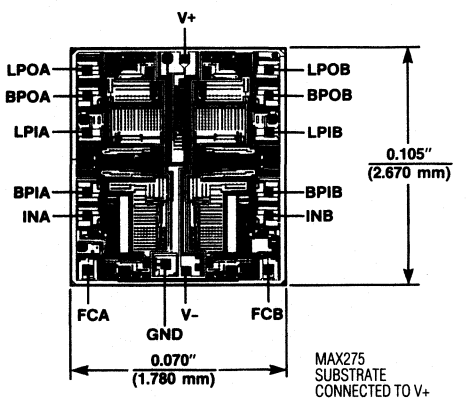


Figure 12. Programmable Bandpass Filter (MAX275)

Chip Topographies





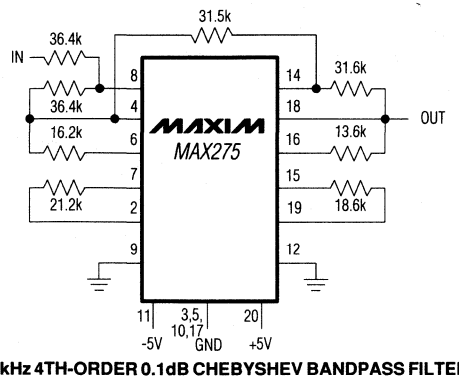
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX274AENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX274BENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX274AEWI	-40°C to +85°C	28 Wide SO
MAX274BEWI	-40°C to +85°C	28 Wide SO
MAX274AMRG	-55°C to +125°C	24 CERDIP**
MAX274BMRG	-55°C to +125°C	24 CERDIP**
MAX274EV KIT-DIP	0°C to +70°C	Plastic DIP – Through Hole
MAX274_SOFT	—	MAX274/MAX275 Design Software
MAX275ACPP	0°C to +70°C	20 Plastic DIP
MAX275BCPP	0°C to +70°C	20 Plastic DIP
MAX275ACWP	0°C to +70°C	20 Wide SO
MAX275BCWP	0°C to +70°C	20 Wide SO
MAX275BC/D	0°C to +70°C	Dice*
MAX275AEPP	-40°C to +85°C	20 Plastic DIP
MAX275BEPP	-40°C to +85°C	20 Plastic DIP
MAX275AEWP	-40°C to +85°C	20 Wide SO
MAX275BEWP	-40°C to +85°C	20 Wide SO
MAX275AMJP	-55°C to +125°C	20 CERDIP**
MAX275BMJP	-55°C to +125°C	20 CERDIP**
MAX274_SOFT	—	MAX274/MAX275 Design Software

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

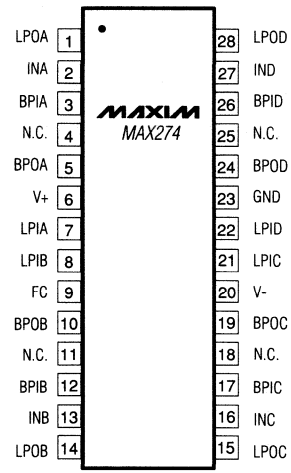
Typical Operating Circuits (continued)



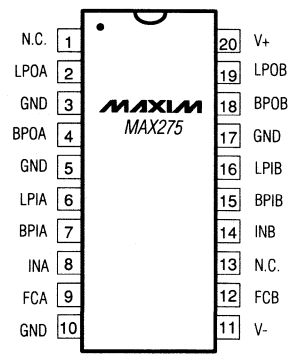
100kHz 4TH-ORDER 0.1dB CHEBYSHEV BANDPASS FILTER
PIN NUMBERS ARE FOR DIP

Pin Configurations (continued)

TOP VIEW



WIDE SO



DIP/SO

4th- and 8th-Order Continuous-Time Active Filters

Power Supplies

The MAX274/MAX275 can be operated from a single power supply or dual supplies (Figure 9). V+ and V- pins must be properly bypassed to GND with 4.7µF electrolytic (tantalum preferred) and 0.1µF ceramic capacitors in parallel. These should be as close as possible to the chip supply pins.

For single-supply applications, GND must be centered between V+ and V- voltages so signals remain in the common-mode range of the internal amplifiers.

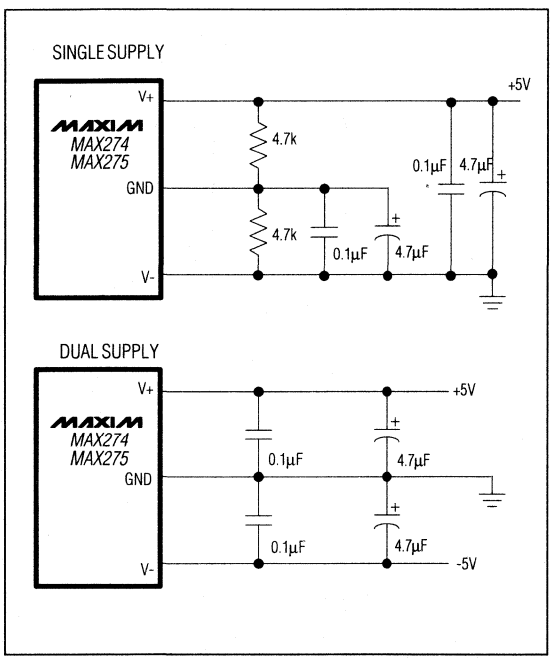


Figure 9. Power-Supply Configurations

Software General Desciption

Maxim's filter software reduces the time required to design a continuous-time lowpass or bandpass filter using the MAX274 or MAX275. Starting from your basic filter requirements, using a "spreadsheet-style" format, the software calculates order, poles and Qs of classic filter types (Butterworth, Chebyshev, or Bessel), and resistor values required to implement the desired filter response.

For hardware prototyping with the MAX274, the MAX274 evaluation kit is recommended, which includes a PC board and a MAX274 IC.

Features

- **Calculates filter order, poles, and Qs from your filter requirements.**
- **Plots filter responses – gain, phase, and group delay – for inspection BEFORE you build the filter.**
- **Calculates resistor values used to obtain desired filter response using the MAX274 or MAX275.**

Ordering Information

PART	DISK TYPE
MAX274SOFT	5¼" Floppy
MAX275SOFT	5¼" Floppy

In the USA and Canada, order directly from Maxim (1-800-998-8800). In other countries, call your local Maxim representative.

Software Operation

NOTE: CHECK FILE "README.DOC" FOR IMPORTANT CHANGES.

Installation

You will need an IBM-compatible PC, DOS version 2.0 or later with a 5¼" floppy disk drive, and one of the following video displays: Hercules graphics, CGA, EGA, VGA, or compatible. Either a hard drive or an additional floppy drive is also required.

To install the program, insert the floppy into your disk drive and type "A: INSTALL" (or B:INSTALL). Follow the instructions on the screen. After installation, type "FILTER" to start the program. Be sure you are in the drive/directory where the software is installed.

Help

After installing the software, print a hard copy of the file FILTER.HLP by entering "TYPE FILTER.HLP > PRN" from DOS. This collection of help screens serves as the instruction manual for operating the software. Individual help screens may be printed while running the software by pressing F1, then following the instructions on the screen.

References

The following references contain information and tables to aid in filter designs:

Carson, Chen. *Active Filter Design*, Hayden, 1982.

Tedeschi, Franck. *Active Filter Cookbook*, Tab Books No 1133, 1979.

Hilburn, Johnson. *Manual of Active Filter Design*, McGraw Hill, 1973.

German Language:

U. Tietze; Ch. Schenk. *Halbleiter-Schaltungstecknik Springer-Verlag*, Berlin Heidelberg, New York/Tokyo 1991.

4th- and 8th-Order Continuous-Time Active Filters

EV Kit General Description

The MAX274 Evaluation Kit (EV Kit) shrinks the time required to design and implement a continuous-time lowpass or bandpass filter by providing a software design tool and a prototyping PC board complete with a MAX274 8th-order, continuous-time filter IC. Starting from your basic filter requirements, Maxim's Filter Design Software calculates filter order, poles, and Qs of classic filter types (Butterworth, Chebyshev, or Bessel), then calculates resistor values required to implement the complete filter. Installing these resistors on the PC board provided and cascading the required number of sections of the MAX274 filter yields a complete filter — ready for testing — eliminating the need for expensive and time-consuming prototyping. The MAX274 PC board layout may be incorporated directly in production PC boards for absolutely consistent results from prototype to production.

Feature

- **Allows You to Design and Build Lowpass or Bandpass Filters**
- **Pole Frequencies (Fo) from 100Hz to 150kHz**
- **Kit Supports Butterworth, Chebyshev, and Bessel Designs**
- **Includes Design Software:**
  - **Calculates filter order, poles, and Qs from your filter requirements**
  - **Plots filter responses — gain, phase, and group delay — for inspection BEFORE you build the filter**
  - **Calculates resistor values needed to build filter**
- **Includes PC Board for Evaluation:**
  - **PC board allows you to build filters immediately — simply install proper resistor values on board**
  - **Build up to 8th-order filters by cascading the four second-order sections — or use sections individually for multiple filters**
  - **Operates from single +5V or dual 5V supplies**

EV Kit

Figure 1. The MAX274 EV kit includes filter design software, PC board with MAX274 IC, and full documentation.

Ordering Information

PART	TEMP. RANGE	BOARD TYPE
MAX274EVKIT	0°C to +70°C	Plastic DIP – Through Hole

Component List

QUANTITY	COMPONENT	SYMBOL
1	MAX274ACNG Filter IC	None
1	MAX274 Filter Circuit PC Board	None
2	BNC Screw-In Connectors	None
3	Banana Jacks	None
4	Standoffs, 4-40 Screws	None
2	10µF/16V Dipped Tantalum Capacitors	C1, C4 or CS1
2	0.1µF Ceramic Capacitors	C2, C3
1	Filter Design Software on 5 1/4" Floppy Disk	None

4th- and 8th-Order Continuous-Time Active Filters

Filter Design Software

NOTE: CHECK FILE "README.DOC" FOR IMPORTANT CHANGES

Installation

You will need an IBM-compatible PC, DOS version 2.0 or later, with a 5 1/4" floppy disk drive, and one of the following video displays: Hercules graphics, CGA, EGA, VGA or compatible. Either a hard drive or an additional floppy drive is also required.

To install the program, insert the floppy into your disk drive and type "A:INSTALL" (or "B:INSTALL"). Follow the instructions on the screen. After installation, type "FILTER" to start the program. Be sure you are in the drive/directory where the software is installed.

Help

After installing the software, print a hard copy of the file FILTER.HLP by entering TYPE FILTER.HLP > PRN from DOS. This collection of help screens serves as the instruction manual for operating the software. Individual help screens may be printed while running the software by pressing F1, then following instructions on the screen.

Assembly Instructions

1. Install BNC connectors and banana jacks as shown in Figure 2. Connect wires from the V+, GND, and V- jacks to the nodes designated V+, GND, and V- on the circuit. Install MAX274 IC as shown (or install an IC socket if desired).
2. Install filter feedback resistors (R1A-R4A, R1B-R4B, R1C-R4C, R1D-R4D). The values of these resistors depend on the particular filter being built, and can be calculated from the data sheet or with the aid of Maxim's Filter Design Software. All resistors except RS1 and RS2 should be either carbon or metal-film type (not wire-wound).

   If using resistor T-networks (described in the *High-Value Resistor Transformation* section of the MAX274 data sheet — denoted as R5_ - R10_ in the filter software), perform the following:

   On the PC board, scratch off the green soldermask from the ground trace (Figure 2). Where required, substitute each normal resistor connection (R2, R3, or R4) with three T-network resistors on the underside of the board, using jumper wire to connect the T-network ground connection with the ground trace on the PC board (Figure 3).

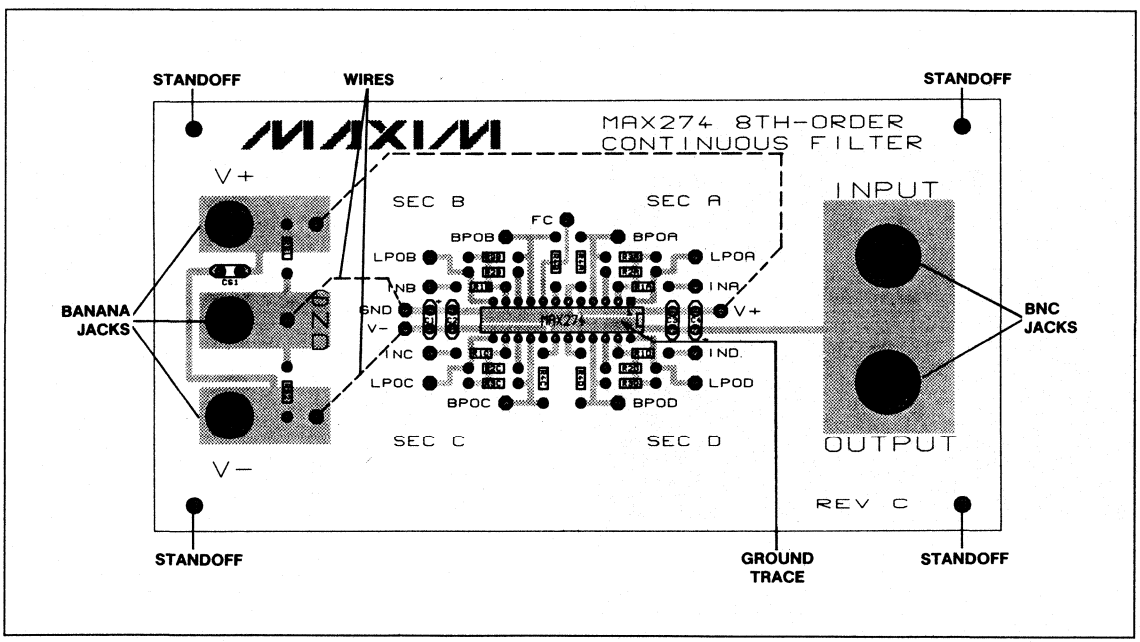


Figure 2. MAX274 EV Kit Component Placement Diagram

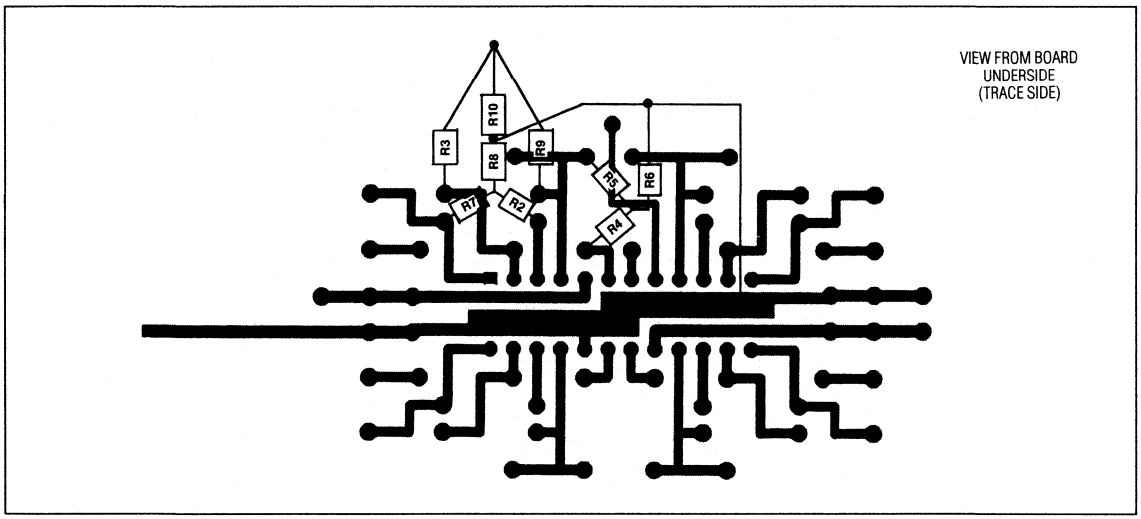


Figure 3. T-Network PC Board Connections

Recommended Resistor Sources

AVAILABLE TOLERANCES	TYPE	MANUFACTURER
1%, 0.1%, Others 5-100ppm/°C	Metal Film PTF Series	Dale 402-371-0800 FAX: 402-644-4206
1%, 0.1%	Surface Mount RN73H2B RN73E2B	KOA Speer 814-362-5536 FAX: 814-362-8883
1%, 0.1% to 2ppm/°C	PR, RL Series	Precision Resistive Products 319-394-9131 FAX: 319-394-9280

3. BE SURE IC IS INSTALLED ON BOARD BEFORE POWER IS APPLIED. Single +5V or +10V operation: Install RS1 and RS2 (both 4.7kΩ). Install C1, C2, and CS1 - omit C3 and C4. Apply positive supply to V+, supply ground to V-. Do not connect any supply to GND. For dual supply (5V) operation, omit RS1 and RS2, and apply positive supply, negative supply, and ground to V+, V-, and GND respectively.
4. Perform a frequency-response test for each filter section used (A,B,C, and D) to verify F_O/Q accuracy, before connecting them in series (cascading). For highest-accuracy results, perform frequency-response tests using a spectrum analyzer. Use the F_O and Q measurement techniques described in the MAX274 data sheet in the *Measuring F_O and Q* section. These methods apply to both lowpass and bandpass designs.

To measure filter section A's F_O and Q, apply the test sweep signal at INA, measure BPOA. F_O is the frequency at which INA and BPOA are exactly 180° out of phase. Q is determined by the formula:

Q = FPK/-3dB bandwidth

where FPK is the frequency at which the gain at BPOA is greatest (this may not be equal to F_O); and the -3dB bandwidth is the difference between the two frequencies at which BPOA is attenuated by 3dB from its peak gain. Repeat these measurements for filter sections B, C, and D. For more information, refer to Figure 2 of the MAX274 data sheet, *Bandpass Output.*

If the filter operates from a single supply, signals applied to the filters must be "centered" between V+ and V- so that signals remain in the common-mode range of the internal amplifiers.

5. Cascade the filter sections (connect them in series) to produce the desired filter response. For example, for an 8th-order bandpass filter, use jumper wires to connect BPOA to INB, BPOB to INC, and BPOC to IND. Apply the signal input at INA; the filter output is taken at OUTD. If desired, connect the INPUT and OUTPUT BNC connectors to the input and output of the cascaded filter using jumper wires. For lowpass filters, cascade the sections using LPO_ as the outputs. For lower-order filters, omit unused sections; for higher than 8th-order filters, order additional MAX274 PC boards from Maxim to add the required number of sections.

19-4526; Rev 0; 1/92

MAXIM

8th-Order, Lowpass, Switched-Capacitor Filters

General Description

The MAX291/292/295/296 are easy-to-use, 8th-order, lowpass, switched-capacitor filters that can be set up with corner frequencies from 0.1Hz to 25kHz (MAX291/MAX292) or 0.1Hz to 50kHz (MAX295/MAX296).

The MAX291/MAX295 Butterworth filters provide maximally flat passband response, and the MAX292/MAX296 Bessel filters provide low overshoot and fast settling. All four filters have fixed responses, so the design task is limited to selecting the clock frequency that controls the filter's corner frequency.

An external capacitor is used to generate a clock using the internal oscillator, or an external clock signal can be used. An uncommitted operational amplifier (noninverting input grounded) is provided for building a continuous-time lowpass filter for post-filtering or anti-aliasing.

Produced in 8-pin DIP and SO packages, and requiring a minimum of external components, the MAX291 series delivers very aggressive performance from a tiny area.

Applications

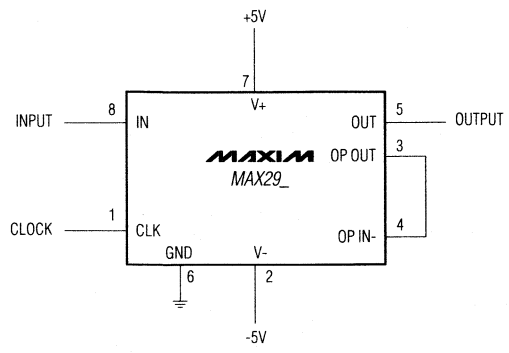
ADC Anti-Aliasing Filter

Noise Analysis

DAC Post-Filtering

50Hz/60Hz Line-Noise Filtering

Typical Operating Circuit



Pin configuration is 8-pin DIP/SO.

Features

- ♦ **8th-Order Lowpass Filters:**
  Butterworth (MAX291/MAX295)
  Bessel (MAX292/MAX296)
- ♦ **Clock-Tunable Corner-Frequency Range:**
  0.1Hz to 25kHz (MAX291/MAX292)
  0.1Hz to 50kHz (MAX295/MAX296)
- ♦ **No External Resistors or Capacitors Required**
- ♦ **Internal or External Clock**
- ♦ **Clock to Corner Frequency Ratio:**
  100:1 (MAX291/MAX292)
  50:1 (MAX295/MAX296)
- ♦ **Low Noise: -70dB THD + Noise (Typ)**
- ♦ **Operate with a Single +5V Supply or Dual ±5V Supplies**
- ♦ **Uncommitted Op Amp for Anti-Aliasing or Clock-Noise Filtering**
- ♦ **8-Pin DIP and SO Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX291CPA	0°C to +70°C	8 Plastic DIP
MAX291CSA	0°C to +70°C	8 SO*
MAX291CWE	0°C to +70°C	16 Wide SO
MAX291C/D	0°C to +70°C	Dice**
MAX291EPA	-40°C to +85°C	8 Plastic DIP
MAX291ESA	-40°C to +85°C	8 SO*
MAX291EWE	-40°C to +85°C	16 Wide SO
MAX291MJA	-55°C to +125°C	8 CERDIP***
MAX292CPA	0°C to +70°C	8 Plastic DIP
MAX292CSA	0°C to +70°C	8 SO*
MAX292CWE	0°C to +70°C	16 Wide SO
MAX292C/D	0°C to +70°C	Dice**

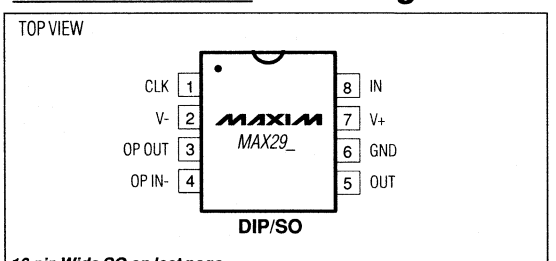
Ordering Information continued on last page.

** Contact factory for availability.*

*** Contact factory for dice specifications.*

**** Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



16-pin Wide SO on last page

8th-Order, Lowpass, Switched-Capacitor Filters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-) 12V
Input Voltage at Any Pin ..... V- + (-0.3V) ≤ V_{IN} ≤ V+ +(0.3V)
Continuous Power Dissipation
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) .. 727mW
8-Pin SO (derate 5.88mW/°C above +70°C) 471mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) .. 762mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX29_C__ ..... 0°C to +70°C
MAX29_E__ ..... -40°C to +85°C
MAX29_MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, filter output measured at OUT pin, 20kΩ load resistor to ground at OUT and OP OUT, f_{CLK} = 100kHz (MAX291/MAX292) or f_{CLK} = 50kHz (MAX295/MAX296), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS						
Corner-Frequency Range	MAX291/MAX292			0.1-25k		Hz
	MAX295/MAX296			0.1-50k		
Clock to Corner Frequency Ratio	MAX291/MAX292			100:1		
	MAX295/MAX296			50:1		
Clock to Corner Frequency Tempco	MAX291			10		ppm/°C
	MAX292			40		
	MAX295			5		
	MAX296			60		
Insertion Gain Relative to DC Gain	MAX291	f_{IN} = 0.50 F_O		-0.02	-0.1	dB
		f_{IN} = 1.00 F_O	-2.2	-2.7	-3.2	
		f_{IN} = 2.00 F_O	-43.0	-48.0		
		f_{IN} = 3.00 F_O	-70.0	-76.0		
	MAX292	f_{IN} = 0.25 F_O	-0.1	-0.2	-0.3	
		f_{IN} = 0.50 F_O	-0.6	-0.8	-1.0	
		f_{IN} = 1.00 F_O	-2.7	-3.0	-3.3	
		f_{IN} = 2.00 F_O	-11.0	-13.0	-15.0	
		f_{IN} = 3.00 F_O	-30.0	-34.0		
		f_{IN} = 4.00 F_O	-47.0	-51.0		
		f_{IN} = 6.00 F_O	-74.0	-78.0		
	MAX295	f_{IN} = 0.50 F_O		-0.02	-0.1	
		f_{IN} = 1.00 F_O	-2.2	-2.7	-3.2	
		f_{IN} = 2.00 F_O	-43.0	-48.0		
		f_{IN} = 3.00 F_O	-70.0	-76.0		
	MAX296	f_{IN} = 0.25 F_O	-0.1	-0.2	-0.3	
		f_{IN} = 0.50 F_O	-0.6	-0.8	-1.0	
		f_{IN} = 1.00 F_O	-2.7	-3.0	-3.3	
		f_{IN} = 2.00 F_O	-11.0	-13.0	-15.0	
		f_{IN} = 3.00 F_O	-30.0	-34.0		
		f_{IN} = 4.00 F_O	-47.0	-51.0		
		f_{IN} = 6.00 F_O	-74.0	-78.0		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, filter output measured at OUT pin, 20kΩ load resistor to ground at OUT and OP OUT, f_{CLK} = 100kHz (MAX291/MAX292) or f_{CLK} = 50kHz (MAX295/MAX296), T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output DC Swing		±4			V
Output Offset Voltage	IN = GND		±150	±400	mV
DC Insertion Gain Error with Output Offset Removed		0.15	0	-0.15	dB
Total Harmonic Distortion plus Noise	T_A = +25°C, f_{CLK} = 100kHz		-70		dB
Clock Feedthrough	f_{CLK} = 100kHz		6		mVp-p
CLOCK					
Internal Oscillator Frequency	C_{OSC} = 1000pF	29	35	43	kHz
Internal Oscillator Current Source/Sink	V_{CLK} = 0V or 5V		±70	±120	µA
Clock Input (Note 1) High		4.0			V
Low				1.0	
UNCOMMITTED OP AMP					
Input Offset Voltage			±10	±50	mV
Output DC Swing		±4			V
POWER REQUIREMENTS					
Supply Voltage Dual Supply		±2.375		±5.500	V
Single Supply	V- = 0V, GND = V+/2	4.750		11.000	
Supply Current	V+ = 5V, V- = -5V, V_{CLK} = 0V to 5V		15	22	mA
	V+ = 2.375V, V- = -2.375V, V_{CLK} = -2V to 2V		7	12	

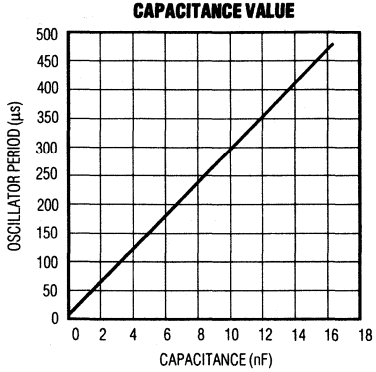
Note 1: Guaranteed by design.

6

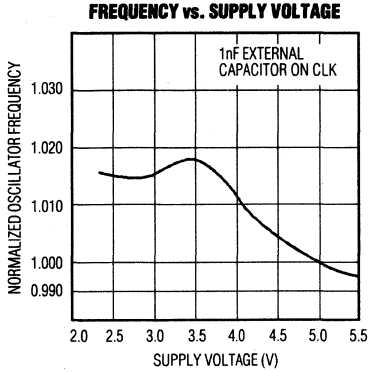
Typical Operating Characteristics

(V+ = 5V, V- = -5V, T_A = +25°C, f_{CLK} = 100kHz (MAX291/MAX292) or f_{CLK} = 50kHz (MAX295/MAX296), unless otherwise noted.)

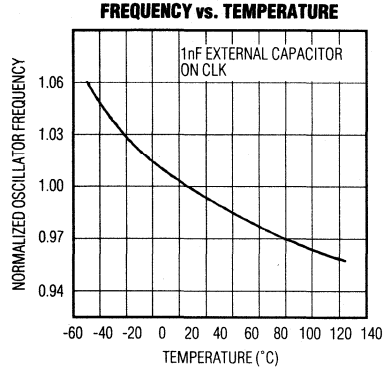
INTERNAL OSCILLATOR PERIOD vs. CAPACITANCE VALUE



NORMALIZED INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



NORMALIZED INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE

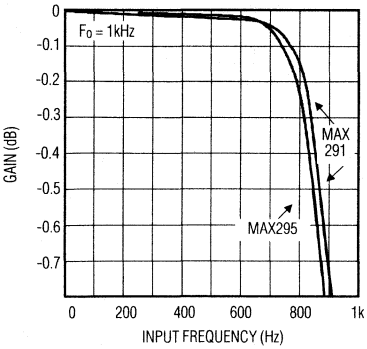


8th-Order, Lowpass, Switched-Capacitor Filters

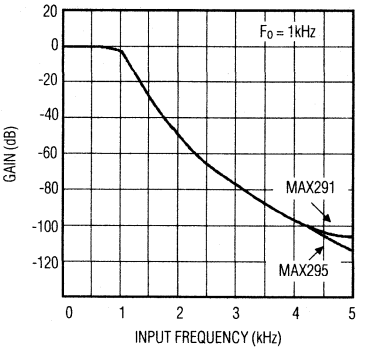
Typical Operating Characteristics (continued)

(V+ = 5V, V- = -5V, T_A = +25°C, f_{CLK} = 100kHz (MAX291/MAX292) or f_{CLK} = 50kHz (MAX295/MAX296), unless otherwise noted.)

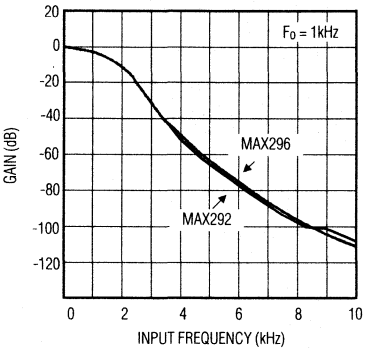
MAX291/MAX295 FREQUENCY RESPONSE



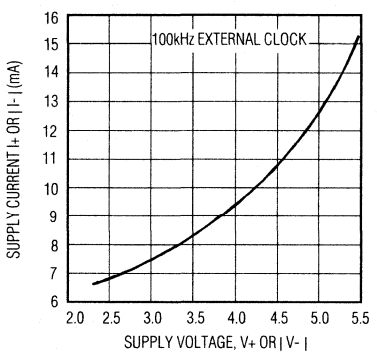
MAX291/MAX295 FREQUENCY RESPONSE



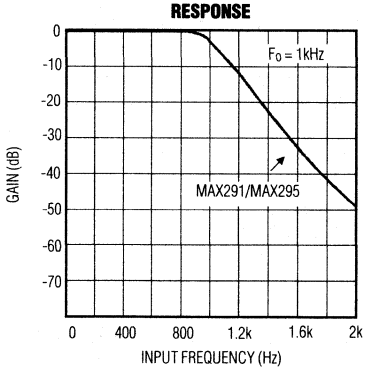
MAX292/MAX296 FREQUENCY RESPONSE



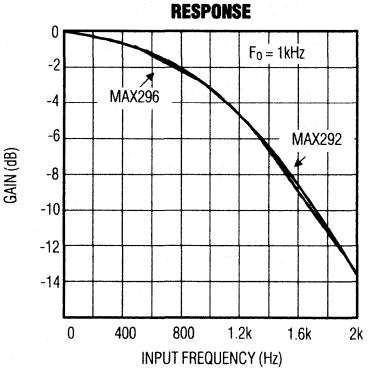
SUPPLY CURRENT vs. SUPPLY VOLTAGE



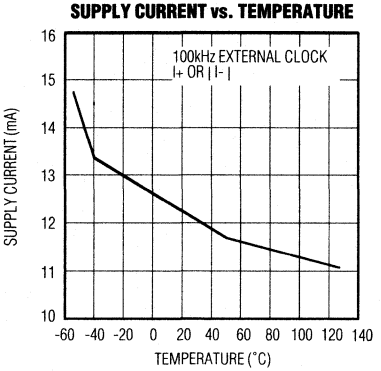
MAX291/MAX295 FREQUENCY RESPONSE



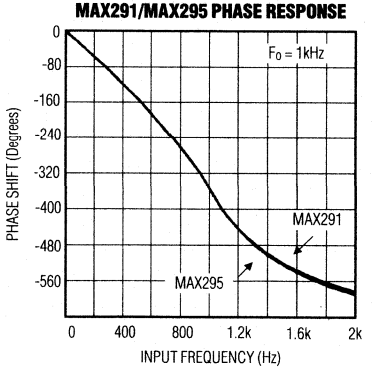
MAX292/MAX296 FREQUENCY RESPONSE



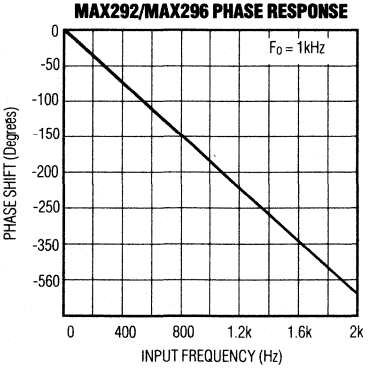
SUPPLY CURRENT vs. TEMPERATURE



MAX291/MAX295 PHASE RESPONSE



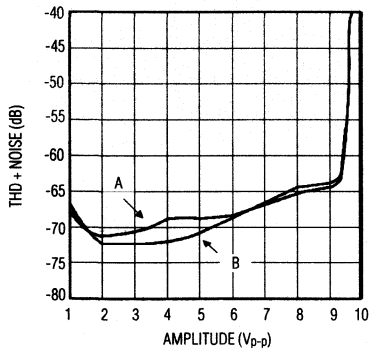
MAX292/MAX296 PHASE RESPONSE



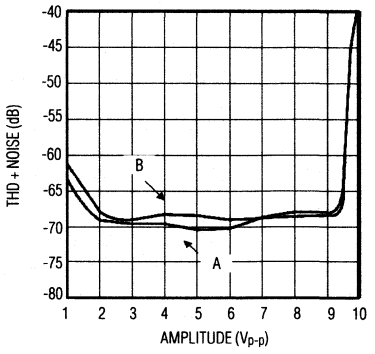
Typical Operating Characteristics

(V+ = 5V, V- = -5V, R_{LOAD} = 5kΩ, T_A = +25°C, unless otherwise noted.)

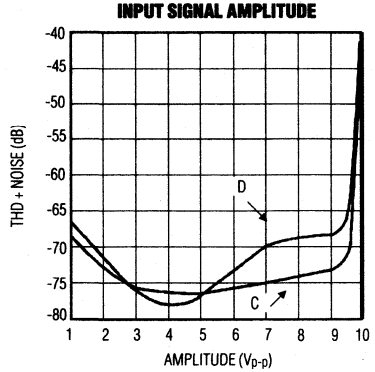
MAX291 THD + NOISE vs. INPUT SIGNAL AMPLITUDE



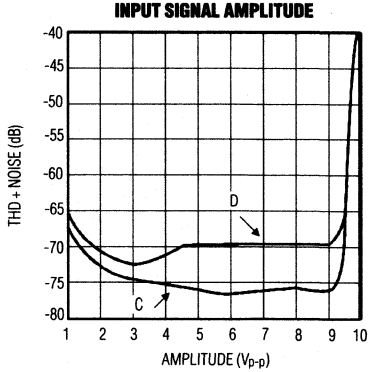
MAX292 THD + NOISE vs. INPUT SIGNAL AMPLITUDE



MAX295 THD + NOISE vs. INPUT SIGNAL AMPLITUDE



MAX296 THD + NOISE vs. INPUT SIGNAL AMPLITUDE



LABEL	f_{CLK} (Hz)	F_O (kHz)	INPUT FREQUENCY (Hz)	MEASUREMENT BANDWIDTH (kHz)
A	200k	2	200	30
B	1M	10	1k	80
C	200k	4	400	30
D	1M	20	2k	80

8th-Order, Lowpass, Switched-Capacitor Filters

Pin Description

8-PIN	16-PIN	NAME	FUNCTION
	1, 2, 7, 8, 9, 10, 15, 16	N.C.	No Connect
1	3	CLK	Clock Input. Use internal or external clock.
2	4	V-	Negative Supply pin. Dual supplies: -2.375V to -5.500V. Single supplies: V- = 0V.
3	5	OP OUT	Uncommitted Op-Amp Output
4	6	OP IN-	Inverting Input to the uncommitted op amp. The noninverting op amp is internally tied to ground.
5	11	OUT	Filter Output
6	12	GND	Ground. In single-supply operation, GND must be biased to the mid-supply voltage level.
7	13	V+	Positive Supply pin. Dual supplies: +2.375V to +5.500V. Single supplies: +4.75V to +11.0V.
8	14	IN	Filter Input

Detailed Description

Lowpass Butterworth filters such as the MAX291/MAX295 provide maximally flat passband response, making them ideal for instrumentation applications that require minimum deviation from the DC gain throughout the passband.

Lowpass Bessel filters such as the MAX292/MAX296 delay all frequency components equally, preserving the shape of step inputs, subject to the attenuation of the higher frequencies. They also settle faster than Butterworth filters. Faster settling can be important in applications that use a multiplexer (mux) to select one signal to be sent to an analog-to-digital converter (ADC) — an anti-aliasing filter placed between the mux and the ADC must settle quickly after a new channel is selected by the mux.

The difference in the filters' responses can be observed when a 3kHz square wave is applied to the filter input (Figure 1, trace A). With the filter cutoff frequencies set at 10kHz, trace C shows the MAX291/MAX295 Butterworth filter response and trace B shows the MAX292/MAX296 Bessel filter response. Since the MAX292/MAX296 have a linear phase response in the passband, all frequency components are delayed equally, which preserves the square wave. The filters attenuate higher frequencies of the input square wave giving rise to the rounded edges at the output. The MAX291/MAX295 delay dif ferent frequency components by varying times, causing the overshoot and ringing shown in trace C.

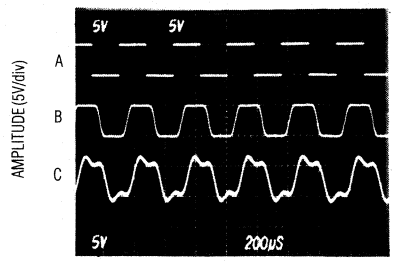


Figure 1. Bessel vs. Butterworth Filter Responses

The MAX291/MAX295 give more attenuation outside the passband. The phase and frequency response curves in the *Typical Operating Characteristics* reveal the differences between the two types of filters.

Corner Frequency and Filter Attenuation

The MAX291/MAX292 operate with a 100:1 clock to corner frequency ratio and a 25kHz maximum corner frequency, where corner frequency is defined as the point where the filter output is 3dB below the filter's DC gain. The MAX295/MAX296 operate with a 50:1 clock to corner frequency ratio with a 50kHz maximum corner frequency. The 8 poles provide 48dB of attenuation per octave.

Background information

Most switched-capacitor filters are designed with biquadratic sections. Each section implements two filtering poles, and the sections can be cascaded to produce higher-order filters. The advantage to this approach is ease of design. However, this type of design can display poor sensitivity if any section's Q is high.

An alternative approach is to emulate a passive network using switched-capacitor integrators with summing and scaling. The passive network can be synthesized using CAD programs, or can be found in many filter books. Figure 2 shows the basic ladder filter structure.

A switched-capacitor filter that emulates a passive ladder filter retains many of its advantages. The filter's component sensitivity is low when compared to a cascaded biquad design because each component affects the entire filter shape, not just one pole pair. That is, a mismatched component in a biquad design will have a concentrated error on its respective poles, while the

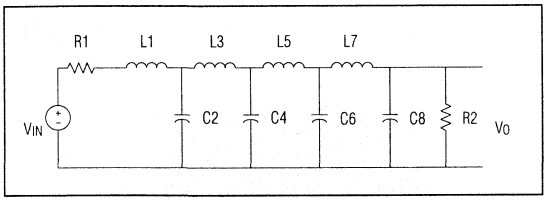


Figure 2. 8th-Order Ladder Filter Network

same mismatch in a ladder filter design will spread its error over all poles.

Clock-Signal Requirements

The MAX291/292/295/296 maximum recommended clock frequency is 2.5MHz, producing a cutoff frequency of 25kHz for the MAX291/MAX292 and 50kHz for the MAX295/MAX296. The CLK pin can be driven by an external clock or by the internal oscillator with an external capacitor. For external clock applications, the clock circuitry has been designed to interface with +5V CMOS logic. Drive the CLK pin with a CMOS gate powered from 0V and +5V when using either a single +5V supply or dual ±5V supplies. Varying the rate of an external clock will dynamically adjust the corner frequency of the filter.

When using the internal oscillator, the capacitance (C_{OSC}) on the CLK pin determines the oscillator frequency:

$$f_{OSC}\,(kHz) \approx \frac{10^5}{3C_{OSC}\,(pF)}$$

The stray capacitance at CLK should be minimized because it will affect the internal oscillator frequency.

Application Information

Power Supplies

The MAX291/292/295/296 operate from either dual or single power supplies. The dual-supply voltage range is ±2.375V to ±5.500V. When using a single supply, tie the V- pin to ground and bias the GND pin to the mid-supply point using a resistor-divider network, as shown in Figure 3.

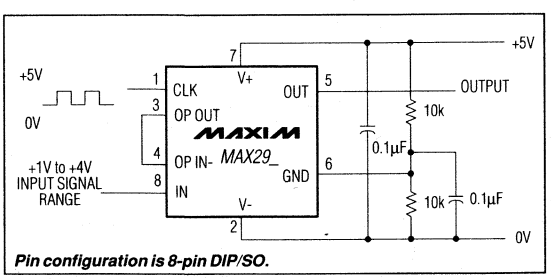


Figure 3. +5V Single-Supply Operation

Input Signal Range

The ideal input signal range is determined by observing at what voltage level the total harmonic distortion plus noise (THD + Noise) ratio is maximized for a given corner frequency. The *Typical Operating Characteristics* show the MAX291/292/295/296 THD + Noise response as the input signal's peak-to-peak amplitude is varied.

Uncommitted Op Amp

The uncommitted op amp has its noninverting input tied to the GND pin, and can be used to build a 1st- or 2nd-order continuous lowpass filter. This filter is convenient for anti-aliasing applications, or for clock noise attenuation at the switched-capacitor filter's output. Figure 4 shows a 2nd-order lowpass Butterworth with components selected for a 10kHz corner frequency. This filter's input resistance is 22kΩ, which satisfies the minimum load requirements of the switched-capacitor filter.

DAC Post-Filtering

When using the MAX291/292/295/296 for DAC post-filtering, synchronize the DAC and the filter clocks. If clocks are not synchronized, beat frequencies will alias into the desired passband. The DAC's clock should be generated by dividing down the switched-capacitor filter's clock.

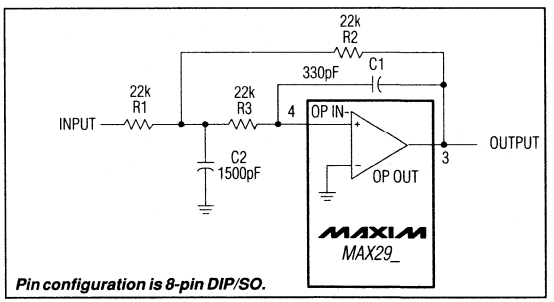


Figure 4. Uncommitted Op Amp Configured as a 2nd-Order Butterworth Lowpass Filter (F_O = 10kHz)

Harmonic Distortion

Harmonic distortion arises from nonlinearities within the filters. These nonlinearities generate harmonics when a pure sine wave is applied to the filter input. Table 1 lists typical harmonic distortion values for the MAX291/292/295/296 with a 1kHz 5Vp-p sine wave input signal, a 1MHz clock frequency, and a 5kΩ load.

Table 1. Typical Harmonic Distortion (dB)

		Harmonic			
		2nd	3rd	4th	5th
Filter	MAX291	-72	-78	-83	-89
	MAX292	-71	-82	-82	-88
	MAX295	-93	-86	-92	-97
	MAX296	-71	-89	-96	-96

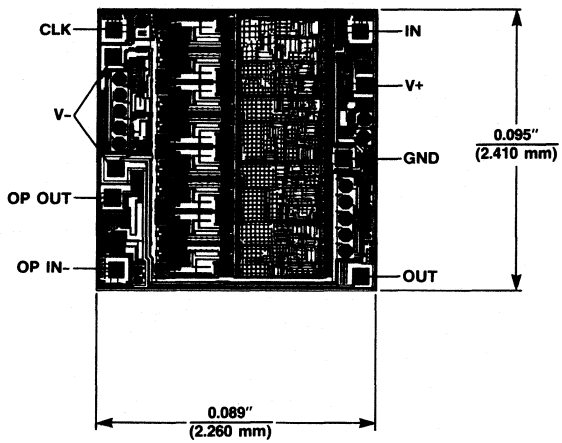
8th-Order, Lowpass, Switched-Capacitor Filters

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX292EPA	-40°C to +85°C	8 Plastic DIP
MAX292ESA	-40°C to +85°C	8 SO*
MAX292EWE	-40°C to +85°C	16 Wide SO
MAX292MJA	-55°C to +125°C	8 CERDIP***
MAX295CPA	0°C to +70°C	8 Plastic DIP
MAX295CSA	0°C to +70°C	8 SO*
MAX295CWE	0°C to +70°C	16 Wide SO
MAX295C/D	0°C to +70°C	Dice**
MAX295EPA	-40°C to +85°C	8 Plastic DIP
MAX295ESA	-40°C to +85°C	8 SO*
MAX295EWE	-40°C to +85°C	16 Wide SO
MAX295MJA	-55°C to +125°C	8 CERDIP***
MAX296CPA	0°C to +70°C	8 Plastic DIP
MAX296CSA	0°C to +70°C	8 SO*
MAX296CWE	0°C to +70°C	16 Wide SO
MAX296C/D	0°C to +70°C	Dice**
MAX296EPA	-40°C to +85°C	8 Plastic DIP
MAX296EWE	-40°C to +85°C	16 Wide SO
MAX296ESA	-40°C to +85°C	8 SO*
MAX296MJA	-55°C to +125°C	8 CERDIP***

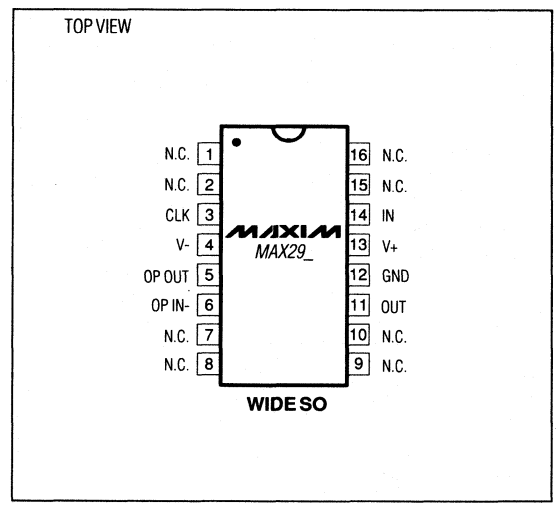
** Contact factory for availability.*
*** Contact factory for dice specifications.*
**** Contact factory for availability and processing to MIL-STD-883.*

Chip Topography



NOTE: SUBSTRATE CONNECTED TO V+.

Pin Configurations (continued)



19-0020; Rev 0; 6/92

MAXIM

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

General Description

The MAX293/MAX294/MAX297 are easy-to-use, 8th-order, lowpass, elliptic, switched-capacitor filters that can be set up with corner frequencies from 0.1Hz to 25kHz (MAX293/MAX294) or from 0.1Hz to 50kHz (MAX297).

The MAX293/MAX297's 1.5 transition ratio provides sharp rolloff and -80dB of stopband rejection. The MAX294's 1.2 transition ratio provides the steepest rolloff and -58dB of stopband rejection. All three filters have fixed responses, so the design task is limited to selecting the clock frequency that controls the filter's corner frequency.

An external capacitor is used to generate a clock using the internal oscillator, or an external clock signal can be used. An uncommitted op amp (noninverting input grounded) is provided for building a continuous-time lowpass filter for post-filtering or anti-aliasing. Steep rolloff and high order make these filters ideal for anti-aliasing applications that require maximum bandwidth, and for communication applications that require filtering signals in close proximity within the frequency domain.

The MAX293/MAX294/MAX297 are available in 8-pin DIP and 16-pin wide SO packages, delivering aggressive performance from a tiny area.

Applications

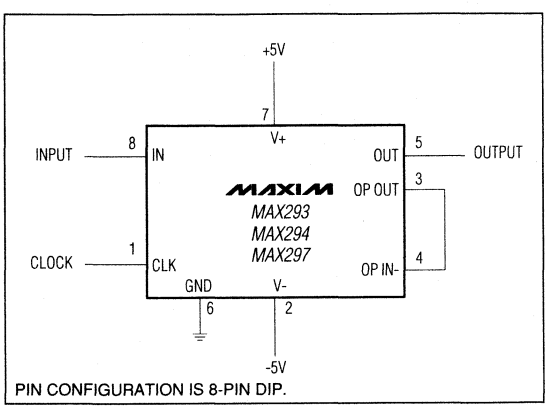
Data-Acquisition Systems

Anti-Aliasing

DAC Post-Filtering

Voice/Data Signal Filtering

Typical Operating Circuit



PIN CONFIGURATION IS 8-PIN DIP.

Features

- ♦ **8th-Order Lowpass Elliptic Filters**
- ♦ **Clock-Tunable Corner-Frequency Range:**
  0.1Hz to 25kHz (MAX293/MAX294)
  0.1Hz to 50kHz (MAX297)
- ♦ **No External Resistors or Capacitors Required**
- ♦ **Internal or External Clock**
- ♦ **Clock to Corner Frequency Ratio:**
  100:1 (MAX293/294)
  50:1 (MAX297)
- ♦ **Operate with a Single +5V Supply or Dual ±5V Supplies**
- ♦ **Uncommitted Op Amp for Anti-Aliasing or Clock-Noise Filtering**
- ♦ **8-Pin DIP and 16-Pin Wide SO Packages**

Ordering Information

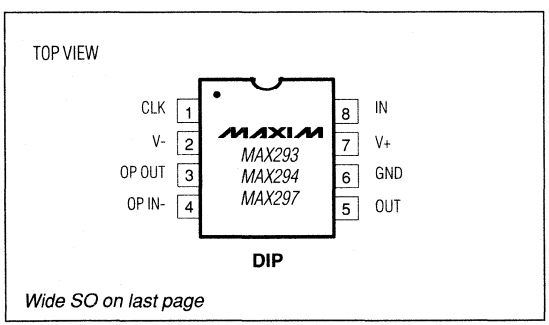
PART	TEMP. RANGE	PIN-PACKAGE
MAX293CPA	0°C to +70°C	8 Plastic DIP
MAX293CWE	0°C to +70°C	16 Wide SO
MAX293C/D	0°C to +70°C	Dice*
MAX293EPA	-40°C to +85°C	8 Plastic DIP
MAX293EWE	-40°C to +85°C	16 Wide SO
MAX293MJA	-55°C to +125°C	8 CERDIP**
MAX294CPA	0°C to +70°C	8 Plastic DIP
MAX294CWE	0°C to +70°C	16 Wide SO
MAX294C/D	0°C to +70°C	Dice*

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations



Wide SO on last page

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-) 12V
Input Voltage at Any Pin ..... (V- - 0.3V) ≤ V_{IN} ≤ (V+ + 0.3V)
Continuous Power Dissipation
8-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
16-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
8-Pin CERDIP (derate 8.00mW/°C above +70°C) 640mW

Operating Temperature Ranges:
MAX29_C__ ..... 0°C to +70°C
MAX29_E__ ..... -40°C to +85°C
MAX29_MJA ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, filter output measured at OUT pin, 20kΩ load resistor to ground at OUT, f_{CLK} = 100kHz (MAX293/MAX294) or f_{CLK} = 50kHz (MAX297) T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FILTER CHARACTERISTICS						
Corner-Frequency Range	MAX293/MAX294			0.1-25k		Hz
	MAX297			0.1-50k		
Clock to Corner Frequency Ratio	MAX293/MAX294			100:1		
	MAX297			50:1		
Clock to Corner Frequency Tempco	MAX293			8		ppm/°C
	MAX294			7		
	MAX297			4		
Insertion Gain Relative to DC Gain (Note 1)	MAX293	f_{IN} = 0.381F_O	0.12	-0.10	-0.17	dB
		f_{IN} = 0.594F_O	0.12	0.02	-0.17	
		f_{IN} = 0.759F_O	0.12	-0.11	-0.17	
		f_{IN} = 0.866F_O	0.12	-0.03	-0.17	
		f_{IN} = 0.939F_O	0.12	-0.11	-0.17	
		f_{IN} = 0.993F_O	0.12	0.04	-0.17	
		f_{IN} = 1.000F_O	0.12	0.01	-0.17	
		f_{IN} = 1.500F_O	-75	-78		
		f_{IN} = 1.610F_O	-80	-87		
		f_{IN} = 2.020F_O	-80	-84		
		f_{IN} =4.020F_O	-80	-84		
	MAX294	f_{IN} = 0.425F_O	0.10	-0.11	-0.17	
		f_{IN} = 0.644F_O	0.10	0.02	-0.17	
		f_{IN} = 0.802F_O	0.10	-0.10	-0.17	
		f_{IN} = 0.895F_O	0.10	-0.03	-0.17	
		f_{IN} = 0.946F_O	0.10	-0.07	-0.17	
		f_{IN} = 0.994F_O	0.26	0.16	-0.17	
		f_{IN} = 1.000F_O	0.26	0.13	-0.17	
		f_{IN} = 1.200F_O	-51	-54		
		f_{IN} = 1.270F_O	-57	-62		
		f_{IN} = 1.530F_O	-57	-60		
		f_{IN} = 2.840F_O	-57	-60		

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, filter output measured at OUT pin, 20kΩ load resistor to ground at OUT, f_{CLK} = 100kHz (MAX293/MAX294) or f_{CLK} = 50kHz (MAX297) T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Insertion Gain Relative to DC Gain (Note 1) (continued)	MAX297	f_{IN} = 0.377F_O	0.10	-0.11	-0.17	dB
		f_{IN} = 0.591F_O	0.10	0.03	-0.17	
		f_{IN} = 0.754F_O	0.10	-0.12	-0.17	
		f_{IN} = 0.873F_O	0.10	0.02	-0.17	
		f_{IN} = 0.944F_O	0.10	-0.07	-0.17	
		f_{IN} = 0.996F_O	0.20	0.11	-0.17	
		f_{IN} = 1.000F_O	0.20	0.10	-0.17	
		f_{IN} = 1.500F_O	-75	-79		
		f_{IN} = 1.610F_O	-80	-87		
		f_{IN} = 2.020F_O	-80	-84		
		f_{IN} = 4.000F_O	-80	-85		
Passband Ripple	MAX293			0.15		dB
	MAX294			0.27		
	MAX297			0.23		
Output DC Swing			±4			V
Output Offset Voltage	IN = GND			±150	±400	mV
DC Insertion Gain with Output Offset Removed			-0.15	±0.01	0.15	dB
Total Harmonic Distortion plus Noise	T_A = +25°C	MAX293		-71		dB
		MAX294		-69		
		MAX297		-77		
Clock Feedthrough	T_A = +25°C			5.0		mVp-p
Output Drive Capability			20	10		kΩ
CLOCK						
Internal Oscillator Frequency	C_{OSC} = 1000pF		29	35	43	kHz
Internal Oscillator Current Source/Sink	V_{CLK} = 0V or 5V			±70	±120	µA
Clock Input (Note 2) High			4.0			V
Low					1.0	
UNCOMMITTED OP AMP						
Input Offset Voltage				±10	±50	mV
Output Drive Capability			20	10		kΩ
Output DC Swing			±4			V
Gain-Bandwidth Product				4		MHz
POWER REQUIREMENTS						
Supply Voltage Dual Supply			±2.375		±5.5	V
Single Supply	V- = 0V, GND = V+/2		4.75		11.0	
Supply Current	V+ = 5V, V- = -5V, V_{CLK} = 0V to 5V			15.0	22.0	mA
	V+ = 2.375V, V- = -2.375V, V_{CLK} = -2V to 2V			7.0	12.0	

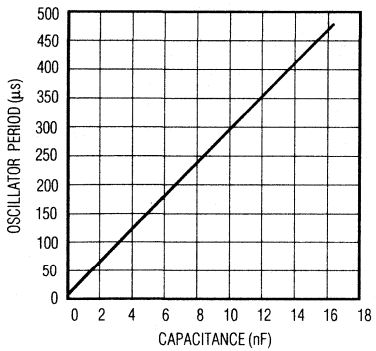
Note 1: Test frequencies selected at ripple peaks and troughs.
Note 2: Guaranteed by design.

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

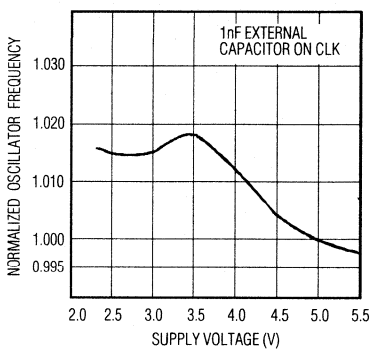
Typical Operating Characteristics

(V+ = 5V, V- = -5V, f_{CLK} = 100kHz (MAX293/MAX294) or f_{CLK} = 50kHz (MAX297), T_A = +25°C, unless otherwise noted.)

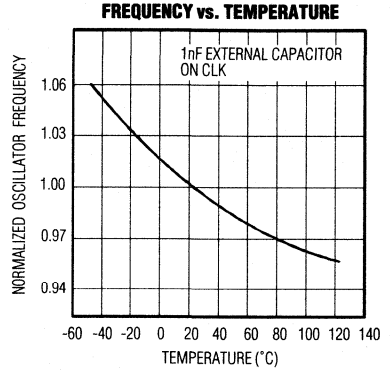
INTERNAL OSCILLATOR PERIOD vs. CAPACITANCE VALUE



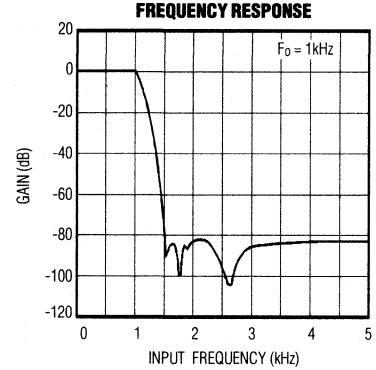
NORMALIZED INTERNAL OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



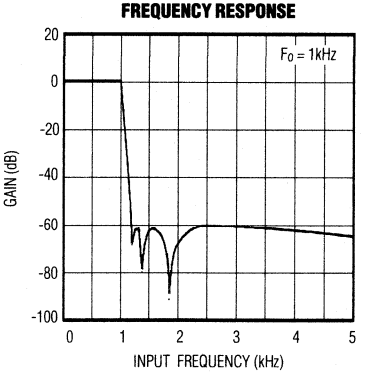
NORMALIZED INTERNAL OSCILLATOR FREQUENCY vs. TEMPERATURE



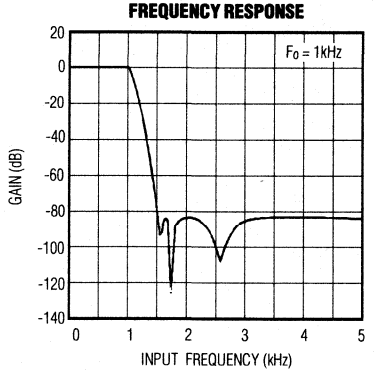
MAX293 FREQUENCY RESPONSE



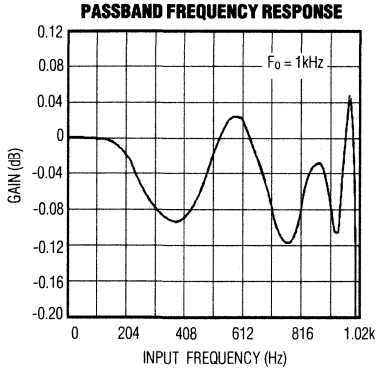
MAX294 FREQUENCY RESPONSE



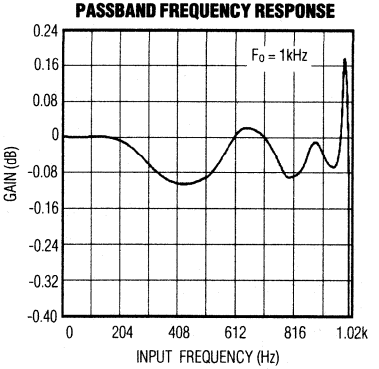
MAX297 FREQUENCY RESPONSE



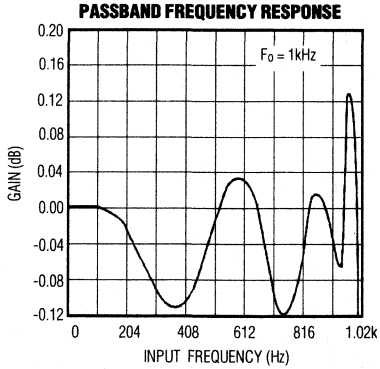
MAX293 PASSBAND FREQUENCY RESPONSE



MAX294 PASSBAND FREQUENCY RESPONSE



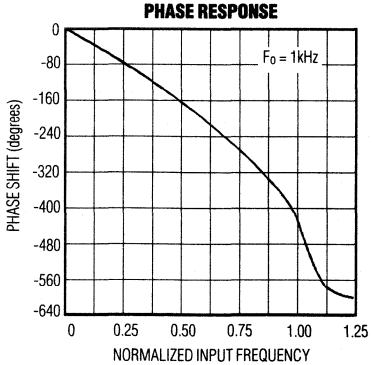
MAX297 PASSBAND FREQUENCY RESPONSE



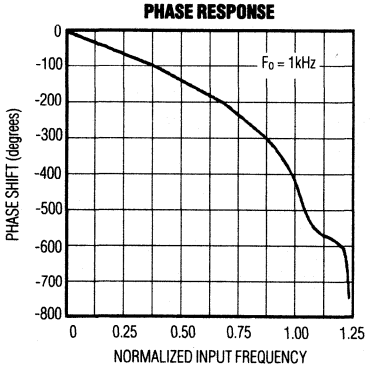
Typical Operating Characteristics (continued)

(V+ = 5V, V- = -5V, f_{CLK} = 100kHz (MAX293/MAX294) or f_{CLK} = 50kHz (MAX297), T_A = +25°C, unless otherwise noted.)

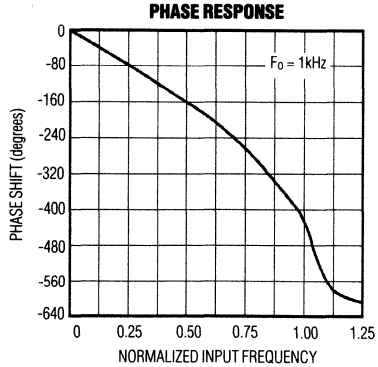
MAX293 PHASE RESPONSE



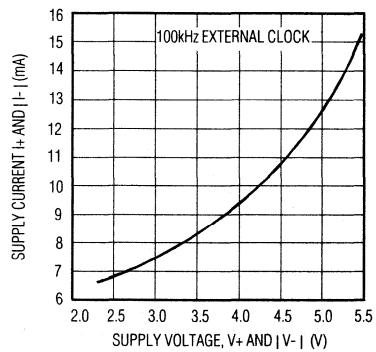
MAX294 PHASE RESPONSE



MAX297 PHASE RESPONSE



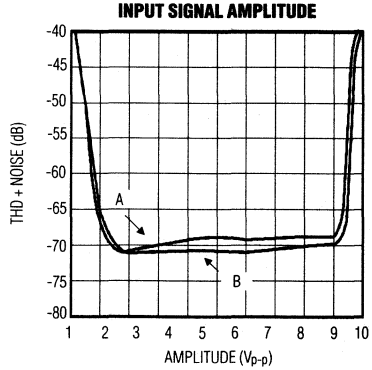
SUPPLY CURRENT vs. SUPPLY VOLTAGE



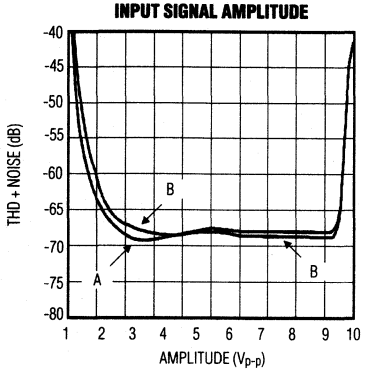
LABEL	f_{CLK} (Hz)	F_O (kHz)	INPUT FREQ. (Hz)	MEASUREMENT BANDWIDTH (kHz)
A	200k	2	200	30
B	1M	10	1k	80
C	200k	4	400	30
D	1M	20	2k	80

(V+ = 5V, V- = -5V, R_{LOAD} = 20kΩ, T_A = +25°C, unless otherwise noted.)

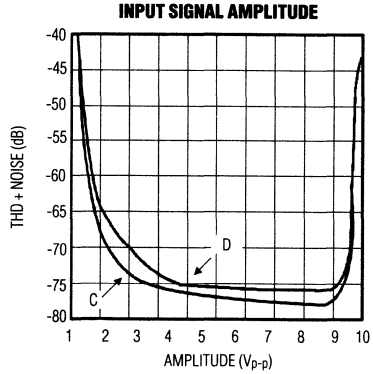
MAX293 THD + NOISE vs. INPUT SIGNAL AMPLITUDE



MAX294 THD + NOISE vs. INPUT SIGNAL AMPLITUDE



MAX297 THD + NOISE vs. INPUT SIGNAL AMPLITUDE



8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

Pin Description

PIN		NAME	FUNCTION
8-PIN DIP	16-PIN SO		
	1,2,7,8,9, 10,15,16	N.C.	No Connect—not internally connected
1	3	CLK	Clock Input—use internal or external clock.
2	4	V-	Negative Supply pin. Dual supplies: -2.375V to -5.5V. Single supply: V- = 0V.
3	5	OP OUT	Uncommitted Op-Amp Output
4	6	OP IN-	Inverting Input to the uncommitted op amp. The noninverting op amp is internally tied to GND.
5	11	OUT	Filter Output
6	12	GND	Ground. In single-supply operation, GND must be biased to the mid-supply voltage level.
7	13	V+	Positive Supply pin. Dual supplies: +2.375V to +5.5V. Single supply: +4.75V to +11.0V.
8	14	IN	Filter Input

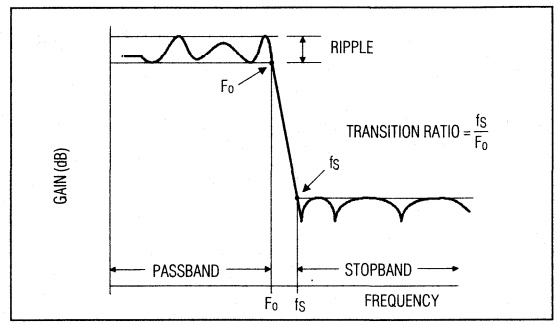


Figure 1. Elliptic Filter Response

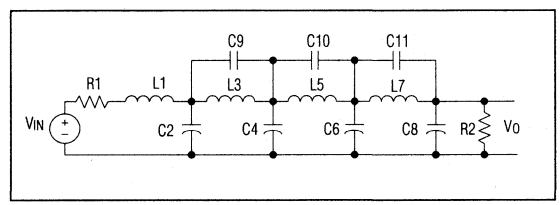


Figure 2. 8th-Order Ladder Filter Network

Detailed Description

The MAX293/MAX294/MAX297 8th-order (eight-pole), elliptic, switched-capacitor, lowpass filters provide the steepest possible rolloff with frequency of the four common filter types (Butterworth, Bessel, Chebyshev, elliptic). The high Q value of the poles near the passband edge combined with stopband zeros allows for the sharp attenuation characteristic of elliptic filters. The MAX293/MAX297 have a 1.5 transition ratio and typically -78dB and -79dB of stopband rejection, respectively; the MAX294 has a 1.2 transition ratio (providing the steepest rolloff) and typically -58dB of stopband rejection.

Passband Ripple and Corner Frequency

The MAX293/MAX294 operate with a 100:1 clock to corner frequency ratio and a 25kHz maximum corner frequency, with corner frequency defined as the point where the filter output attenuation falls just below the passband ripple (Figure 1). The passband ripple is typically 0.15dB (MAX293) and 0.27dB (MAX294). The MAX297 operates with a 50:1 clock to corner frequency ratio and a 50kHz maximum corner frequency. Its passband ripple is typically 0.23dB.

Transition Ratio and Stopband Response

In the frequency domain, the first transmission zero causes the filter's amplitude to drop to a minimum level. Beyond this zero, the response rises as the frequency increases until the next transmission zero. Several repetitions of this response create the filter's stopband comb shape (Figure 1). The stopband begins at f_S. At frequencies above f_S, the filter's gain does not exceed the gain at f_S. The transition ratio is defined as the ratio of the stopband frequency to the corner frequency.

Background Information

Most switched-capacitor filters are designed with biquadratic sections. Each section implements two filtering poles, and the sections can be cascaded to produce higher-order filters. The advantage to this approach is ease of design. However, this type of design is highly sensitive to component variations if any section's Q is high.

An alternative approach is to emulate a passive network using switched-capacitor integrators with summing and scaling. The passive network can be synthesized using CAD programs, or can be found in many filter books. Figure 2 shows the basic ladder filter structure.

A switched-capacitor filter that emulates a passive ladder filter retains many of its advantages. The filter's component sensitivity is low when compared to a cascaded biquad design because each component affects the entire filter shape, not just one pole pair. That is, a mismatched component in a biquad design will have a concentrated error on its respective poles, while the

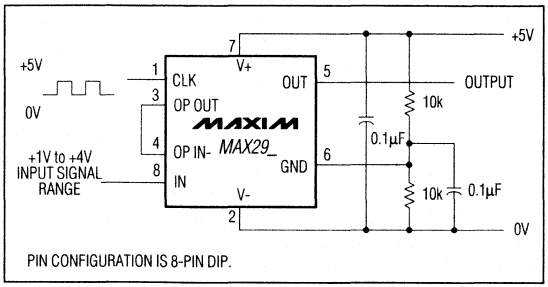


Figure 3. +5V Single-Supply Operation

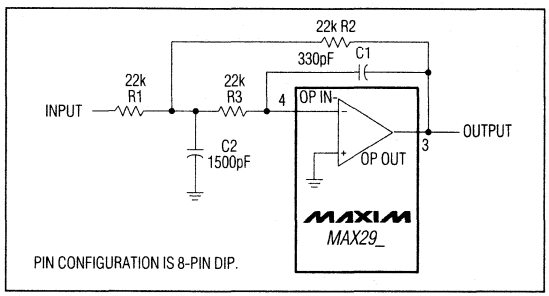


Figure 4. Uncommitted Op Amp Configured as a 2nd-Order Butterworth Lowpass Filter (F_o = 10kHz)

same mismatch in a ladder filter design will spread its error over all poles.

Clock-Signal Requirements

The MAX293/MAX294/MAX297 maximum recommended clock frequency is 2.5MHz, producing a cutoff frequency of 25kHz for the MAX293/MAX294 and 50kHz for the MAX297. The CLK pin can be driven by an external clock or by the internal oscillator with an external capacitor. For external clock applications, the clock circuitry has been designed to interface with +5V CMOS logic. Drive the CLK pin with a CMOS gate powered from 0V and +5V when using either a single supply or dual ±5V supplies. Varying the rate of an external clock will dynamically adjust the filter's corner frequency.

When using the internal oscillator, the capacitance (C_{OSC}) on the CLK pin determines the oscillator frequency:

$$f_{OSC(kHz)} = \frac{10^5}{3C_{OSC(pF)}}$$

The stray capacitance at CLK should be minimized, since it will affect the internal oscillator frequency.

Applications Information

Power Supplies

The MAX293/MAX294/MAX297 operate from either dual or single power supplies. The dual-supply voltage range is ±2.375V to ±5.5V (0.1µF bypass capacitors from each supply to GND are recommended). When using a single supply, tie the V- pin to ground and bias the GND pin to the mid-supply point using a resistor-divider network, as shown in Figure 3.

Input-Signal Amplitude Range

The ideal input-signal range is determined by observing at what voltage level the signal-to-noise plus distortion (SINAD) ratio is maximized for a given corner frequency. The *Typical Operating Characteristics* show the MAX293/MAX294/MAX297 THD + Noise response as the input signal's peak-to-peak amplitude is varied.

Uncommitted Op Amp

The uncommitted op amp has its noninverting input connected to the GND pin, and can be used to build a 1st- or 2nd-order continuous-time lowpass filter. This filter is intended for anti-aliasing applications preceding the switched-capacitor filter, but it can be used as a post-filter to reduce clock noise. Figure 4 shows one of many filters that can be built with this op amp: a 2nd-order Butterworth filter with a 10kHz corner frequency and an input impedance greater than 22kΩ. Table 1 gives alternative component values for different corner frequencies of the same Butterworth filter.

Table 1. Component Values for Figure 4's Filter

Corner Freq. (Hz)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	C1 (F)	C2 (F)
100k	10	10	10	68p	330p
50k	20	20	20	68p	330p
25k	20	20	20	150p	680p
10k	22	22	22	330p	1.5n
1k	22	22	22	3.3p	15n
100	22	22	22	33n	150n
10	22	22	22	330n	1.5µ

NOTE: Some approximations have been made in selecting preferred component values.

The passband error caused by a 2nd-order Butterworth can be calculated using the formula:

$$\text{Gain error} = -10\log\left[1 + \left(\frac{f}{f_c}\right)^4\right] \text{ dB}$$

8th-Order, Lowpass, Elliptic, Switched-Capacitor Filters

As the passband ripple of the MAX293/MAX294/MAX297 elliptic filters is of the order of ±0.1dB, it is normally appropriate to keep the passband errors of any anti-aliasing filter at or below this level. This is achieved by choosing the corner frequency of Figure 4's Butterworth filter (f_{cB}) to be higher than the corner frequency of the elliptic switched-capacitor filter (f_{cE}) by a factor of 2.5 or more. A factor of 5 or more is recommended to avoid problems with component tolerances, i.e. $f_{cB} > (5)(f_{cE})$.

When using the uncommitted op amp as a post-filter to reduce clock noise, keep the filter's input impedance above 20kΩ to avoid excessive loading of the switched-capacitor filter. Note that the op amp experiences some clock feedthrough, so it is generally more useful for anti-aliasing than for clock-noise attenuation.

DAC Post-Filtering

When using the MAX293/MAX294/MAX297 for DAC post-filtering, synchronize the DAC and the filter clocks. If clocks are not synchronized, beat frequencies will alias into the desired passband. The DAC's clock should be generated by dividing down the switched-capacitor filter's clock.

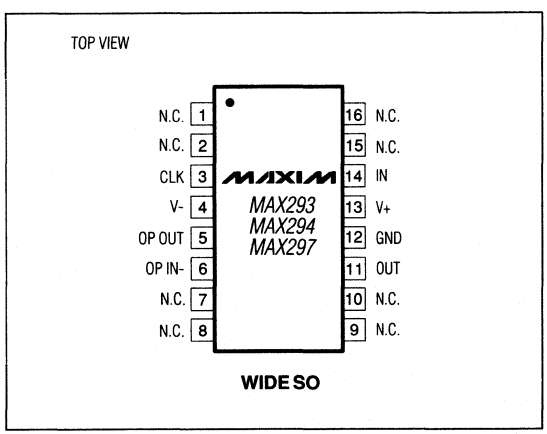
Harmonic Distortion

Harmonic distortion arises from nonlinearities within the filter. These nonlinearities generate harmonics when a pure sine wave is applied to the filter input. Table 2 lists typical harmonic distortion values for the MAX293/MAX294/MAX297 with a 1kHz 5Vp-p sine wave input signal, a 1MHz clock frequency, and a 20kΩ load.

Table 2. Typical Harmonic Distortion (dB)

FILTER	HARMONIC			
	2nd	3rd	4th	5th
MAX293	70	90	88	92
MAX294	67	90	92	94
MAX297	84	89	93	99

Pin Configurations (continued)



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX294EPA	-40°C to +85°C	8 Plastic DIP
MAX294EWE	-40°C to +85°C	16 Wide SO
MAX294MJA	-55°C to +125°C	8 CERDIP**
MAX297CPA	0°C to +70°C	8 Plastic DIP
MAX297CWE	0°C to +70°C	16 Wide SO
MAX297C/D	0°C to +70°C	Dice*
MAX297EPA	-40°C to +85°C	8 Plastic DIP
MAX297EWE	-40°C to +85°C	16 Wide SO
MAX297MJA	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*
*** Contact factory for availability and processing to MIL-STD-883.*

A/D Converters

7

* Advance Information – first page of data sheet in preparation.

General-Purpose A/D Converters

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	Features	Price† 1000-up ($)
MAX153	8	0.660	1	1000	E	µP/8	+5 & ±5	+5, ±2.5	High-speed A/D with powerdown	††
MX7821	8	0.660	1	1000	E	µP/8	+5 & ±5	+5, ±2.5	Complete A/D with T/H	7.54
MAX150	8	1.34	1	500	E/I/+2.5	µP/8	+5	+5	Complete A/D with T/H and ref	7.96
MX7820	8	1.34	1	500	E	µP/8	+5	+5	Plug-in replacement for AD7820	7.93
ADC0820	8	1.38	1	400	E	µP/8	+5	+5	Complete A/D with T/H	7.16
MAX154	8	2	4	300	E/I/+2.5	µP/8	+5	+5	4-Ch A/D with T/H and ref	8.36
MAX158	8	2	8	300	E/I/+2.5	µP/8	+5	+5	8-Ch A/D with T/H and ref	8.76
MX7824	8	2	4	300	E	µP/8	+5	+5	Plug-in replacement for AD7824	8.33
MX7828	8	2	8	300	E	µP/8	+5	+5	Plug-in replacement for AD7828	8.73
MAX155	8	3.8	8	250	E/I/+2.5	µP/8	+5	+2.5, ±2.5	8-Ch simultaneous T/H and ref	10.00
MAX156	8	3.8	4	250	E/I/+2.5	µP/8	+5	+2.5, ±2.5	4-Ch simultaneous T/H and ref	8.85
MAX160	8	4	1	-	E	µP/8	+5	+10, ±5	Ratiometric, single-supply A/D	7.20
MAX165	8	5	1	200	E/I/+1.23	µP/8	+5	+5	Complete sampling A/D with ref	4.99
MAX166	8	5	1	200	E/I/+1.23	µP/8	+5	+5	Differential input complete A/D	4.99
MX7575	8	5	1	200	E	µP/8	+5	+5	Plug-in replacement for AD7575	3.74
MX7576	8	10	1	-	E	µP/8	+5	+5	Plug-in replacement for AD7576	3.52
MX7574	8	15	1	-	E	µP/8	+5	+10, ±5	Plug-in replacement for AD7574	4.80
MAX161	8	20	8	-	E	µP/8	+5	+10	8-Ch A/D with RAM buffer	11.12
MX7581	8	66.6	8	-	E	µP/8	+5	+10	Plug-in replacement for AD7581	11.08
MAX151	10	2.5	1	300	E/I/+4.0	µP/10	±5	+5	Sampling A/D with ref	12.67
MAX173	10	5	1	-	I/-5.25	µP/8/12	+5 & -12/-15	+5	Complete with ref	7.01
MAX177	10	8.33	1	100	I/-5.25	µP/8/12	+5 & -12/-15	±2.5	Sampling A/D with ref	7.96
MAX120	12	1.6	1	500	I/-5.0	µP/12	+5 & -12/-15	±5	High-speed complete sampling A/D	††
MAX122	12	2.6	1	333	I/-5.0	µP/12	+5 & -12/-15	±5	High-speed complete sampling A/D	††
MX578	12	3	1	-	E/I/+10.0	Logic	+5 & ±15	±10	With parallel/serial outputs	88.71
MAX162	12	3.25	1	-	I/-5.25	µP/8/12	+5 & -12/-15	+5	High-speed A/D with internal ref	19.20
MAX183	12	3.25	1	-	E	µP/8/12	+5 & -12/-15	+5, ±5, +10	High-speed A/D with external ref	15.00
MX7672-03	12	3.25	1	-	E	µP/8/12	+5 &-12	+5, ±5, +10	Plug-in replacement for AD7672-03	57.38
MAX176	12	3.5	1	250	I/-5.0	Serial	+5 & -12/-15	±5	8-pin miniDIP	††
MAX170	12	5	1	-	I/-5.25	Serial/12	+5 & -12/-15	+5	8-pin miniDIP	11.96
MAX171	12	5	1	-	I/-5.25	Serial/12	+5 & -12/-15	+5	Opto-isolated	20.25
MAX184	12	5	1	-	E	µP/8/12	+5 & -12/-16	+5/±5/+10	High-speed A/D with external ref	13.75

* E = external reference, I = internal reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product- contact factory for pricing and availability.

General-Purpose A/D Converters (continued)

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	Features	Price† 1000-up ($)
MX7572-05	12	5	1	-	I/-5.25	µP/8/12	+5 & -15	+5	Plug-in replacement for AD7572-05	20.00
MX7672-05	12	5	1	-	E	µP/8/12	+5 & -12	+5, ±5, +10	Plug-in replacement for AD7672-05	33.66
MAX186	12	7.5	8	133	E/I/+4.096	Serial	+5/±5	+5, ±2.5	7mW, 10µA powerdown	††
MAX187	12	7.5	1	133	E/I/+4.096	Serial	+5/±5	+5, ±2.5	7mW, 8-pin package	††
MAX188	12	7.5	8	133	E	Serial	+5/±5	+5, ±2.5	MAX186 without reference	††
MAX189	12	7.5	1	133	E	Serial	+5/±5	+5, ±2.5	MAX187 without reference	††
MAX191	12	7.5	1	100	E/I/+4.096	µP/12/serial	+5/±5	+5, ±2.5	15mW, 100µW powerdown	††
MAX190	12	7.8	1	100	E/I/+4.096	µP/12/serial	+5 & ±5	+5	Low-power sampling A/D with ref	10.00
MAX174	12	8	1	-	E/I/+10.0	µP/8/12	+5 & ±12/±15	±5, ±10, +10, +20	Upgrades for AD574A/AD674A	28.13
MAX163	12	8.33	1	100	I/-5.0	µP/8/12	+5 & -12/-15	+5	Complete sampling A/D with ref	14.40
MAX164	12	8.33	1	100	I/-5.0	µP/8/12	+5 & -12/-15	±5	Complete sampling A/D with ref	14.40
MAX167	12	8.33	1	100	I/-5.0	µP/8/12	+5 & -12/-15	±2.5	Complete sampling A/D with ref	14.40
MAX180	12	8.33	8	100	E/I/-5.0	µP/8/16	+5 & -12/-15	+5, ±2.5	Data-acquisition system	17.00
MAX181	12	8.33	6	100	E/I/-5.0	µP/8/16	+5 & -12/-15	+5, ±2.5	Data-acquisition system	17.00
MAX172	12	10	1	-	I/-5.25	µP/8/12	+5 & -12/-15	+5	First lowest-cost complete A/D	9.60
MAX185	12	10.4	1	-	E	µP/8/12	+5 & -12/-15	+5, ±5, +10	High-speed A/D with external ref	12.00
MX7672-10	12	10.4	1	-	E	µP/8/12	+5 & -12	+5, ±5, +10	Plug-in replacement for AD7672-05	25.25
MX7572-12	12	12	1	-	I/-5.25	µP/8/12	+5 & -15	+5	Plug-in replacement for AD7572-12	14.00
MX674A	12	15	1	-	E/I/+10.0	µP/8/12	+5 & ±12/±15	±5, ±10, +10, +20	Plug-in replacement for AD574A	23.44
MX574A	12	25	1	-	E/I/+10.0	µP/8/12	+5 & ±12/±15	±5, ±10, +10, +20	Plug-in replacement for AD674A	11.97
MAX178	12	50	1	20	E/I/+5.0	µP/8/16	+5 & +15 & -5	+5	Calibrated to 1LSB, with T/H, ref	15.24
MAX182	12	50	4	20	E/I/+5.0	µP/8/16	+5 & +15 & -5	+5	Calibrated to 1LSB, with T/H, ref	17.55
MX7578	12	100	1	-	E	µP/8/16	+5 & +15 & -5	+5	Plug-in replacement for AD7578	16.96
MX7582	12	100	4	-	E	µP/8/16	+5 & +15 & -5	+5	Plug-in replacement for AD7582	19.50
MAX121	14	2.0	1	400	I/-5.0	Serial	+5 & -12/-15	±5	High-speed, complete sampling A/D with DSP interface	††
MAX168	14	3.5	1	250	E/I/+3.0	µP/8/16	+5 & -5	±3	Complete sampling A/D	††
MAX135	15 + sign	10ms	1	-	E	µP/8	±5	±0.5	High-resolution A/D, <1mW	8.00
MAX132	18 + sign	10ms	1	-	E	Serial	±5	±0.5	Serial high-resolution A/D, <1mW	8.00

* E = external reference, I = internal reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product- contact factory for pricing and availability.

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	Features	Price† 1000-up ($)
MAX153	8	0.660	1	1000	E	µP/8	+5 & ±5	+5, ±2.5	High-speed A/D with powerdown	††
MX7821	8	0.660	1	1000	E	µP/8	+5 & ±5	+5, ±2.5	Complete A/D with T/H	7.54
MAX150	8	1.34	1	500	E/I/+2.5	µP/8	+5	+5	Complete A/D with T/H and ref	7.96
MX7820	8	1.34	1	500	E	µP/8	+5	+5	Plug-in replacement for AD7820	7.93
ADC0820	8	1.38	1	400	E	µP/8	+5	+5	Complete A/D with T/H	7.16
MAX154	8	2	4	300	E/I/+2.5	µP/8	+5	+5	4-Ch A/D with T/H and ref	8.36
MAX158	8	2	8	300	E/I/+2.5	µP/8	+5	+5	8-Ch A/D with T/H and ref	8.76
MX7824	8	2	4	300	E	µP/8	+5	+5	Plug-in replacement for AD7824	8.33
MX7828	8	2	8	300	E	µP/8	+5	+5	Plug-in replacement for AD7828	8.73
MAX155	8	3.8	8	250	E/I/+2.5	µP/8	+5	+2.5, ±2.5	8-Ch simultaneous T/H and ref	10.00
MAX156	8	3.8	4	250	E/I/+2.5	µP/8	+5	+2.5, ±2.5	4-Ch simultaneous T/H and ref	8.85
MAX165	8	5	1	200	E/I/+1.23	µP/8	+5	+5	Complete sampling A/D with ref	4.99
MAX166	8	5	1	200	E/I/+1.23	µP/8	+5	+5	Differential input complete A/D	4.99
MX7575	8	5	1	200	E	µP/8	+5	+5	Plug-in replacement for AD7575	3.74
MAX151	10	2.5	1	300	E/I/+4.0	µP/10	±5	+5	Sampling A/D with ref	12.67
MAX177	10	8.33	1	100	I/-5.25	µP/8/12	+5 & -12/-15	±2.5	Sampling A/D with ref	7.96
MAX120	12	1.6	1	500	I/-5.0	µP/12	+5 & -12/-15	±5	High-speed complete sampling A/D	††
MAX122	12	2.6	1	333	I/-5.0	µP/12	+5 & -12/-15	±5	High-speed complete sampling A/D	††
MAX176	12	3.5	1	250	I/-5.0	Serial	+5 & -12/-15	±5	8-pin miniDIP	††
MAX186	12	7.5	8	133	E/I/+4.096	Serial	+5/±5	+5, ±2.5	7mW, 10µA powerdown	††
MAX187	12	7.5	1	133	E/I/+4.096	Serial	+5/±5	+5, ±2.5	7mW, 8-pin package	††
MAX188	12	7.5	8	133	E	Serial	+5/±5	+5, ±2.5	MAX186 without reference	††
MAX189	12	7.5	1	133	E	Serial	+5/±5	+5, ±2.5	MAX187 without reference	††
MAX191	12	7.5	1	100	E/I/+4.096	µP/12/serial	+5/±5	+5, ±2.5	15mW, 100µW powerdown	††
MAX190	12	7.8	1	100	E/I/+4.096	µP/12/serial	+5 & ±5	+5	Low-power sampling A/D with ref	10.00
MAX163	12	8.33	1	100	I/-5.0	µP/8/12	+5 & -12/-15	+5	Complete sampling A/D with ref	14.40
MAX164	12	8.33	1	100	I/-5.0	µP/8/12	+5 & -12/-15	±5	Complete sampling A/D with ref	14.40
MAX167	12	8.33	1	100	I/-5.0	µP/8/12	+5 & -12/-15	±2.5	Complete sampling A/D with ref	14.40
MAX180	12	8.33	8	100	E/I/-5.0	µP/8/16	+5 & -12/-15	+5, ±2.5	Data-acquisition system	17.00
MAX181	12	8.33	6	100	E/I/-5.0	µP/8/16	+5 & -12/-15	+5, ±2.5	Data-acquisition system	17.00
MAX178	12	50	1	20	E/I/+5.0	µP/8/16	+5 & +15 & -5	+5	Calibrated to 1LSB, with T/H, ref	15.24
MAX182	12	50	4	20	E/I/+5.0	µP/8/16	+5 & +15 & -5	+5	Calibrated to 1LSB, with T/H, ref	17.55
MAX121	14	2.0	1	400	I/-5.0	Serial	+5 & -12/-15	±5	High-speed, complete sampling A/D with DSP interface	††
MAX168	14	3.5	1	250	E/I/+3.0	µP/8/16	+5 & -5	±3	Complete sampling A/D	††

* E = external reference, I = internal reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Future product- contact factory for pricing and availability.

Multi-Channel A/D Converters

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	Features	Price† 1000-up ($)
MAX154	8	2	4	300	E/I/+2.5	µP/8	+5	+5	4-Ch A/D with T/H and ref	8.36
MAX158	8	2	8	300	E/I/+2.5	µP/8	+5	+5	8-Ch A/D with T/H and ref	8.76
MX7824	8	2	4	300	E	µP/8	+5	+5	Plug-in replacement for AD7824	8.33
MX7828	8	2	8	300	E	µP/8	+5	+5	Plug-in replacement for AD7828	8.73
MAX155	8	3.8	8	250	E/I/+2.5	µP/8	+5	+2.5, ±2.5	8-Ch simultaneous T/H and ref	10.00
MAX156	8	3.8	4	250	E/I/+2.5	µP/8	+5	+2.5, ±2.5	4-Ch simultaneous T/H and ref	8.85
MAX161	8	20	8	-	E	µP/8	+5	+10	8-Ch A/D with RAM buffer	11.12
MX7581	8	66.6	8	-	E	µP/8	+5	+10	Plug-in replacement for AD7581	11.08
MAX186	12	7.5	8	133	E/I/+4.096	Serial	+5/±5	+5, ±2.5	7mW, 10µA powerdown	††
MAX188	12	7.5	8	133	E	Serial	+5/±5	+5, ±2.5	MAX186 without reference	††
MAX180	12	8.33	8	100	E/I/-5.0	µP/8/16	+5 & -12/-15	+5, ±2.5	Data-acquisition system	17.00
MAX181	12	8.33	6	100	E/I/-5.0	µP/8/16	+5 & -12/-15	+5, ±2.5	Data-acquisition system	17.00
MAX182	12	50	4	20	E/I/+5.0	µP/8/16	+5 & +15 & -5	+5	Calibrated to 1LSB, with T/H, ref	17.55
MX7582	12	100	4	-	E	µP/8/16	+5 & +15 & -5	+5	Plug-in replacement for AD7582	19.50

Serial A/D Converters

Part Number	Resolution (Bits)	Conversion Time (µs max)	Input Channels	Sample Rate (kHz max)	Reference Voltage* (V)	Data-Bus Interface (Bits)	Supply Voltage (V)	Input Ranges (V)	Features	Price† 1000-up ($)
MAX176	12	3.5	1	250	I/-5.0	Serial	+5 & -12/-15	±5	8-pin miniDIP	††
MAX186	12	7.5	8	133	E/I/+4.096	Serial	+5/±5	+5, ±2.5	7mW, 10µA powerdown	††
MAX187	12	7.5	1	133	E/I/+4.096	Serial	+5/±5	+5, ±2.5	7mW, 8-pin package	††
MAX188	12	7.5	8	133	E	Serial	+5/±5	+5, ±2.5	MAX186 without reference	††
MAX189	12	7.5	1	133	E	Serial	+5/±5	+5, ±2.5	MAX187 without reference	††
MAX191	12	7.5	1	100	E/I/+4.096	µP/12/serial	+5/±5	+5, ±2.5	15mW, 100µW powerdown	††
MAX190	12	7.8	1	100	E/I/+4.096	µP/12/serial	+5 & ±5	+5	Low-power sampling A/D with ref	10.00
MAX121	14	2.0	1	400	I/-5.0	Serial	+5 & -12/-15	±5	High-speed, complete sampling A/D with DSP interface	††
MAX132	18 + sign	10ms	1	-	E	Serial	±5	±0.5	Serial high-resolution A/D, <1mW	8.00

* E = external reference, I = internal reference

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

†† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates. Contact factory for pricing and availability.

Part Number	Resolution (digits)	Resolution (counts)	Output Type	Supply Voltage (V)	Supply Current (mA) max (typ)	References	Features	Price† 1000-up ($)
MAX130	3 1/2	±2000	LCD	+4.5 to 14	0.25 (0.1)	Bandgap	Replacement for ICL7106	4.86
MAX131	3 1/2	±2000	LCD	+4.5 to 14	0.1 (0.06)	Bandgap	Replacement for ICL7136	4.86
MAX136	3 1/2	±2000	LCD	+9	0.15 (0.06)	Bandgap	Hold function, low power	4.32
MAX138	3 1/2	±2000	LCD	+2.25 to 7	0.8 (0.2)	Bandgap	± inputs with single supply	6.88
ICL7106	3 1/2	±2000	LCD	+9	1.8 (0.6)	Zener	For digital multimeters	4.32
ICL7116	3 1/2	±2000	LCD	+9	1.8 (0.8)	Zener	ICL7106 with display hold	4.32
ICL7126	3 1/2	±2000	LCD	+9	0.1 (0.6)	Zener	Use ICL7136 for new designs	4.32
ICL7136	3 1/2	±2000	LCD	+9	0.1 (0.06)	Zener	Low power/noise ICL7106	4.32
MAX139	3 1/2	±2000	LED	+5	0.8 (0.2)	Bandgap	± inputs with single supply	6.08
MAX140	3 1/2	±2000	LED	+5	0.8 (0.2)	Bandgap	Low segment current (2mA)	4.68
ICL7107	3 1/2	±2000	LED	+9	1.8 (0.6)	Zener	For digital panel meters	4.32
ICL7117	3 1/2	±2000	LED	±5	1.8 (0.8)	Zener	ICL7107 with display hold	4.32
ICL7137	3 1/2	±2000	LED	±5	0.2 (0.06)	Zener	Low power when LEDs off	4.32
MAX133	3 3/4	±40,000	µP	+9	0.2 (0.09)	External	20 conv/sec, ±10µV resolution	10.89
MAX134	3 3/4	±40,000	µP	±5	0.2 (0.09)	External	20 conv/sec, ±10µV resolution	10.89
ICL7109	12 bits + sign	±4096	8-/16-bit µP/UART	±5	1.5 (0.7)	Zener	3-state binary outputs	5.10
ICL7129A	4 1/2	±20,000	Triplexed LCD	+9	1.4 (1.0)	External	Lowest noise ±3µV	7.96
ICL7135	4 1/2	±20,000	Multiplexed BCD	±5	2.0 (1.0)	External	For DMM, DPM, data loggers	5.48
MAX135	15 bits + sign	±20,000	µP/8	±5	0.125(0.06)	External	3-state twos-complement outputs	8.00
MAX132	18 bits + sign	±260,000	Serial µP	±5	0.125(0.06)	External	Serial low-power A/D	8.00

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

A/D CONVERTERS

FAST CONVERSION (<100µs) (SEE SAR/FLASH A/Ds)

SLOW CONVERSION (>50ms) (INTEGRATING A/Ds)

LCD DISPLAY

MAX130 (3 1/2 D, B/G)
MAX131 (3 1/2 D, D/G, L)
MAX136 (3 1/2 D, Z, L)
MAX138 (3 1/2 D, B/G, S/S)
ICL7106 (3 1/2 D, Z)
ICL7116 (3 1/2 D, Z, HOLD)
ICL7126 (3 1/2 D, Z, L)
ICL7129A (4 1/2 D)
ICL7136 (3 1/2 D, Z, L)

LED DISPLAY

MAX139 (3 1/2 D, B/G, S/S)
MAX140 (3 1/2 D, B/G, S/S)
ICL7107 (3 1/2 D, Z)
ICL7117 (3 1/2 D, Z, HOLD)
ICL7137 (3 1/2 D, Z, L)

µP INTERFACE

★ **MAX132** (±18 bit, serial out)
MAX133 (±40,000 count, L)
MAX134 (±40,000 count, L)
★ **MAX135** (±15 bit)
ICL7109 (12 bit, Z)
ICL7135 (±20,000 count)

NOTES: HOLD - Has display-hold input
S/S - Has +5V single supply
B/G - Has bandgap reference
Z - Has zener reference
L - Low power

★ New product since the publication of the 1990 Short Form Product Guide.

A/D CONVERTERS

FAST CONVERSION (<100µs) (SAR/FLASH A/Ds)

8-BITS

SINGLE CHANNEL

INTERNAL T/H

- MAX150 (1.34µs/ref)
- ★ MAX153 (0.66µs)
- MX7820 (1.34µs)
- ★ MX7821 (0.66µs)
- ADC0820 (1.38µs)
- MAX165 (5µs/ref)
- MAX166 (5µs/ref/diff in)
- MX7575 (5µs)

EXTERNAL T/H

- MAX160 (4µs)
- MX7575 (5µs)
- MX7574 (15µs)
- ★ MX7576 (10µs)

MULTI-CHANNEL

INTERNAL T/H

- MAX154 (2µs/4-ch/ref)
- MAX158 (2µs/8-ch/ref)
- MAX155 (3µs/8-ch/ref)
- MX7824 (2µs/4-ch)
- MAX156 (3µs/4-ch/ref)
- MX7828 (2µs/8-ch)

EXTERNAL T/H

- MAX161 (20µs/8-ch)
- MX7581 (67µs/8-ch)

10-BITS

INTERNAL T/H

- MAX151 (2.5µs/ref)
- MAX177 (8.33µs/ref)

EXTERNAL T/H

- MAX173 (5µs/ref)

12-BITS

SINGLE CHANNEL

INTERNAL T/H

- ★ MAX120 (1.6µs/ref)
- ★ MAX122 (2.6µs/ref)
- MAX163 (10µs/ref)
- MAX164 (10µs/ref)
- MAX167 (10µs/ref)
- ★ MAX176 (3.5µs/ref/serial)
- MAX178 (50µs/ref)
- ★ MAX187 (7.5µs/ref)
- ★ MAX189 (7.5µs)
- ★ MAX190 (7.8µs/ref)
- ★ MAX191 (7.5µs/ref)

EXTERNAL T/H

- MAX162 (3.25µs/ref)
- MX578 (3µs/ref)
- MAX170 (5µs/ref/serial)
- MX674A (15µs/ref)
- MAX171 (6µs/ref/serial)
- MX7572-05 (5µs/ref)
- MAX172 (10µs/ref)
- MX7572-12 (12µs/ref))
- MAX174 (8µs/ref)
- MX7578 (100µs)
- MAX183 (3.25µs)
- MX7572-03 (3.25µs)
- MAX184 (5µs)
- MX7672-05 (5µs)
- MAX185 (10µs)
- MX672-10 (10µs)
- MX574A (25µs/ref)

MULTI-CHANNEL

INTERNAL T/H

- MAX180 (8.33µs/ref/8-ch)
- ★ MAX186 (7.5µs/ref)
- MAX181 (8.33µs/ref/6-ch)
- ★ MAX188 (7.5µs)
- MAX182 (50µs/ref/4-ch)

EXTERNAL T/H

- MX7582 (100µs/4-ch)

14-BITS

INTERNAL T/H

- ★ MAX121 (2µs/ref)
- ★ MAX168 (3.5µs/ref)

SLOW CONVERSION (>50ms) (SEE INTEGRATING A/Ds)

★ New product since the publication of the 1990 Short Form Product Guide.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

EVALUATION KIT AVAILABLE

MAXIM

500ksps, 12-Bit Sampling ADCs with Track/Hold and Reference

General Description

The MAX120 and MAX122, BiCMOS, sampling 12-bit analog-to-digital converters (ADCs) combine an on-chip track/hold (T/H) and a low-drift voltage reference with fast conversion speeds and low power consumption. The T/H's 350ns acquisition time combined with the MAX120's 1.6µs conversion time results in throughputs as high as 500k samples per second (ksps). Throughput rates of 333ksps are possible with the 2.6µs conversion time of the MAX122.

The MAX120/MAX122 accept analog input voltages from -5V to +5V. The only external components needed are decoupling capacitors for the power-supply and reference voltages. The MAX120 operates with TTL-compatible clocks in the 0.1MHz to 8MHz frequency range. The MAX122 accepts 0.1MHz to 5MHz clock frequencies.

The MAX120/MAX122 employ a standard microprocessor (µP) interface. 3-state data outputs are configured to operate with 12-bit data buses. Data-access and bus-release timing specifications are compatible with most popular µPs without resorting to wait states. All logic inputs and outputs are TTL/CMOS compatible.

Applications

Digital-Signal Processing

Audio and Telecom Processing

Speech Recognition and Synthesis

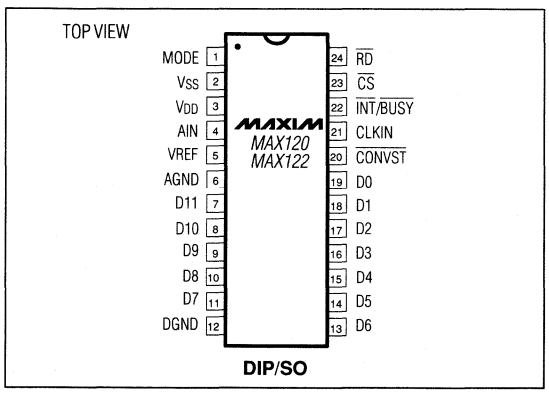
High-Speed Data Acquisition

Spectrum Analysis

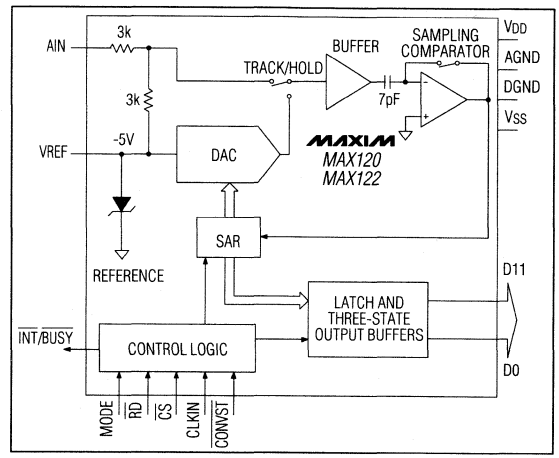
Features

- ♦ **12-Bit Resolution**
- ♦ **No Missing Codes Over Temperature**
- ♦ **20ppm°/C, -5V Internal Reference**
- ♦ **1.6µs Conversion Time/500ksps Throughput (MAX120)**
- ♦ **2.6µs Conversion Time/333ksps Throughput (MAX122)**
- ♦ **Low Noise and Distortion:**
  70 dB Min SINAD;
  -77 dB Max THD (MAX122)
- ♦ **Low Power Dissipation: 210mW**
- ♦ **Separate Track/Hold Control Input**
- ♦ **Continuous-Conversion Mode Available**
- ♦ **±5V Input Range, Overvoltage Tolerant to ±15V**
- ♦ **24-Pin Narrow DIP and Wide SO Packages**

Pin Configuration



Functional Diagram



7

500ksps 12-Bit ADCs with Track/Hold and Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V to +6V
V_{SS} to DGND ..... +0.3V to -17V
AIN to AGND ..... ±15V
AGND to DGND ..... ±0.3V
Digital Inputs/Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 8.70mW/°C above +70°C) 727mW
SO (derate 11.76mW/°C above +70°C) 941mW
CERDIP (derate 12.50W/°C above +70°C) 1000mW

Operating Temperature Ranges:
MAX12_C__ ..... 0°C to +70°C
MAX12_E__ ..... -40°C to +85°C
MAX12_MRG ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +4.75V to +5.25V, V_{SS} = -10.8V to -15.75V, f_{CLK} = 8MHz for MAX120 and 5MHz for MAX122, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution	RES			12			Bits
Differential Nonlinearity (Note 1)	DNL	No missing codes over temp range	MAX122A			±3/4	LSB
			MAX120, MAX122B			±1	
Integral Non-linearity (Note 1)	INL		MAX122A			±3/4	LSB
			MAX120, MAX122B			±1	
Bipolar Zero Error (Note 1)		Code 00..00 to 00..01 transition, near AIN = 0V				±3	LSB
		Temperature drift			±0.005		LSB/°C
Full-Scale Error (Notes 1, 2)		Including reference; adjusted for bipolar zero error; T_A = +25°C				±8	LSB
Full-Scale Temperature Drift		Excluding reference			±1		ppm/°C
Power-Supply Rejection Ratio (Change in FS, Note 3)	PSRR	V_{DD} only, 5V to ±5%			±1/4	±3/4	LSB
		V_{SS} only, -12V to ±10%			±1/4	±1	
		V_{SS} only, -15V to ±5%			±1/4	±1	
ANALOG INPUT							
Input Range				-5		+5	V
Input Current		AIN = +5V (approximately 6kΩ to REF)				2.5	mA
Input Capacitance (Note 4)						10	pF
Full-Power Input Bandwidth					1.5		MHz
REFERENCE							
Output Voltage		No external load, AIN = 5V, T_A = +25°C		-5.02		-4.98	V
External Load Regulation		0mA < I_{SINK} < 5mA, AIN = 0V				5	mV
Temperature Drift (Note 5)		MAX12_C/E				±20	ppm/°C
		MAX12_M				±25	
Supply Rejection		V_{DD} only, +5V to ±5%			0.6		mV
		V_{SS} only, -12V to ±10%			0.6		
		V_{SS} only, -15V to ±5%			0.6		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +4.75V to +5.25V, V_{SS} = -10.8V to -15.75V, f_{CLK} = 8MHz for MAX120 and 5MHz for MAX122, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE (MAX120: f_S = 500kHz, AIN = ±5Vp-p, 100kHz, Note 4) (MAX122: f_S = 333kHz, AIN = ±5Vp-p, 50kHz, Note 4)							
Signal-to-Noise Plus Distortion	S/(N+D)	MAX120		69	70		dB
		MAX122		70	71.5		
Total Harmonic Distortion (First Five Harmonics)	THD	MAX120			-80	-75	dB
		MAX122			-82	-77	
Spurious-Free Dynamic Range	SFDR	MAX120		75	80		dB
		MAX122		77	82		
Intermodulation Distribution (2nd-Order Terms)	IMD	MAX120 f_A = 98kHz, f_B = 102kHz			-75		dB
		MAX122 f_A = 49kHz, f_B = 51kHz			-75		
CONVERSION TIME							
Synchronous	t_{CONV}	13t_{CLK}	MAX120			1.63	µs
			MAX122			2.60	
Clock Frequency	f_{CLK}		MAX120	0.1		8	MHz
			MAX122	0.1		5	
DIGITAL INPUTS (CLKIN, $\overline{CONVST}$, $\overline{RD}$, $\overline{CS}$)							
Input High Voltage	V_{IH}			2.4			V
Input Low Voltage	V_{IL}					0.8	V
Input Capacitance (Note 4)						10	pF
Input Current		V_{IN} = 0V or V_{DD}				±5	µA
DIGITAL OUTPUTS ($\overline{INT}$/$\overline{BUSY}$, D11-D0)							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 1mA		V_{DD} - 0.5			V
Leakage Current	I_{LKG}	V_{IN} = 0V or V_{DD}, D11-D0				±5	µA
Output Capacitance (Note 4)						10	pF
POWER REQUIREMENTS							
Positive Supply Voltage	V_{DD}	Guaranteed by supply rejection test		4.75		5.25	V
Negative Supply Voltage	V_{SS}	Guaranteed by supply rejection test		-10.80		-15.75	V
Positive Supply Current	I_{DD}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V, $\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = 0V, MODE = 5V			9	15	mA
Negative Supply Current	I_{SS}	V_{DD} = 5.25V, V_{SS} = -15.75V, AIN = 0V, $\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = 0V, MODE = 5V			14	20	mA
Power Dissipation		V_{DD} = 5V, V_{SS} = -12V, AIN = 0V, $\overline{CS}$ = $\overline{RD}$ = $\overline{CONVST}$ = 0V, MODE = 5V			210	315	mW

Note 1: These tests are performed at V_{DD} = 5V, V_{SS} = -15V. Operation over supply is guaranteed by supply rejection tests.
Note 2: Ideal full-scale transition is at +5V -3/2LSB = +4.9963V, adjusted for offset error.
Note 3: Supply rejection defined as change in full-scale transition voltage with the specified change in supply voltage = (FS at nominal supply) - (FS at nominal supply ± tolerance), expressed in LSBs.
Note 4: For design guidance only, not tested.
Note 5: Temperature drift is defined as the change in output voltage from +25°C to T_{MIN} or T_{MAX}. It is calculated as TC = (ΔVREF)/VREF) /ΔT)

500ksps 12-Bit ADCs with Track/Hold and Reference

TIMING CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = -12V or -15V, 100% tested, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 6)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX12_C/E			MAX12_M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup TIme	t_{CS}		0			0			0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CH}		0			0			0			ns
$\overline{CONVST}$ Pulse Width	t_{CW}		30			30			30			ns
$\overline{RD}$ Pulse Width	t_{RW}		t_{DA}			t_{DA}			t_{DA}			ns
Data-Access Time	t_{DA}	C_L = 100pF		40	75			100			120	ns
Bus-Relinquish Time	t_{DH}			30	50			65			80	ns
$\overline{RD}$ or $\overline{CONVST}$ to $\overline{BUSY}$	t_{B0}	C_L = 50pF		30	75			100			120	ns
CLKIN to $\overline{BUSY}$ or $\overline{INT}$	t_{B1}	C_L = 50pF		70	110			150			180	ns
CLKIN to $\overline{BUSY}$ Low	t_{B2}	In Mode 5		45	90			120			150	ns
$\overline{RD}$ to $\overline{INT}$ High	t_{IH}	C_L = 50pF		30	50			75			90	ns
$\overline{BUSY}$ or $\overline{INT}$ to Data Valid	t_{BD}	C_L (Data) = 100pF, C_L ($\overline{INT}$, $\overline{BUSY}$) = 50pF			20			30			35	ns
Acquisition TIme (Note 7)	t_{AQ}		350			350			400			ns
Aperture Delay (Note 7)	t_{AP}			10								ns
Aperture Jitter (Note 7)				30								ps
Clock Setup/Hold Time (Note 7)	t_{CK}		10		50	10		50	10		50	ns

Note 6: Control inputs specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a 1.6V voltage level. Output delays are measured to +0.8V if going low, or +2.4V if going high. For bus-relinquish time, a change of 0.5V is measured. See Figures 1 and 2 for load circuits.

Note 7: For design guidance only, not tested.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

Serial-Output, 400ksps, 14-Bit ADC with Track/Hold and Reference

General Description

The MAX121 is a complete, serial-output, sampling 14-bit analog-to-digital converter (ADC) that combines an on-chip track/hold (T/H) and a low-drift, low-noise, buried-zener voltage reference with fast conversion speed and low power consumption. The throughput rate is as high as 400k samples per second (ksps). The analog input range is ±5V.

Fabricated with a combined bipolar CMOS (BiCMOS) process, the MAX121 utilizes the successive-approximation architecture with a high-speed DAC to achieve both fast conversion speeds and low-power operation. Operating with +5V and -12V or -15V power supplies, power consumption is only 220mW.

The only external components needed are decoupling capacitors for the power-supply and reference voltages.

The MAX121 can be directly interfaced to the serial port of most popular digital-signal processors, and come in space-saving 16-pin DIP and SO packages. The MAX121 operates with TTL-compatible clocks in the 0.5MHz to 8MHz frequency range. All logic inputs and outputs are TTL/CMOS compatible.

Features

- ♦ **14-Bit Resolution; 12-Bit Linearity Over Temp**
- ♦ **400ksps Throughput**
- ♦ **350ns Acquisition Time**
- ♦ **±5V Bipolar Input Range; Overvoltage Tolerant to ±15V**
- ♦ **220mW Power Dissipation**
- ♦ **Continuous-Conversion Mode Available**
- ♦ **20ppm/°C, -5V Internal Reference**
- ♦ **Interfaces to DSP Processors**
- ♦ **16-Pin DIP and SO Packages**

Applications

Digital-Signal Processing

Audio and Telecom Processing

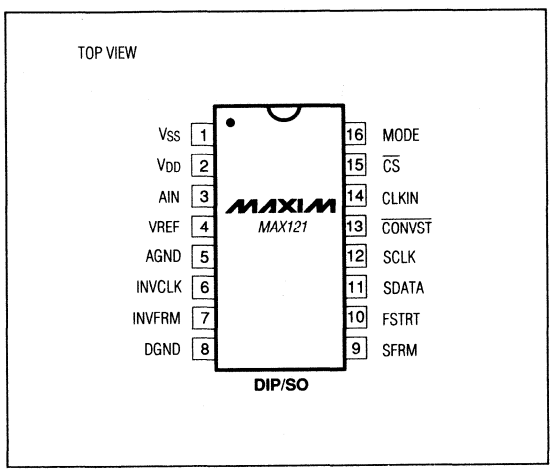
Speech Recognition and Synthesis

High-Speed Data Acquisition

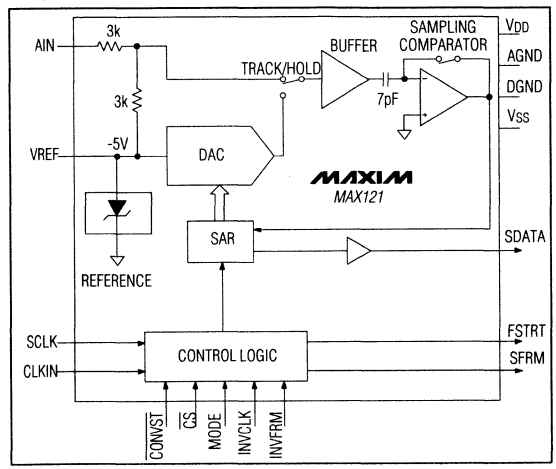
Spectrum Analysis

Data Loggers

Pin Configurations



Functional Diagram



7

19-0009; Rev. 1; 7/92

EVALUATION KIT AVAILABLE

MAXIM

±18-Bit ADC with Serial Interface

General Description

The MAX132 is a CMOS, 18-bit plus sign, serial-output, analog-to-digital converter (ADC). Multi-slope integration provides high-resolution conversions in less time than standard integrating ADCs, allowing operation up to 100 conversions per second. Low conversion noise provides guaranteed operation with ±512mV full-scale input range (2µV/LSB). A simple 4-wire serial interface connects easily to all common microprocessors, and twos-complement output coding simplifies bipolar measurements. Typical supply current is only 60µA and is reduced to 1µA in sleep mode. Four serially programmed digital outputs can be used to control an external multiplexer or programmable-gain amplifier. The MAX132 comes in 24-pin narrow DIP and wide SO packages, and is available in commercial and extended temperature grades.

High resolution, compact size, and low power make this device ideal for data loggers, weigh scales, data-acquisition systems, and panel meters.

Applications

Remote Data Acquisition

Battery-Powered Instruments

Industrial Process Control

Transducer-Signal Measurement
Pressure, Flow, Temperature, Voltage, Current, Resistance, Weight

Features

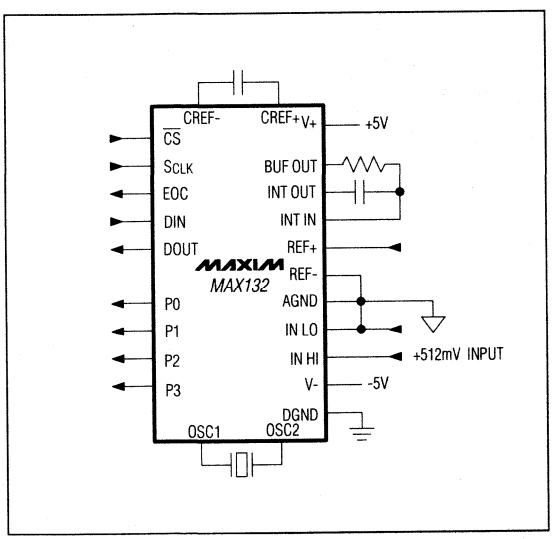
- **Low Supply Current**
  60µA (Normal Operation)
  1µA (Sleep-Mode Operation)
- **±0.006% FSR Accuracy at 16 Conv/Sec**
- **Low Noise: 15µVRMS**
- **Serial I/O Interface with Programmed Output for Mux and PGA**
- **Performs up to 100 Conv/Sec**
- **±10pA Input Current**
- **50Hz/60Hz Rejection**

Ordering Information

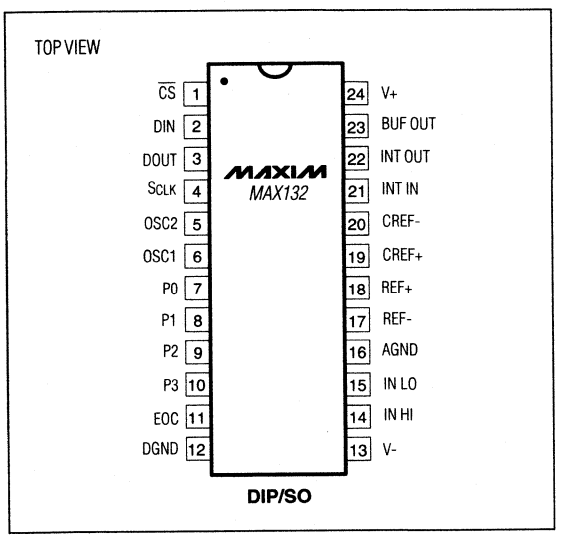
PART	TEMP. RANGE	PIN-PACKAGE
MAX132CNG	0°C to +70°C	24 Narrow Plastic DIP
MAX132CWG	0°C to +70°C	24 Wide SO
MAX132C/D	0°C to +70°C	Dice*
MAX132ENG	-40°C to +85°C	24 Narrow Plastic DIP
MAX132EWG	-40°C to +85°C	24 Wide SO
MAX132MRG	-55°C to +125°C	24 CERDIP**

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configuration



7

±18-Bit ADC with Serial Interface

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V+ to DGND ..... -0.3V < V+ < +6.0V
- V- to DGND ..... +0.3V < V- < -9.0V
- V+ to V- ..... +15V

Analog Input Voltage (any input) ..... V+ to V-
Digital Input Voltage ..... (DGND - 0.3V) to (V+ + 0.3V)
Continuous Power Dissipation
- Narrow Plastic DIP (derate 8.70mW/°C above +70°C) 478mW
- Wide SO (derate 11.76mW/°C above +70°C) 647mW

Operating Temperature Ranges:
- MAX132C_ _ ..... 0°C to +70°C
- MAX132E_ _ ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, DGND = AGND = IN LO = REF LO = 0V, REF HI = 545mV, RINT = 602kΩ, CINT = 0.0047µF, CREF = 0.1µF, f_{CLK} = 32,768Hz, 60Hz mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY						
Resolution					±18	Bits
Zero Error	V_{IN} HI = 0V	T_A = +25°C		0	±0.0076	% of FSR
		T_A = T_{MIN} to T_{MAX}			±0.0168	
Integral Nonlinearity	(Notes 1, 2)	T_A = +25°C		±0.0015	±0.006	% of FSR
Rollover Error	(Note 3)	T_A = +25°C		0	±0.010	% of FSR
		T_A = T_{MIN} to T_{MAX}			±0.032	
Input Voltage Range	IN HI to IN LO, for specified accuracy				±512	mV
	See *Typical Operating Characteristics*				±2	V
Leakage Current	IN HI, IN LO	T_A = +25°C		±2	±10	pA
		T_A = T_{MIN} to T_{MAX}		±12	±250	
Common-Mode Rejection Ratio	IN HI = IN LO	V_{CM} = ±500mV		±0.009	±0.032	% of FSR
		V_{CM} = ±3.0V		±0.25	±0.50	
Common-Mode Range	IN HI = IN LO				±3.0	V
Read-Zero 50Hz/60Hz Range					±3.1	% of FSR
RMS Noise		T_A = +25°C		15		µV
Zero-Reading Drift	(Note 2)			±0.15	±1.5	ppm/°C
Scale Factor Temp. Coefficient	(Note 2)				±5	ppm/°C
POWER REQUIREMENTS						
Positive Supply Voltage			4.5		5.5	V
Negative Supply Voltage			-5.5		-4.5	V
Positive Supply Rejection	V_{IN} HI = 400mV, V- = -5.0V, 4.5V ≤ V+ ≤ 5.5V	T_A = +25°C		±0.003	±0.0061	% of FSR
		T_A = T_{MIN} to T_{MAX}		±0.003	±0.0168	
Negative Supply Rejection	V_{IN} HI = 400mV, V+ = 5.0V, -5.5V ≤ V- ≤ -4.5V	T_A = +25°C		±0.003	±0.0061	% of FSR
		T_A = T_{MIN} to T_{MAX}		±0.003	±0.0168	
Positive Supply Current	Digital input = 0V or V+			60	125	µA
Negative Supply Current	Digital input = 0V or V+			-35	-65	µA
Digital Ground Supply Current	Digital input = 0V or V+			-25	-60	µA
Positive Sleep-Mode Current	Digital input = 0V or V+			1	10	µA
Negative Sleep-Mode Current	Digital input = 0V or V+			-1	-10	µA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, DGND = AGND = IN LO = REF LO = 0V, REF HI = 545mV, RINT = 602kΩ, CINT = 0.0047µF, CREF = 0.1µF, f_{CLK} = 32,768Hz, 60Hz mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL SECTION						
Output High	V_{OH}	DOUT, I_{OUT} = -1mA	3.5	4.3		V
		DOUT, I_{OUT} = -100µA	4.0	4.5		
		EOC, P0-P3, I_{OUT} = -100µA	4.0	4.7		
Output Low	V_{OL}	DOUT, I_{OUT} = 1.6mA		0.1	0.4	V
		EOC, P0-P3, I_{OUT} = 100µA		0.1	0.4	
Input High	V_{IH}	Referred to DGND, 4.5V ≤ V+ ≤ 5.5V, $\overline{CS}$, DIN, S_{CLK}	2.4			V
Input Low	V_{IL}	Referred to DGND, 4.5V ≤ V+ ≤ 5.5V, $\overline{CS}$, DIN, S_{CLK}			0.8	V
Input Current	I_{IN}	$\overline{CS}$, DIN, S_{CLK}, and DOUT when three-stated		±10	±500	nA
Input Capacitance	C_{IN}	$\overline{CS}$, DIN, S_{CLK}, and DOUT when three-stated			5	pF

INTERFACE TIMING

(Test Circuit of Figure 1, Figure 2, V+ = 5V, V- = -5V, DGND = AGND = 0V, T_A = +25°C, unless otherwise noted.) (Note 2)

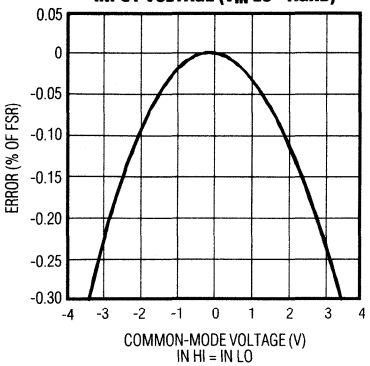
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Lead Time	t_1		500			ns
$\overline{CS}$ Lag Time	t_2		400			ns
S_{CLK} High Time	t_3		400			ns
S_{CLK} Low Time	t_4		300			ns
$\overline{CS}$ High Pulse Width	t_5		1			µs
DIN to S_{CLK} Setup Time	t_6		0			ns
DIN to S_{CLK} Hold Time	t_7		200			ns
DOUT Access Time from Three-State	t_8	See Figure 3			320	ns
Data Valid	t_9				60	ns
DOUT Disable Time to Three-State	t_{10}	See Figure 4			320	ns
Delay to P0-P3 High	t_{11}			230	350	ns
Delay to P0-P3 Low	t_{12}			230	350	ns

Note 1: Maximum deviation from best straight-line fit.
Note 2: Guaranteed by design, not tested.

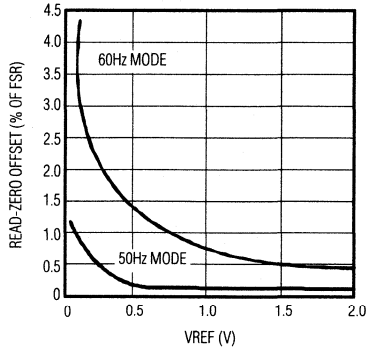
±18-Bit ADC with Serial Interface

Typical Operating Characteristics

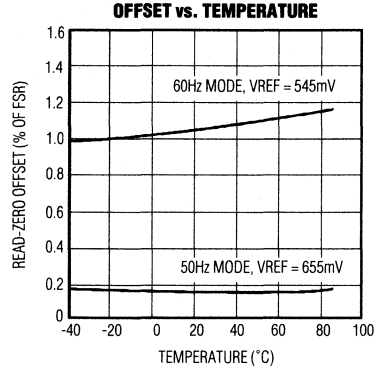
ERROR vs. COMMON-MODE INPUT VOLTAGE (V_{IN} LO - AGND)



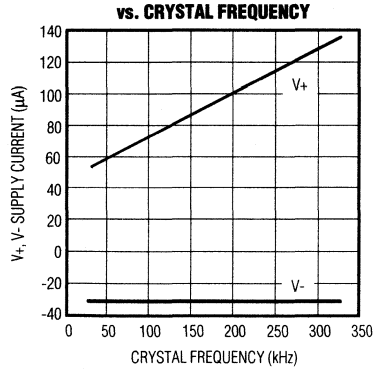
50Hz/60Hz READ-ZERO OFFSET vs. VREF



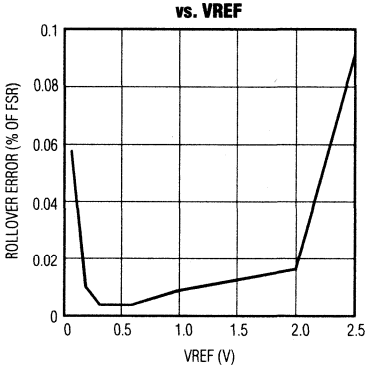
50Hz/60Hz READ-ZERO OFFSET vs. TEMPERATURE



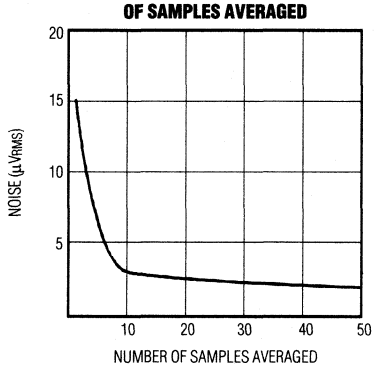
SUPPLY CURRENT vs. CRYSTAL FREQUENCY



FULL-SCALE ROLLOVER ERROR vs. VREF



NOISE vs. NUMBER OF SAMPLES AVERAGED



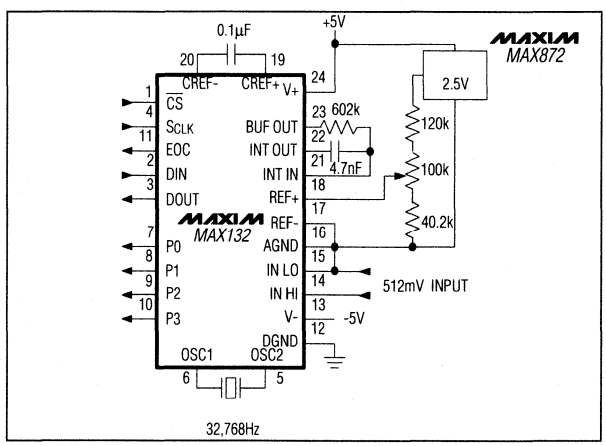


Figure 1. Test and Typical Application Circuit

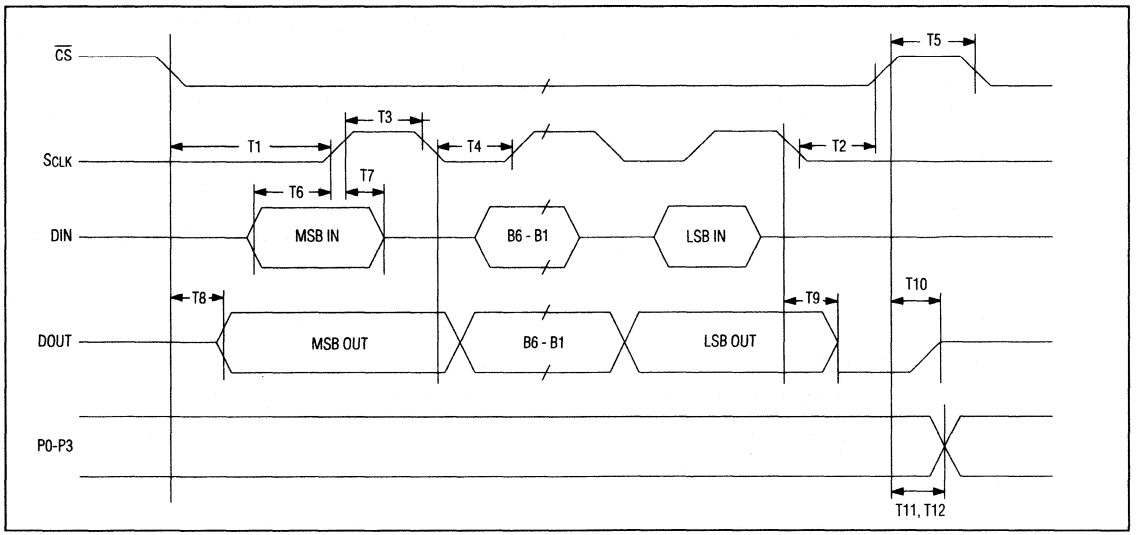


Figure 2. Serial-Mode Timing

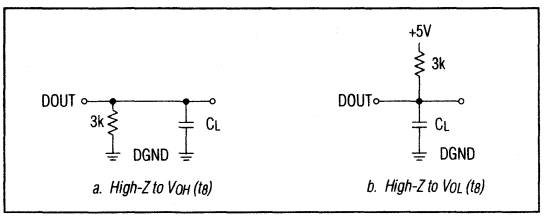


Figure 3. Load Circuits for Access Time

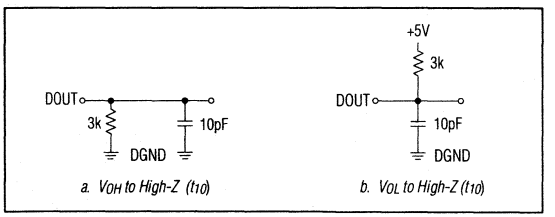


Figure 4. Load Circuits for Disable Time to Three-State

Pin Description

7

PIN	NAME	FUNCTION
1	$\overline{CS}$	$\overline{CHIP\ SELECT}$ Input has 3 functions: 1) When low, selects IC for communication; 2) on rising edge, loads input shift register data into one of the command registers; 3) on falling edge, loads data from one of the output registers into the output shift register.
2	DIN	Serial Data In, D7 first bit in.
3	DOUT	Serial Data Out, D7 first bit out. $\overline{CS}$ controls the three-state output condition.
4	SCLK	Serial Clock Input. On SCLK's rising edge, data is shifted into the internal shift register through DIN. On SCLK's falling edge, data is clocked out of DOUT.
5	OSC2	Oscillator Output 2 is normally connected to a 32,768Hz crystal. No connection with external clock.
6	OSC1	Oscillator Input 1 is normally connected to a 32,768Hz crystal, or may be connected to an external clock.
7	P0	User-programmable output bit 0 - programmed through the serial port
8	P1	User-programmable output bit 1 - programmed through the serial port
9	P2	User-programmable output bit 2 - programmed through the serial port
10	P3	User-programmable output bit 3 - programmed through the serial port
11	EOC	End of Conversion Output goes high at end of conversion.

±18-Bit ADC with Serial Interface

Pin Description (continued)

PIN	NAME	FUNCTION
12	DGND	Digital Ground – power-supply return
13	V-	Negative Supply, nominally -5V
14	IN HI	Positive Analog Input
15	IN LO	Negative Analog Input
16	AGND	Analog Ground
17	REF-	Negative Reference Input
18	REF+	Positive Reference Input
19	CREF+	Positive Reference Capacitor connection
20	CREF-	Negative Reference Capacitor connection
21	INT IN	Integrator Input
22	INT OUT	Integrator Output. To minimize noise, this pin should drive the capacitor's outside foil (negative end).
23	BUF OUT	Buffer-Amplifier Output drives the integrator resistor.
24	V+	Positive Supply, nominally +5V

Functional Description

The MAX132 integrates the input voltage for a fixed period of time, then deintegrates a known reference voltage and measures the time required to reach zero. Good line rejection is achieved by setting the (input) integration time equal to one 50Hz or 60Hz period. The MAX132 has a 50Hz/60Hz mode selection bit that sets the integration time to 655/545 clock periods, respectively, so that 50Hz/60Hz rejection is obtained with a 32,768Hz crystal. The MAX132 is tested and guaranteed at a 16 conv/sec throughput rate. Figure 1 shows the basic MAX132 application circuit, with component values selected for 16 conv/sec.

For applications that don't require 50Hz/60Hz rejection, the MAX132 will operate up to 100 conv/sec at reduced accuracy (typically 0.012% FSR nonlinearity, or ±13 bits). In these applications, the 50Hz mode is recommended because of its longer (655 count) integration time. See *Increased Speed* section.

Analog Design Procedure

Input Voltage Range

The differential input voltage is applied across pins 14 and 15 (IN HI, IN LO). Performance is tested and guaranteed at ±512mV full scale, corresponding to a 2µV/LSB resolution at 18 bits. In general:

Resolution [Volts/LSB] = V_{IN} (FS) /262,144

For larger differential input ranges, consult the *Typical Operating Characteristics* section. Also note in that section how accuracy depends on common-mode input voltage (common-mode is defined here as V_{IN} LO - AGND). The input voltage at IN HI and IN LO should not come within 2V of either the positive of negative supply.

Reference Voltage Selection

Choose the reference voltage based on the input voltage range and the mode (50Hz/60Hz):

$$\text{60Hz Mode: } VREF = \frac{(545 \text{ counts})\,(512)\,(V_{IN\,(FS)})}{262{,}144}$$

or

$$\text{50Hz Mode: } VREF = \frac{(655 \text{ counts})\,(512)\,(V_{IN\,(FS)})}{262{,}144}$$

For 512mV full scale, a 545mV reference voltage is used for the 60Hz mode and a 655mV reference voltage is used for 50Hz mode. The MAX872 is a 10µA supply-current, 2.50V reference that is ideally suited for MAX132 operation. Figure 7 shows how 2.50V can be divided to obtain the desired reference voltage. The reference input accepts voltages anywhere within the converter's power-supply voltage range; however, for best performance, neither REF+ nor REF- should come within 2V of the supplies.

Crystal Frequency

The crystal frequency sets the conversion rate. Use a 32,768Hz crystal frequency for applications that re-

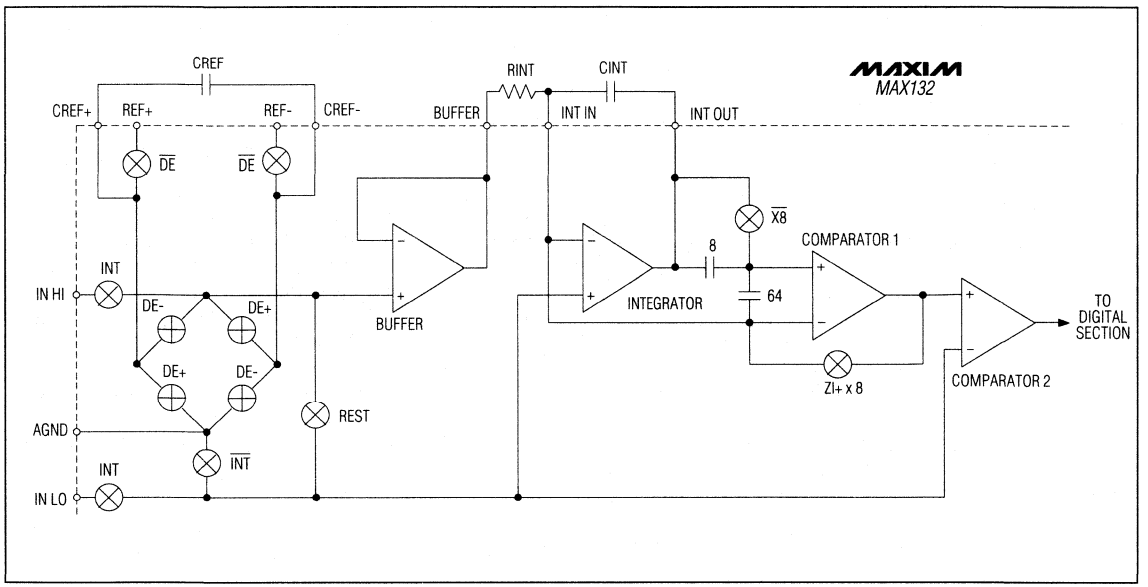


Figure 5. Analog Section Block Diagram

quire 50Hz or 60Hz line rejection. This frequency yields 16 conv/sec. The same clock frequency can be used to reject both line frequencies because the MAX132 integrates for a different number of clock cycles in its 50Hz and 60Hz modes. In each case, the MAX132 integrates for a single complete line cycle (20ms for the 50Hz mode, 16.67ms for the 60Hz mode).

Figure 6 shows the internal oscillator drive circuitry used with external crystals.

Refer to the *Increased Speed* section for operation at higher conversion rates.

Manufacturers of miniature quartz crystals include:

Seiko Instruments (USA)	Phone (213) 517-7833
	FA X (213) 517-7792
Micro Crystal (Switzerland)	Phone +41 (65) 512111
	FAX +41 (65) 530557

Integrator Components

The MAX132 requires an integrator resistor (RINT) and capacitor (CINT), a reference capacitor (CREF), and a crystal. All MAX132 tests are performed with a 32,768Hz crystal frequency. The crystal frequency, reference voltage, and integrator current determine the values of RINT and CINT.

Integrator Resistor

The integrator resistor sets the maximum integrator output current for the integrate phase. A 602kΩ metal-film integrator resistor is recommended for use with reference voltages between 545mV and 655mV. Best linearity is achieved when integration current (I_{INT}) does not exceed 2.0µA. For other reference voltages, select RINT as follows:

$$RINT = \frac{VREF}{I_{INT}}; \quad 0.5\mu A < I_{INT} < 2.0\mu A$$

Integrator Capacitor

The oscillator frequency, integrator resistor, and integrator capacitor set the maximum integrator output-voltage swing for full-scale reading. The integrator voltage swing is about 3V with a 602kΩ integrator resistor and a 4.7nF integrator capacitor when the clock frequency is 32,768Hz. If different clock frequencies are used, select CINT using the following equations:

$$CINT = \frac{(V_{IN(FS)})\,(t_{INT})}{(RINT)\,(V_{SWING})}; \quad 1V < V_{SWING} < 3.5V$$

$$t_{INT} = \frac{545}{f_{OSC}} \text{ for 60Hz mode;}$$

$$t_{INT} = \frac{655}{f_{OSC}} \text{ for 50Hz mode}$$

The integrator capacitor's dielectric absorption directly affects integral nonlinearity. High-quality, metal-film capacitors are recommended in the following order of preference: polypropylene, polystyrene, polycarbonate, and polyester (Mylar). The polyester capacitor will generate some integral nonlinearity.

Reference Capacitor

The reference capacitor value must be small enough to fully charge from a discharged state on power-up in the desired time, and large enough so the charge does not droop excessively during a conversion. The reference capacitor is normally 0.1µF for all oscillator frequencies. For applications that require a physically smaller capacitor, the equation below will maintain CREF proportionality.

$$CREF = \frac{0.0033}{f_{OSC}}$$

The reference capacitor must have low leakage, since it stores the reference voltage while floating during the deintegrate phase. Any leakage or charge loss during this phase changes the scale factor, and will cause an error. Appropriate metal-film capacitors recommended for their low-leakage characteristics (in this order) are polypropylene, polystyrene, polycarbonate, and polyester. At temperatures above +85°C, capacitor leakage may affect accuracy. In such cases, increasing the value of CREF will help.

The main source of rollover voltage error is common-mode voltage, which is caused by the reference capacitor losing or gaining charge to stray capacitance. A positive signal with a large common-mode voltage can cause the reference capacitor to gain charge (increase voltage). In contrast, the reference capacitor will lose charge (decrease voltage) when deintegrating a negative input signal. Rollover error is a direct result of the difference in reference to positive or negative input voltages. Use an optimum reference capacitor to hold rollover error under one-half count for worst-case conditions. A common-mode voltage near or at AGND minimizes rollover error caused by these sources.

Digital Interface

Serial data at DIN is sent in 8-bit packets and is shifted into the internal 8-bit shift register with each rising edge of S_{CLK}. The data is then latched into either command input register 0 or command input register 1, as determined by the LSB of the data sent, and is latched on the rising edge of CHIP SELECT ($\overline{CS}$). Data is clocked out of the selected output register on each falling edge of S_{CLK}. D7(MSB) must be the first data bit to be shifted in and is the first bit to be shifted out.

Because data is shifted out at the same time command data is shifted in, command data must be clocked in on the previous 8-bit read-write cycle to receive conversion data in the present cycle.

Since there is no internal power-on reset, initialize the MAX132 immediately after power-up to insure correct operation.

Table 1 defines each bit of five registers: the two command input registers, output register 0, output register 1, and the status output register.

Command Input Register 0

Register-Set Bits

Data bits D1 and D2 of command register 0 (RS1 and RS0) determine the data to be read on the data bus. These bits select which register outputs data to the bus. Table 2 defines the bit values that determine which register is read on the next cycle (see Figure 8).

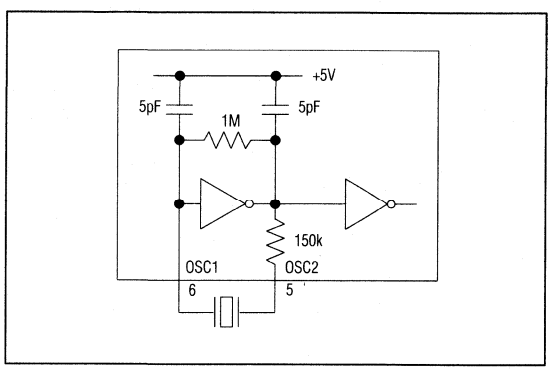


Figure 6. MAX132 Internal Oscillator Drive Circuitry

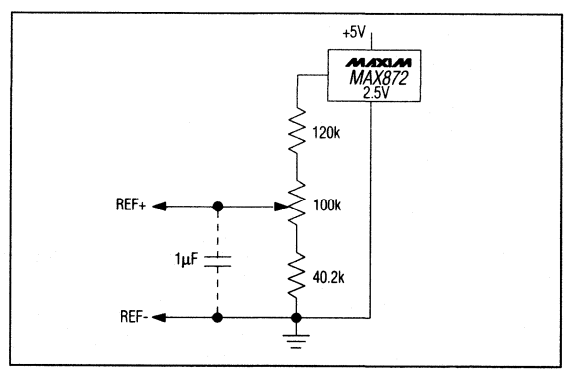


Figure 7. Dividing MAX872 to Generate the MAX132's Reference Voltage

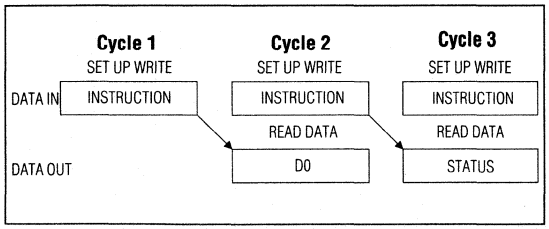


Figure 8. Instruction and Data Sequencing

Read-Zero Bit

The read-zero bit allows the ADC to calibrate on command for zero offset. The read-zero bit, when set to 1, internally shorts the inputs; when a start-conversion command is given, the zero error is converted. Subtract the results from the standard external measurement conversion when the read-zero conversion ends. If the read-zero bit is set to 0, the converter measures the voltage between IN HI and IN LO once a start bit is given. Take a new zero reading periodically and whenever the ambient temperature, the reference voltage, or the common-mode input voltage are changed.

Averaging multiple read-zero measurements provides the most accurate read-zero value.

Sleep Bit

When the sleep bit is set to 1, and 1 is written to D5 in command input register 0, the low-power sleep mode starts when EOC = 1. In sleep mode, the supply current is typically 1mA, the oscillator shuts down, and data can be read. When sleep mode is released, the analog circuitry needs time to stabilize before the next conversion starts. Accomplish this by writing a separate instruction to emerge from sleep mode, and wait at least one conversion cycle before writing a start instruction.

50Hz/60Hz

With a 32,768Hz crystal, the 50Hz/60Hz bit sets the integrate period equal to one line cycle for 50Hz/60Hz environments. When D6 (in command input register 0) is set to 0, the integrate count is an integer multiple of 60Hz (32,768Hz/60Hz = 546 counts). When D6 is set to 1, the integrate input count is an integer multiple of 50Hz (32,768Hz/50Hz = 655 counts). Achieve the greatest AC rejection by adjusting the integration period for 50Hz or 60Hz.

Start Conversion Bit

The start conversion bit (D7) in command input register 0 initiates a conversion when set to 1. The MAX132

Table 2. Register Set-Bit Definitions

RS0	RS1	DEFINITIONS
0	0	Selects register 0; output for data bits B3-B10
1	0	Selects register 1; output for data bits B11-B18
0	1	Selects register 2; output for status bits B0-B2, polarity, sleep, integrating, EOC and collision bit
1	1	Invalid data

Table 1. Register Map of Input and Output Data

REGISTER		DATA BIT							
		D7	D6	D5	D4	D3	D2	D1	D0
Command Input Register 0	"1"	Start Convert	50Hz	Sleep	Read Zero	Don't Care	RS0*	RS1*	0
	"0"	Returns to 0 at EOC	60Hz	Awake	Read V_{IN}	Don't Care			
Command Input Register 1		Set P3 Output	Set P2 Output	Set P1 Output	Set P0 Output	Don't Care	Don't Care	Don't Care	1
Output Register 0 RS1 = 0, RS0 = 0		B10	B9	B8	B7	B6	B5	B4	B3
Output Register 1 RS1 = 0, RS0 = 1		B18 MSB	B17	B16	B15	B14	B13	B12	B11
Output Status Register RS1 = 1, RS0 = 0	"1"	Collision	EOC	Integrating Input	Sleep	- Polarity	B2	B1	B0 LSB
	"0"	No Collision	Converting	Not Integrating	Awake	+ Polarity			

***NOTE:** REFER TO TABLE 2.

immediately starts a conversion, stops at conversion end, and then waits for the next start-bit command. A start instruction is needed to initiate each conversion.

To initiate a continuous data stream, write a separate start command for each conversion in three ways:

1. Wait longer than a known conversion time and then write another start command.
2. Poll either the EOC status register bit or the EOC line to determine conversion end and start time for the next conversion. EOC becomes 1 at conversion end at count 0000 of the conversion counter (Figure 9).
3. Set the start bit to 1 before a conversion end. The internal conversion counter is then checked for its count. If the count is 0000 (EOC = 1), a new conversion starts and the conversion counter is set to 0001. The start bit resets to 0 after 5 clock cycles. The MAX132 will not check the start bit again until the conversion counter returns to a 0000 count. This means a start command can be given any time after 0005 internal conversion count; the next conversion starts when the counter returns to 0000.

Command Input Register 1

User-Programmable Output Bits P0 to P3

Command input register 1 always has data bit D0 = 1. Data bits D4 to D7 of command register 1 control the states of the user-programmable output pins P0 to P3, respectively (see Table 1). These four outputs can be used to control an external multiplexer, programmable-gain amplifier, or other devices.

Output Registers

Register 0

Register 0 contains the low-byte (bits B3-B10) conversion data. New data is available after EOC goes high. Access register 0 by setting RS0 and RS1 to 0. Output data is the sum of system offset (read zero) plus the results of the external input voltage measurement.

Register 1

Register 1 contains the high-byte (bits B11-B18) data. Data is in a twos-complement format, where the polarity bit is a 1 for negative polarity data. Access register 1 by setting control bits RS0 = 1 and RS1 = 0 when writing to the command input register.

Status Register

The B0, B1, and B2 bits are located in the status register. At the end of each conversion these bits are updated and read back from the status register. For full 18-bit resolution, use bits B0-B2. To stabilize the result of these 18 bits, use an averaging technique.

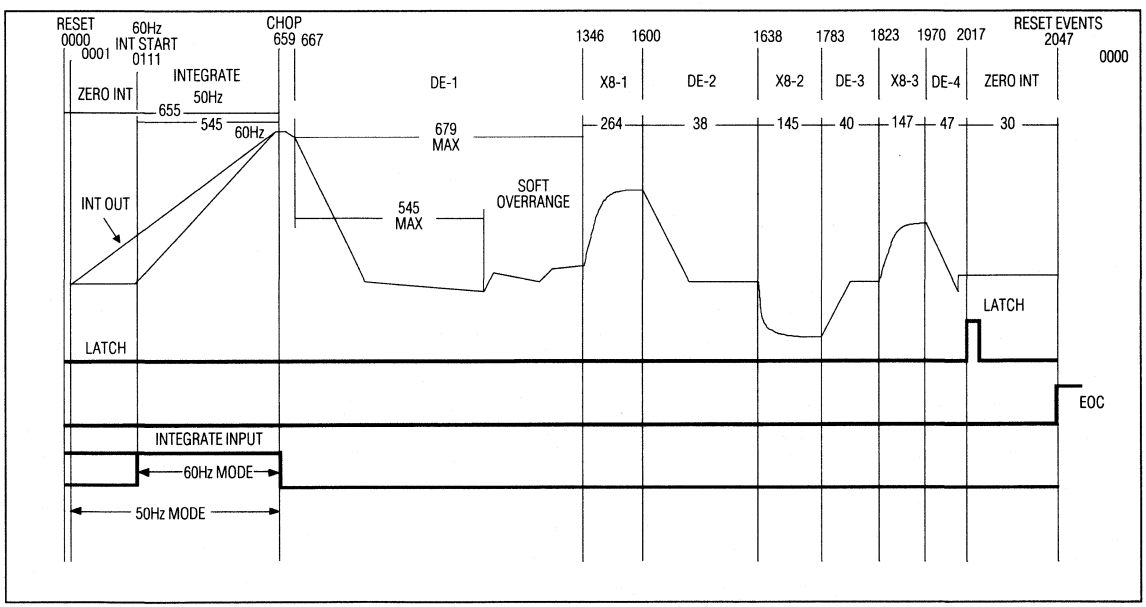


Figure 9. Conversion Timing (Negative Input Shown)

Table 3. Overrange Values for Resolution Used

Bits Used	Resolution Bits	Soft Overrange Start Value	Hard Overrange Maximum Value
B18-B3	±15	34,880	43,805
B18-B2	±16	69,760	87,610
B18-B1	±17	139,520	175,220
B18-B0	±18	279,040	350,440

The integrate (INT) bit is set to 1 at the beginning of the integration phase and becomes 0 at the end. Poll INT to determine the earliest time the input can be changed without affecting the conversion.

The end-of-conversion (EOC) bit signals conversion status. If EOC is 1, the conversion is complete and the ADC waits in zero-integrate mode at time = 0000 for the next start instruction. A conversion cycle has 2048 counts. EOC becomes 1 at count 0000 and 0 at count 0001.

The collision bit warns the microprocessor (µP) that the register's data was changed during the read cycle. A collision occurs if the internal result latches on the falling edge of $\overline{CS}$, causing the collision bit to be set to 1 on the rising edge of the next $\overline{CS}$. This occurs because these two pulses are asynchronous. Once the status register is read, the collision bit is reset to 0. To determine collision status, read the status register collision bit before and after reading output registers 0 and 1.

Collisions will not occur if a conversion's read cycle is completed before the next conversion begins.

Sequence Counter and Results Counter

A binary sequencing counter controls the conversion phase's sequencing (or timing). In integrate phase, both start and stop occur at preset counts. The deintegration phases start at predetermined counts, but are terminated when the comparator detects zero crossing at the integrator output.

The results counter accumulates counts during all deintegrate phases. It is an up/down binary counter, with the count direction determined by the deintegration polarity. In the first deintegrate phase, the results counter counts by 512. Since the second deintegrate phase deintegrates a residual voltage multiplied by 8, the results counter increments or decrements by 64 during this phase. It increments or decrements by 8 during the third deintegrate phase, and by 1 during the fourth deintegrate phase. The results counter content transfers to the results register at each conversion end.

Overrange Indication

B18 is not strictly an overrange bit. This 19th bit is necessary to exploit the converter's full range, and to ensure that a full 18-bit result can be achieved after a zero reading has been deducted.

The actual overrange value is a function of the number of bits of resolution used. Table 3 lists the overrange values for different resolutions.

The MAX132 has two overrange levels (Figure 9). The first level is a soft overrange that is set by the user. Overrange is arbitrarily set at a value, preferably less than the 279,040 (including any zero offset) raw counts soft limit. A nonlinearity step of about 64 counts occurs at raw count 279,040 and again at 330,240 counts.

The second level is a hard overrange with a maximum value of 350,440 counts. Attempts to deintegrate values greater than this will result in a value of 350,440 counts.

Conversion Phases

For an explanation of conversion phases, refer to Figures 5 and 9.

Integrate Phase

The MAX132 integrates the input signal by connecting the integrator's noninverting input to IN LO, and the buffer input to IN HI. The integration period is 545 counts for 60Hz mode and 655 counts for 50Hz mode.

Deintegrate Phase

The integrator capacitor's voltage polarity at the end of integrate phase determines the polarity of the first deintegration phase. The first deintegration phase ends when the comparator detects that the integration capacitor has been discharged. The MAX132 then goes into a rest phase, where both the buffer input and the integrator's noninverting input are connected to AGND, integrating the system offset.

Near the end of the maximum allowable deintegration period, the integrator capacitor voltage polarity is again sampled, resulting in either a positive or negative deintegrate cycle.

Rest Phase

A rest phase follows each deintegrate phase. Rest phase starts when the integrator crosses zero and ends when the maximum count for that deintegration phase has been reached.

First Times-Eight Phase

When the zero crossing is detected at the end of the deintegrate phase, deintegration continues until the next clock cycle. This causes the integrator to overshoot zero crossing slightly, leaving a small residual voltage on the integration capacitor. The first times-eight (X8) phase inverts and multiplies this residual by a factor of 8.

Second Deintegrate Phase

The second deintegrate phase deintegrates residual voltage on the integration capacitor that has been through the X8 phase. Since the voltage across the integration capacitor has been multiplied by 8, each deintegration clock cycle corresponds to 1/8 of one clock cycle during the first deintegration.

±18-Bit ADC with Serial Interface

Additional Times-Eight and Deintegrate Phases

At the end of the second and third deintegration phases, the device performs a X8 multiplication of the residual voltage left on the integration capacitor. After each of these X8 multiplications, a deintegration occurs, resulting in a second, third, and fourth deintegration phase. Each time the residual voltage on the integration capacitor is multiplied by 8, the following deintegration has 8 times finer resolution.

Zero-Integrate Phase

The zero-integrate phase zeros out the integrator to prepare for the next integration (Figure 9). This phase occurs at the beginning and end of each conversion. At power-up, or in the hold mode prior to a conversion, the MAX132 continues to zero integrate until a conversion starts. When a conversion starts in 60Hz mode, another 111 clocks of zero integrate are completed before the beginning of a conversion. In 50Hz mode, only one additional zero integrate is performed before the conversion starts. An additional 20 clocks of zero integrate occur at each conversion end.

Applications Information

Increased Speed

The MAX132 is tested with a 32,768Hz clock frequency, which results in 16 conv/sec. Up to 96 conv/sec may be achieved with higher clock frequencies and some changes in component values, as shown in Table 4. Operation at higher conversion rates reduces accuracy, and care must be taken to get the best results

Although either the 50Hz or 60Hz mode can be used, complete rejection of 50Hz or 60Hz normal-mode noise at conversion rates above 16 conv/sec is impossible. Use the 50Hz mode when operating at more than 16 conv/sec, irrespective of the local line frequency. The 50Hz mode uses a slightly longer integration time than the 60Hz mode, and generally gives lower-noise performance.

Table 4 lists the crystal frequencies and integrating capacitor values for the 50Hz and 60Hz modes for various conversion rates, although the 50Hz mode is recommended for clock rates above 32,768Hz.

The raw data can be used where highest accuracy is not required, and the least significant bits can be ignored. Improvements in accuracy can be gained by averaging both the data and the zero readings, although data averaging compromises the converter's speed performance.

To maximize throughput, take zero readings only when necessary, i.e. when the common-mode voltage changes. It is not normally necessary to take a zero reading after every data reading, and an excessive number of zero readings reduces the converter's effective speed.

Noise Reduction

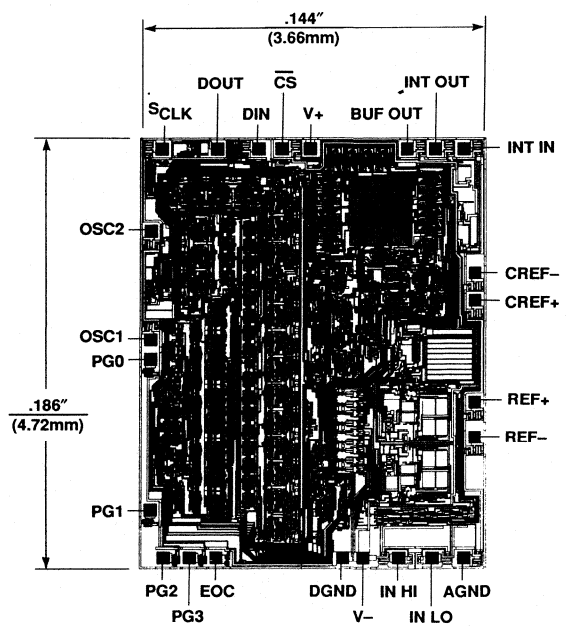
To minimize noise, each supply must be bypassed to GND with a 0.1µF capacitor. A ground plane should also be placed under the analog circuitry. To minimize the coupling effects of stray capacitance, keep digital lines as far from analog components and lines as possible. Also, connect the integrator capacitor's outside foil to the INT OUT pin to minimize stray capacitive coupling. If possible, keep the digital interface inactive while the MAX132 is converting.

Table 4. Crystal Frequencies and Integrator Capacitors for 50Hz to 60Hz Operation

Conv/ Sec	Hz	CINT/60Hz (pF)	CINT/50Hz (pF)	R (kΩ)
16	32,768	4700	6800	602
32	65,536	2700	3300	602
48	98,304	1800	2000	602
64	131,072	1200	1500	602
80	163,840	1000	1200	602
96	196,608	820	1000	602

NOTE: CAPACITOR VALUES ARE FOR A 3.0V INTEGRATOR SWING.

Chip Topography



19-4131; Rev. 0; 9/91

Call 1-800-998-8800 for a Complete Datasheet

MAXIM

15-Bit ADC with Parallel Interface

General Description

The MAX135 is a CMOS 15-bit, binary-output analog-to-digital converter (ADC). Multi-slope integration provides low-noise and high-resolution conversions in less time than standard integrating ADCs: The MAX135 is tested at 16 conversions per second, but operates at up to 6 times that rate. The MAX135 uses Super LSBs with data averaging to achieve 18-bit resolution.

Supply current is 125µA maximum during normal operation and only 10µA maximum in sleep mode. Low conversion noise allows tested operation at only 300mV full scale (15µV per LSB). A simple 8-bit parallel data bus and three control lines easily interface to all common microprocessors, and twos-complement output coding simplifies bipolar measurements.

High resolution and compact size make the MAX135 ideal for data loggers, numerical control systems, weigh scales, data-acquisition systems, and panel meters. The MAX135 comes in 28-pin DIP and SO packages in both commercial and extended temperature grades.

Applications

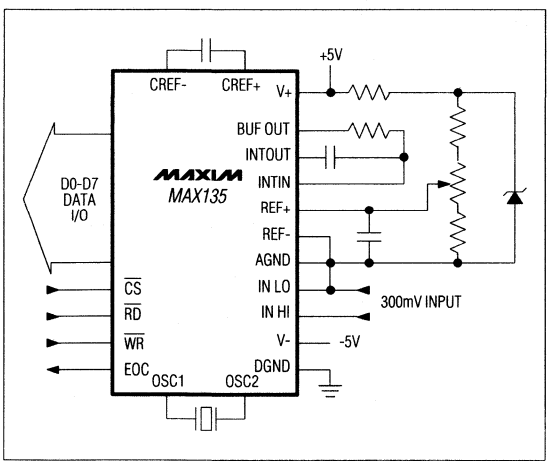
Data Acquisition

Battery-Powered Instruments

Control Applications

Analog-Signal Measurement
Pressure, Flow, Temperature, Voltage, Current, Resistance, Weight

Functional Diagram



Features

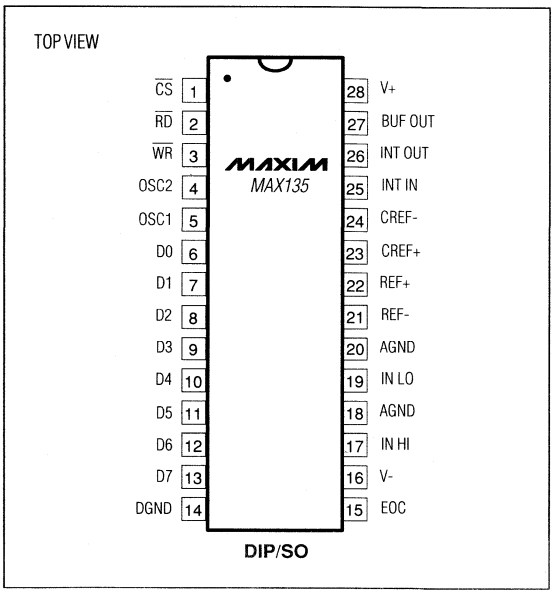
- ♦ **15-Bit, Multi-Slope Integrating ADC**
- ♦ **15µV Resolution at 16 Conv/Sec**
- ♦ **Low Supply Current**
  - **125µA Max (Normal Operation)**
  - **10µA Max (Sleep-Mode Operation)**
- ♦ **±0.005% Accuracy at 16 Conv/Sec**
- ♦ **3 Super Bits for 18-Bit Resolution**
- ♦ **Low Noise - Operates at 300mV Full Scale**
- ♦ **Easy µP Interface - 8-Bit Parallel Data Bus**
- ♦ **±10pA Input Leakage Current**
- ♦ **Small 28-Pin DIP and SO Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX135CPI	0°C to +70°C	28 Plastic DIP
MAX135CWI	0°C to +70°C	28 Wide SO
MAX135C/D	0°C to +70°C	Dice*
MAX135EPI	-40°C to +85°C	28 Plastic DIP
MAX135EWI	-40°C to +85°C	28 Wide SO

* *Contact factory for dice specifications.*

Pin Configuration



15-Bit ADC with Parallel Interface

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- V+ to DGND ..... -0.3V < V+ < +6.0V
- V- to DGND ..... +0.3V < V- < -9.0V
- V+ to V- ..... +15V

Analog Input Voltage (any input) ..... V+ to V-
Digital Input Voltage ..... (DGND - 0.3V) to (V+ + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
- 28-Pin Plastic DIP (derate 9.09mW/°C above +70°C) 786mW
- 28-Pin Wide SO (derate 12.50mW/°C above +70°C) . 688mW

Operating Temperature Ranges:
- MAX135C_ _ ..... 0°C to +70°C
- MAX135E_ _ ..... -40°C to +85°C

Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, DGND = AGND = IN LO = REF- = 0V, REF+ = 545mV, RINT = 402kΩ, CINT = 0.0047µF, CREF = 0.1µF, f_{CLK} = 32,768Hz, 60Hz mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution		(Note 1)				20,000	LSB
Zero Error		IN HI = 0V	T_A = +25°C			±2	LSB
			T_A = T_{MIN} to T_{MAX}			±5	
Nonlinearity		(Notes 2, 3)	T_A = +25°C			±2	LSB
Rollover Error		(Note 4)	T_A = +25°C			±3	LSB
			T_A = T_{MIN} to T_{MAX}			±10	
Conversion Time				63			ms
Input Voltage Range		IN HI to IN LO				±300	mV
Leakage Current		IN HI, IN LO	T_A = +25°C			±10	pA
			T_A = T_{MIN} to T_{MAX}			±250	
Common-Mode Rejection		IN HI = IN LO	V_{CM} = ±500mV		3	10	LSB
			V_{CM} = ±3.5V		70		
Common-Mode Range		IN HI = IN LO			±3.5		V
Read Zero (50Hz/60Hz Range)						±2000	LSB
Noise (Zero-Reading Mode)		IN HI = IN LO	T_A = +25°C		1.5		LSB
Zero-Reading Drift		(Note 3)				0.1	LSB/°C
Scale Factor Temp. Coefficient		(Note 3)				5	ppm/°C
Positive Supply Rejection		FS change, V- = -5.0V, +4.5V ≤ V+ ≤ +5.5V				2	LSB
Negative Supply Rejection		FS change, V+ = 5.0V, -4.5V ≤ V- ≤ -5.5V				2	LSB
Positive Supply Current	I+				60	125	µA
Negative Supply Current	I-				-35	-65	
Digital Ground Supply Current					-25	-60	
Positive Sleep-Mode Current	I+				4	10	µA
Negative Sleep-Mode Current	I-				-4	-10	
Digital Ground Sleep-Mode Current					0	±2	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, DGND = AGND = IN LO = REF- = 0V, REF+ = 545mV, RINT = 402kΩ, CINT = 0.0047µF, CREF = 0.1µF, f_{CLK} = 32,768Hz, 60Hz mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL SECTION						
Output High	V_{OH}	D0-D7, I_{OUT} = -1mA	3.5	4.3		V
		DO-D7, I_{OUT} = -100µA	4.0	4.5		
		EOC, I_{OUT} = -100µA	4.0			
Output Low	V_{OL}	D0-D7, I_{OUT} = 1.6mA		0.2	0.4	V
		EOC, I_{OUT} = 100µA			0.4	
Input High	V_{IH}	Referred to DGND, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$	2.4			V
Input Low	V_{IL}	Referred to DGND, $\overline{CS}$, $\overline{WR}$, $\overline{RD}$			0.8	V
Input Current	I_{IN}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, D0-D7 when three-stated		±10	±500	nA
Input Capacitance	C_{IN}	$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, D0-D7 when three-stated		5		pF

TIMING CHARACTERISTICS

(Test circuit of Figures 1 and 2, V+ = 5V, V- = -5V, DGND = AGND = 0V, T_A = +25°C, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_1		0			ns
$\overline{WR}$ Data-Setup Time	t_2		200	<100		ns
$\overline{WR}$ Pulse Width	t_3		200	<100		ns
Data Hold after $\overline{WR}$	t_4		0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_5		0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_6		0			ns
$\overline{RD}$ to Data Valid	t_7		480	240		ns
Bus-Relinquish Time	t_8		380	190		ns
$\overline{WR}$ to $\overline{RD}$	t_9		300			ns
$\overline{RD}$ to $\overline{WR}$	t_{10}		200			ns
Delay between Write Operations	t_{11}		500	<250		ns

Note 1: 18-bit resolution achieved by averaging multiple conversions.
Note 2: Max deviation from best straight line fit, 1LSB = 15.63µV.
Note 3: Guaranteed by design, not tested.
Note 4: Difference in reading for equal positive and negative inputs near full scale.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

1Msps, µP-Compatible, 8-Bit ADC with Power-Down

General Description

The MAX153 high-speed, microprocessor (µP)-compatible, 8-bit analog-to-digital converter (ADC) uses a half-flash technique to achieve a 660ns conversion time, and digitizes at a rate of 1Msps. It operates with single +5V or dual ±5V supplies and accepts either unipolar or bipolar inputs. A power-down pin reduces current consumption to a typical value of 1µA. The part returns from power-down to normal operating mode in less than 200ns.

The MAX153 is DC and dynamically tested. Its µP interface appears as a memory location or input/output port that requires no external interface logic. The data outputs use latched, three-state buffered circuitry for direct connection to a µP data bus or system input port. The ADC's input/reference arrangement enables ratiometric operation.

Applications

Digital-Signal Processing

High-Speed Data Acquisition

Telecommunications

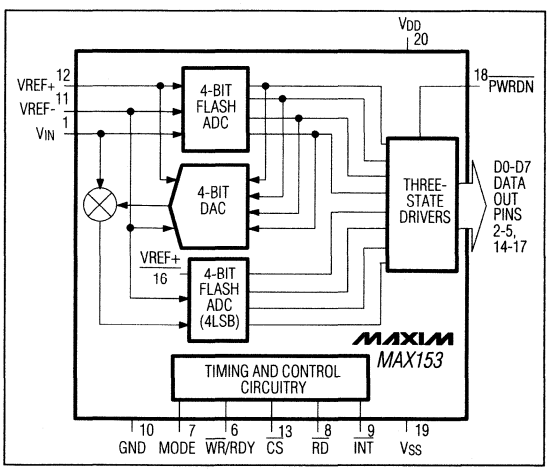
High-Speed Servo Loops

High-Speed/Low-Power Applications

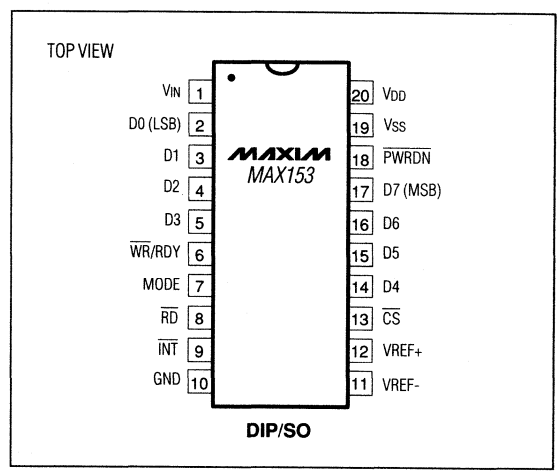
Features

- ♦ **660ns Conversion Time**
- ♦ **Internal Track/Hold**
- ♦ **1Msps Throughput**
- ♦ **Low Power: 40mW Typ (Operating Mode)**
  5µW Typ (Power-Down Mode)
- ♦ **1MHz Full-Power Input Bandwidths**
- ♦ **20-Pin Shrink Small-Outline Package (SSOP) and Narrow DIP/SO Packages**
- ♦ **No External Clock Required**
- ♦ **Unipolar/Bipolar Inputs**
- ♦ **Single +5V or Dual ±5V Supplies**
- ♦ **Ratiometric Reference Inputs**
- ♦ **DC and Dynamic Performance Tested**

Functional Diagram



Pin Configuration



19-2949; Rev. 0; 11/91

EVALUATION KIT AVAILABLE

MAXIM

8-/4-Channel ADCs with Simultaneous T/Hs and Reference

General Description

The MAX155/MAX156 are high-speed, 8-bit, multi-channel analog-to-digital converters (ADCs) with simultaneous track/holds (T/Hs) to eliminate timing differences between input channel samples. The MAX155 has 8 analog input channels, and the MAX156 has 4 analog input channels. Each channel has its own T/H, and all T/Hs sample at the same instant. The ADC converts a channel in 3.6µs and stores the result in an internal 8x8 RAM. The MAX155/MAX156 also feature a 2.5V internal reference and power-down capability, providing a complete, sampling data-acquisition system.

When operating from a single +5V supply, the MAX155/MAX156 perform either unipolar or bipolar, single-ended or differential conversions. For applications requiring wider dynamic range or bipolar conversions around ground, the V_{SS} supply pin may be connected to -5V.

Conversions are initiated with a pulse to the $\overline{WR}$ pin, and data is accessed from the ADC's RAM with a pulse to the $\overline{RD}$ pin. A bidirectional interface updates the channel configuration and provides output data. The ADC may also be wired for output-only operation. The MAX155 comes in 28-pin DIP and wide SO packages, and the MAX156 comes in 24-pin narrow plastic DIP and 28-pin wide SO packages.

Applications

Phase-Sensitive Data Acquisition

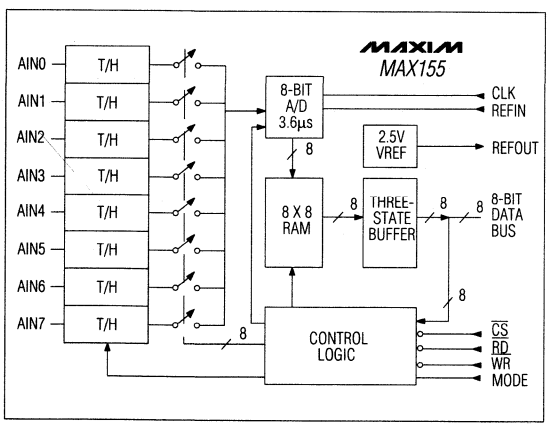
Vibration and Waveform Analysis

DSP Analog Input

AC Power Meters

Portable Data Loggers

Functional Diagram



Features

- ♦ 8 Simultaneously Sampling Track/Hold Inputs
- ♦ 3.6µs Conversion Time per Channel
- ♦ Unipolar or Bipolar Input Range
- ♦ Single-Ended or Differential Inputs
- ♦ Mixed Input Configurations Possible
- ♦ +2.5V Internal Reference
- ♦ Single +5V or Dual ±5V Supply Operation

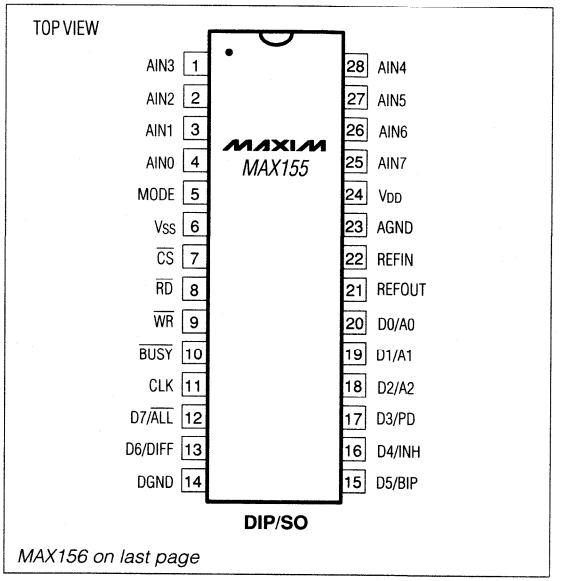
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX155ACPI	0°C to +70°C	28 Plastic DIP	±1/2
MAX155BCPI	0°C to +70°C	28 Plastic DIP	±1
MAX155ACWI	0°C to +70°C	28 Wide SO	±1/2
MAX155BCWI	0°C to +70°C	28 Wide SO	±1
MAX155BC/D	0°C to +70°C	Dice*	±1

Ordering information continued on last page.

* *Contact factory for dice specifications.*

Pin Configurations



MAX156 on last page

7

8-/4-Channel ADCs with Simultaneous T/Hs and Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +6V
V_{DD} to DGND ..... -0.3V, +6V
AGND to DGND ..... -0.3V, V_{DD} +0.3V
V_{SS} to AGND ..... +0.3V, -6V
V_{SS} to DGND ..... +0.3V, -6V
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$, CLK, MODE to DGND ..... -0.3V, V_{DD} +0.3V
$\overline{BUSY}$, D0-D7 to DGND ..... -0.3V, V_{DD} +0.3V
REFOUT to AGND ..... -0.3V, V_{DD} +0.3V
REFIN to AGND ..... -0.3V, V_{DD} +0.3V
AIN to AGND ..... V_{SS} -0.3V, V_{DD} +0.3V
Output Current (REFOUT) 30mA

Continuous Power Dissipation (T_A = +70°C)
24-Pin Plastic DIP (derate 8.7mW/°C above +70°C) .. 696mW
24-Pin CERDIP (derate 12.5mW/°C above +70°C) .. 1000mW
28-Pin Plastic DIP (derate 9.09 mW/°C above +70°C) .. 727mW
28-Pin Wide SO (derate 12.5mW/°C above +70°C) .. 1000mW
28-Pin CERDIP (derate 16.67mW/°C above +70°C) . 1333mW
Operating Temperature Ranges:
MAX155/MAX156_C_ _ ..... 0°C to +70°C
MAX155/MAX156_E_ _ ..... -40°C to +85°C
MAX155_MJI ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, REFIN = +2.5V, External Reference, AGND = DGND = 0V, V_{SS} = 0V or -5V, f_{CLK} = 5MHz External, Unipolar Range, Single-Ended Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution				8			Bits
Integral Linearity Error			MAX15_A			±1/2	LSB
			MAX15_B			±1	
No Missing Codes Resolution		Guaranteed monotonic		8			Bits
Offset Error (Unipolar)			MAX15_A			±1/2	LSB
			MAX15_B			±1	
Offset Error (Bipolar)			MAX15_A			±1	LSB
			MAX15_B			±2	
Gain Error		Unipolar	MAX15_A			±1	LSB
			MAX15_B			±1	
		Bipolar	MAX15_A			±1	
			MAX15_B			±2	
Channel-to-Channel Matching			MAX15_A		±1/2		LSB
			MAX15_B		±1		
DYNAMIC PERFORMANCE (V_{IN} = 50kHz, 2.5Vp-p sine wave sampled at 220ksamples/sec)							
Signal-to-Noise and Distortion Ratio	SINAD		MAX15_A		48		dB
			MAX15_B		47		
Total Harmonic Distortion	THD				-60		dB
Spurious-Free Dynamic Range	SFDR				-62		
Small-Signal Bandwidth					4		MHz
Aperture Delay					20		ns
Aperture Delay Matching (Note 2)						4	ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, REFIN = +2.5V, External Reference, AGND = DGND = 0V, V_{SS} = 0V or -5V, f_{CLK} = 5MHz External, Unipolar Range, Single-Ended Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT							
Voltage Range Unipolar, Single-Ended		AIN_(+) to AGND		0		VREF	V
Unipolar, Differential		AIN_(+) to AIN_(-)		0		VREF	
Bipolar, Single-Ended		AIN_(+) to AGND		-VREF		VREF	
Bipolar, Differential		AIN_(+) to AIN_(-)		-VREF		VREF	
Common-Mode Range		Differential mode		V_{SS}		V_{DD}	
DC Input Impedance		AIN = V_{DD}		10			MΩ
REFERENCE INPUT							
REFIN Range (for specified performance) (Note 2)				2.375	2.500	2.625	V
I_{REF}		REFIN = 2.5V				1	mA
REFERENCE OUTPUT (C_L = 4.7µF)							
Output Voltage		I_L = 0mA	T_A = +25°C	2.44	2.50	2.56	V
			T_A = T_{MIN} to T_{MAX}	2.38	2.50	2.62	
Load Regulation		T_A = +25°C, I_{OUT} = 0mA to 10mA				-10	mV
Power-Supply Sensitivity		T_A = +25°C, V_{DD} = 5V ±5%			±1	±3	mV
Temperature Drift					±100		ppm/°C
LOGIC INPUTS (Mode = Open Circuit)							
$\overline{CS}$, $\overline{RD}$, $\overline{WR}$, CLK, D0-D7 (when inputs) Input Low Voltage	V_{IL}					0.8	V
Input High Voltage	V_{IH}			2.4			
Input Current	I_{IN}					±10	µA
Input Capacitance (Note 2)	C_{IN}					15	pF
MODE Input Low Voltage	V_{IL}					0.5	V
Input High Voltage	V_{IH}			V_{DD} - 0.5			
Input Mid-Level Voltage	V_{MID}			$V_{DD}/2$ - 0.5		$V_{DD}/2$ + 0.5	
Input Floating Voltage	V_{FLT}				VDD/2		
Input Current	I_{IN}				±50	±100	µA
LOGIC OUTPUTS							
$\overline{BUSY}$, D0-D7 Output Low Voltage	V_{OL}	I_{OUT} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	IOUT = -360µA		4			
D0-D7 Floating State Leakage						±10	µA
Floating State Output Capacitance (Note 2)	C_{OUT}					15	pF
Conversion Time		f_{CLK} = 5MHz, single channel		3.6		3.8	µs

7

8-/4-Channel ADCs with Simultaneous T/Hs and Reference

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, REFIN = +2.5V, External Reference, AGND = DGND = 0V, V_{SS} = 0V or -5V, f_{CLK} = 5MHz External, Unipolar Range, Single-Ended Mode, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Positive Power-Supply Voltage	V_{DD}			4.75		5.25	V
Positive Power-Supply Current	I_{DD}	PD = 0	MAX155		18	24	mA
			MAX156		9	12	
		PD = 1	CLK, $\overline{CS}$, $\overline{WR}$, RD = 0V or V_{DD}; D_{OUT} = 0V or V_{DD}		25	100	µA
Negative Power-Supply Voltage	V_{SS}			0		-5	V
Negative Power-Supply Current	I_{SS}	PD = 0			2	50	µA
		PD = 1			2	50	
Power-Supply Rejection (change in full-scale error)		V_{DD} = 5V ±5%, V_{SS} = 0V			±0.1	±0.25	LSB
		V_{DD} = 5V, V_{SS} = -5V ±5%			±0.1		

TIMING CHARACTERISTICS (Note 3, Figures 1-7)

(V_{DD} = +5V, REFIN = +2.5V, External Reference, AGND = DGND = 0V, V_{SS} = 0V or -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CWS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CWH}		0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CRS}		0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time (Note 2)	t_{CRH}		0			ns
$\overline{WR}$ Low Pulse Width	t_{WR}	MAX15_C/E	100		2000	ns
		MAX155M	120		2000	
$\overline{RD}$ Low Pulse Width	t_{RDL}	MAX15_C/E	100			ns
		MAX155M	120			
$\overline{RD}$ High Pulse Width (Note 2)	t_{RDH}	MAX15_C/E	180			ns
		MAX155M	200			
$\overline{WR}$ to $\overline{RD}$ Delay (Note 2)	t_{WRD}	MAX15_C/E	280			ns
		MAX155M	300			
$\overline{WR}$ to $\overline{BUSY}$ Low Delay	t_{WBD}	MAX15_C/E			220	ns
		MAX155M			240	
$\overline{BUSY}$ High to $\overline{WR}$ Delay (to update configuration register) (Notes 2, 3)	t_{BWD}		50			ns
CLK to $\overline{WR}$ Delay (acquisition time) (Note 2)	t_{ACQ}		800			ns
$\overline{BUSY}$ High to $\overline{RD}$ Delay (Notes 2, 3)	t_{BRD}		50			ns
Address-Setup Time	t_{AS}		120			ns
Address-Hold Time	t_{AH}		0			ns

TIMING CHARACTERISTICS (continued) (Note 3, Figures 1-7)

(V_{DD} = +5V, REFIN = +2.5V, External Reference, AGND = DGND = 0V, V_{SS} = 0V or -5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RD}$ to Data Valid (Note 4)	t_{DV}	MAX15_C/E	100			ns
		MAX155M	120			
$\overline{RD}$ to Data Three-State Output (Note 5)	t_{TR}	MAX15_C/E	80			ns
		MAX155M	100			
CLK to $\overline{BUSY}$ Delay (Note 2)	t_{CB}			100	300	ns
CLK Frequency			0.5		5.0	MHz

Note 1: V_{DD} = +5V, REFIN = +2.5V, V_{SS} = 0V. Performance at ±5% power-supply tolerance is guaranteed by Power-Supply Rejection test.
Note 2: Guaranteed by design, not production tested.
Note 3: All input control signals are specified with t_r = t_f = 20ns (10% to 90% of +5V) and timed from a +1.6V voltage level. Output signals are timed from V_{OH} and V_{OL}.
Note 4: t_{DV} is the time required for an output to cross +0.8V or +2.4V measured with load circuit of Figure 1.
Note 5: t_{TR} is the time required for the data lines to change 0.5V, measured with load circuits of Figure 2.

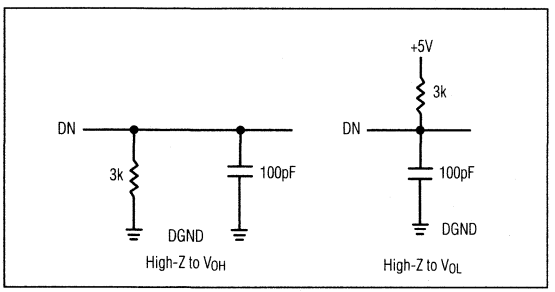


Figure 1. Load Circuits for Data-Access Timing

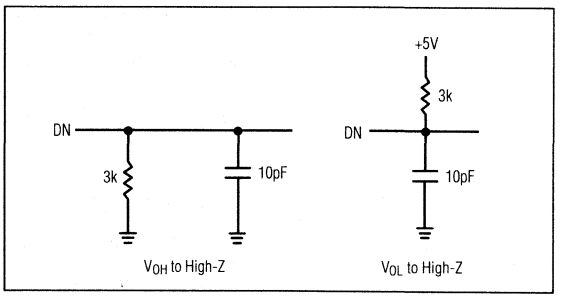


Figure 2. Load Circuits for Three-State Output Timing

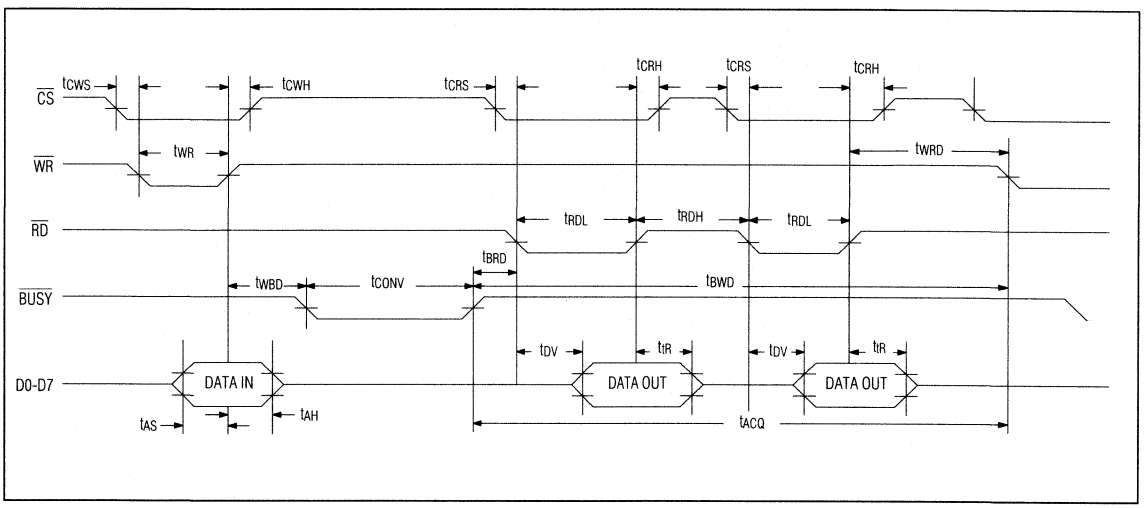


Figure 3. Write and Read Timing

8-/4-Channel ADCs with Simultaneous T/Hs and Reference

Pin Description

MAX155	MAX156		NAME	FUNCTION
DIP/SO	DIP	SO		
1	23	26	AIN3	Sampling Analog Input, channel 3
2	24	28	AIN2	Sampling Analog Input, channel 2
3	1	2	AIN1	Sampling Analog Input, channel 1
4	2	4	AIN0	Sampling Analog Input, channel 0
5	3	5	MODE	Mode configures multiplexer and converter. See Table 4.
6	4	6	V_{SS}	Negative Supply. Power V_{SS} with -5V for extended input range.
7	5	7	$\overline{CS}$	$\overline{CHIP\ SELECT}$ Input must be low for the ADC to recognize $\overline{RD}$, or $\overline{WR}$.
8	6	8	$\overline{RD}$	$\overline{READ}$ Input reads data sequentially from RAM.
9	7	9	$\overline{WR}$	$\overline{WRITE}$ Input's rising edge initiates conversion and updates channel configuration register. Falling edge samples inputs.
10	8	10	$\overline{BUSY}$	$\overline{BUSY}$ Output low when conversion is in progress.
11	9	11	CLK	External Clock Input
12	10	12	D7/$\overline{ALL}$	Three-State Data Output Bit 7 (MSB) / Sequential or Specific Conversion
13	11	13	D6/DIFF	Three-State Data Output Bit 6 / Single-Ended/Differential Select
14	12	14	DGND	Digital Ground
15	13	15	D5/BIP	Three-State Data Output Bit 5 / Unipolar/Bipolar Conversion
16	14	16	D4/INH	Three-State Data Output Bit 4 / Inhibit Conversion Input
17	15	17	D3/PD	Three-State Data Output Bit 3 / Power-Down Input
18	16	18	D2/A2	Three-State Data Output Bit 2 / RAM Address Bit A2 (MAX155 only)
19	17	19	D1/A1	Three-State Data Output Bit 1 / RAM Address Bit A1
20	18	20	D0/A0	Three-State Data Output Bit 0 / RAM Address Bit A0
21	19	21	REFOUT	Reference Output, +2.5V
22	20	22	REFIN	Reference Input, +2.5V normally
23	21	23	AGND	Analog Ground
24	22	24	V_{DD}	Power-Supply Voltage, +5V normally
25-28	—	—	AIN7-4	Sampling Analog Input, channels 7-4
—	—	1, 3, 25, 27	N.C.	No Internal Connection - floating pin.

Detailed Description

A/D Converter Operation

The MAX155/MAX156 contain a 3.6µs successive approximation ADC and 8/4 track-and-hold (T/H) inputs. When a conversion is started, all AIN inputs are simultaneously sampled. All channels sample whether or not they are selected for the conversion. Either a single-channel or multi-channel conversion may be requested and channel configurations may be mixed. ADC results are then stored in an internal RAM.

In hard-wired mode (see *Multiplexer and A/D Configurations* section) multi-channel conversions are initiated with one write operation. In input/output (I/O) mode, multi-channel configurations are set up prior to the conversion by loading channel selections into the configuration register. This register also selects single-ended/differential, unipolar/bipolar (Figure 9), power-down and other functions. Each channel selection requires a separate write operation (i.e. 8 writes for 8 channels), but only after power-up. Once the desired channel arrangement is loaded, each subsequent write converts all selected channels without reconfiguring the multiplexer (mux). I/O mode requires more write operations, but provides more flexibility than hard-wired mode.

To access conversion results, successive $\overline{RD}$ pulses automatically sequence through RAM, beginning with channel 0. Each $\overline{RD}$ pulse increments the RAM address counter, which resets to 0 when $\overline{WR}$ goes low in multi-channel conversions. An arbitrary RAM location may also be read by writing a 1 to INH while loading the RAM address (A0-A2), and then performing a read operation.

Table 1. Multiplexer Configurations

PIN*	INPUT	FUNCTION
D0/A0 D1/A1 D2/A2	1 or 0	A0-A2 select a multiplexer channel for the configurations described below, or select a RAM address for reading with a subsequent $\overline{RD}$.
D3/PD	0	Normal ADC operation
	1	Power-Down reduces the power-supply current. Configuration data may be loaded and is maintained during power-down.
D4/INH	0	A conversion starts when $\overline{WR}$ goes high.
	1	Inhibits the conversion when WR goes high. Allows mux configuration to be loaded and RAM locations to be accessed without starting a conversion.
D5/BIP**	0	Unipolar conversion (Figure 9a) for the channel specified by A0-A2. Input range = 0V to VREF.
	1	Bipolar conversion (Figure 9b) for the channel specified by A0-A2. Input range = ±VREF.
D6/DIFF**	0	Single-ended configuration for the channel specified by A0-A2 as described in Table 2.
	1	Differential configuration for the channel specified by A0-A2 as described in Table 2.
D7/$\overline{ALL}$	0	All previously configured channels are converted. Data is read with consecutive $\overline{RD}$ pulses, beginning with the lowest configured channel.
	1	Only the channel specified by A2-A0 is converted. A single $\overline{RD}$ pulse reads the result of that conversion.

* Configuration inputs are shared with data outputs D0-D7. The functions of D0-D7 are not described in this table.
** DIFF and BIP are not implemented on the current conversion, but go into effect on the following conversion.

8-/4-Channel ADCs with Simultaneous T/Hs and Reference

Multiplexer and A/D Configuration

A conversion is started with a $\overline{WR}$ pulse. All channels sample on $\overline{WR}$'s falling edge. Mux configuration data is loaded on $\overline{WR}$'s rising edge. In I/O mode (MODE = Open Circuit), selections for channel number, single- or multi-channel conversion, unipolar or bipolar input, and single-ended or differential input are made with A0-A2, $\overline{ALL}$, BIP, and DIFF (Table 1). These input pins are also shared with the RAM data outputs D0-D7. An alternate, simpler interface is provided by the hard-wired mode, which selects some general mux configurations without requiring ADC programming. Hard-wired connections of MODE and V_{SS} select from 4 mux configurations as listed in Table 4 (see *Hard-Wired Mode* section).

On the rising edge of $\overline{WR}$, the mux configuration register is updated; falling edge initiates sampling of all inputs. A channel selection can be implemented on the current conversion, but changes from unipolar to bipolar (with BIP) or from single-ended to differential operation (with DIFF) do not go into effect until the following $\overline{WR}$. This can be overcome by writing to the configuration register while inhibiting the conversion (INH = 1), or by changing DIFF and BIP one conversion early, i.e. on the previous write.

Table 2. Single-Ended Channel Selection (MODE = Open Circuit)

MUX ADDRESS				SINGLE-ENDED CHANNEL SELECTION								
A0	A1	A2	DIFF	0	1	2	3	4	5	6	7	AGND
0	0	0	0	+								−
1	0	0	0		+							−
0	1	0	0			+						−
1	1	0	0				+					−
0	0	1	0					+				−
1	0	1	0						+			−
0	1	1	0							+		−
1	1	1	0								+	−

Note: Shaded areas represent MAX156 operation

Table 3. Differential Channel Selection (MODE = Open Circuit)

MUX ADDRESS				DIFFERENTIAL CHANNEL SELECTION							
A0	A1	A2	DIFF	0	1	2	3	4	5	6	7
0	0	0	1	+	−						
0	1	0	1			+	−				
0	0	1	1					+	−		
0	1	1	1							+	−
1	0	0	1	−	+						
1	1	0	1			−	+				
1	0	1	1					−	+		
1	1	1	1							−	+

Note: Shaded areas represent MAX156 operation.

Interface Timing

Input/Output Mode, Multi-Channel Conversion Timing

I/O mode is selected when the MODE input is open circuit. In I/O mode, the mux configuration register determines the conversion type. The register is updated on the rising edge of $\overline{WR}$.

Table 1 lists all conversion options. For example, at D6/DIFF, a logic 0 or 1 selects a single-ended or differential conversion. Data is loaded into addressed locations in the configuration register with a series of $\overline{WR}$ pulses. If INH is high while writing, no conversion takes place. A conversion is started by writing INH = 0 to the configuration register. When a change is made to the contents of the configuration register, a "dummy" conversion may be necessary. This is due to a built-in latency of one full conversion for unipolar/bipolar and single-ended/differential selections.

It is not necessary to update the configuration register before every conversion. A particular mux configuration must be loaded only once after power-up (but the configuration may require several writes to be loaded). A mux configuration is retained for successive conversions and during power-down (PD = 1) so that reconfiguring is unnecessary when the ADC returns to normal operation (PD = 0). Configuration and RAM data is lost only when power is removed from the ADC at V_{DD}.

When updating the configuration register, INH should be high for all except the last $\overline{WR}$ so the conversion is not started until the mux is set. On $\overline{WR}$'s falling edge, all input channels sample simultaneously. $\overline{BUSY}$ goes low at the beginning of the conversion, and channels are converted sequentially starting with the lowest selected channel. When $\overline{BUSY}$ goes high, conversion results are stored in RAM. At conversion end, a microprocessor (µP) can access the RAM contents with consecutive $\overline{RD}$ pulses. The first accessed data is the lowest channel's result. Subsequent $\overline{RD}$ pulses access conversion results for the remaining channels.

The configuration data determines which RAM locations are sequentially read by consecutive $\overline{RD}$ pulses, so new data should be placed in the configuration register only after a full $\overline{RD}$ operation. It is not necessary to update the configuration register for every conversion. A new conversion is initiated with a $\overline{WR}$ pulse (when INH = 0), regardless of the number of channels that have been read.

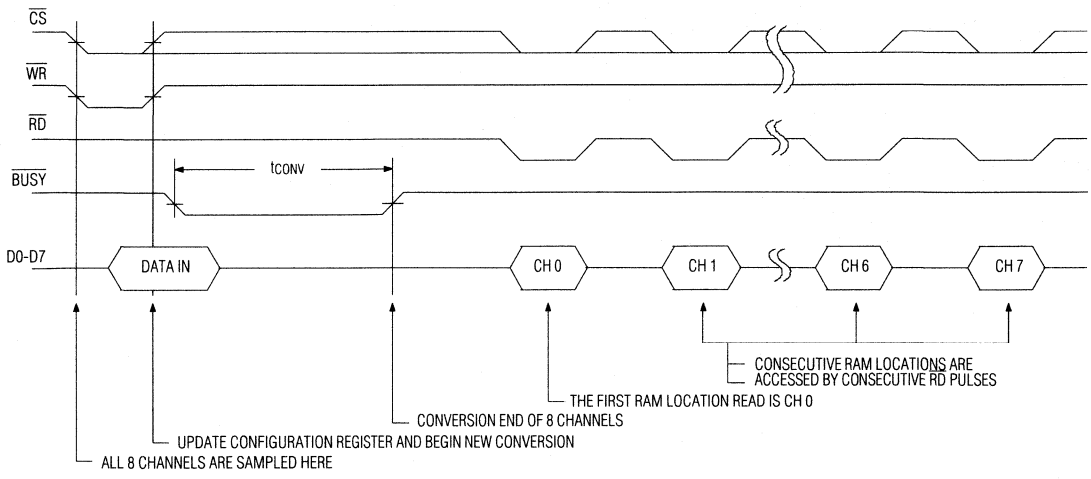
Figure 4a shows the MAX155 timing for an 8-channel unipolar configuration. 8 channels are configured and 8 consecutive $\overline{RD}$ pulses access data. Figure 4b illustrates 4-channel differential conversion timing involving 4 sampled channels and 4 $\overline{RD}$ pulses. In cases where conflicting differential configurations are loaded, the last channel selected with DIFF = 1 will be the positive input of the differential channel.

Input/Output Mode, Single-Channel Conversion Timing

Figure 5a shows timing for a single-channel ($\overline{ALL}$ = 1), single-ended conversion; Figure 5b shows a differential conversion. With MODE floating, the configuration register is updated on the rising edge of $\overline{WR}$. $\overline{BUSY}$ goes low at the beginning of the conversion and returns high when the channel designated by the configuration register has been converted. All channels are sampled on the falling edge of $\overline{WR}$ even if only a single channel has been requested. At conversion end, the µP can read the result for the selected channel with a single $\overline{RD}$ pulse. Subsequent $\overline{RD}$ pulses will access old conversion results remaining in other RAM locations. The next conversion is initiated with a $\overline{WR}$ pulse, regardless of the number of channels that have been read.

INH and A0-A2, in the configuration register, access locations in RAM. INH = 1 allows the RAM address pointer to be updated without starting a conversion. A $\overline{READ}$ pulse then reads the contents of the addressed location.

8-/4-Channel ADCs with Simultaneous T/Hs and Reference



NOTE: After power-up, and prior to the above timing sequence, all single-ended channels must be set up by writing the following data into the configuration register. 8 WRs (see Figure 3) are needed for 8 channels:

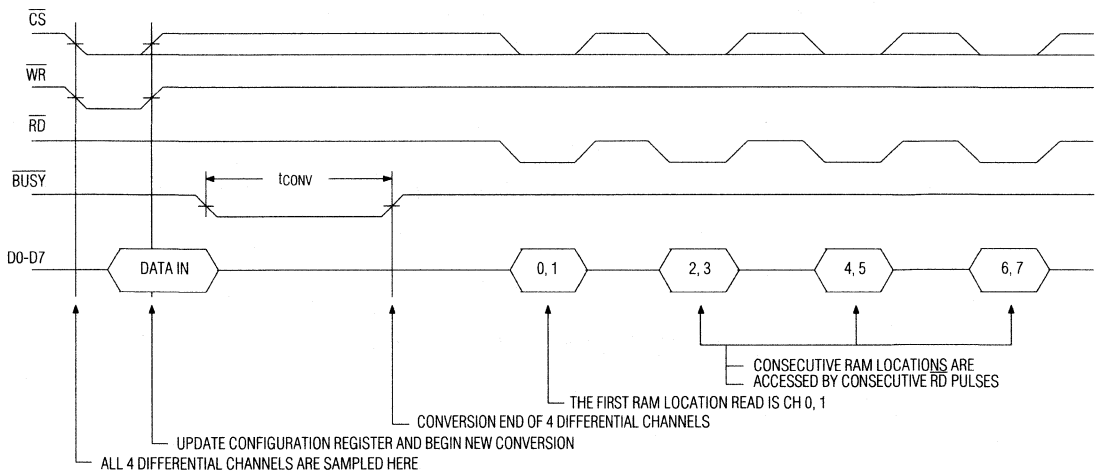
A0	A1	A2	PD	INH	BIP	DIFF	$\overline{ALL}$
0	0	0	0	1	S	0	0
1	0	0	0	1	S	0	0
0	1	0	0	1	S	0	0
1	1	0	0	1	S	0	0
0	0	1	0	1	S	0	0
1	0	1	0	1	S	0	0
0	1	1	0	1	S	0	0
1	1	1	0	1	S	0	0

S = May be selected

Once the above data is loaded, all channels are converted with a single $\overline{WR}$ to any address (this is where the above timing diagram begins). With INH = 0, and $\overline{ALL}$ = 0:

A0	A1	A2	PD	INH	BIP	DIFF	$\overline{ALL}$
0	0	0	0	0	S	0	0

Figure 4a. Input/Output Mode Timing - Eight Single-Ended Conversions



NOTE: After power-up, and prior to the above timing sequence, all differential channels must be set up by writing to the configuration register (AIN0, 2, 4, 6 are +, and AIN1, 3, 5, 7 are - for this example). 4 WRs (see Figure 3) are needed for 4 channels:

A0	A1	A2	PD	INH	BIP	DIFF	$\overline{ALL}$
0	0	0	0	1	S	1	0
0	1	0	0	1	S	1	0
0	0	1	0	1	S	1	0
0	1	1	0	1	S	1	0

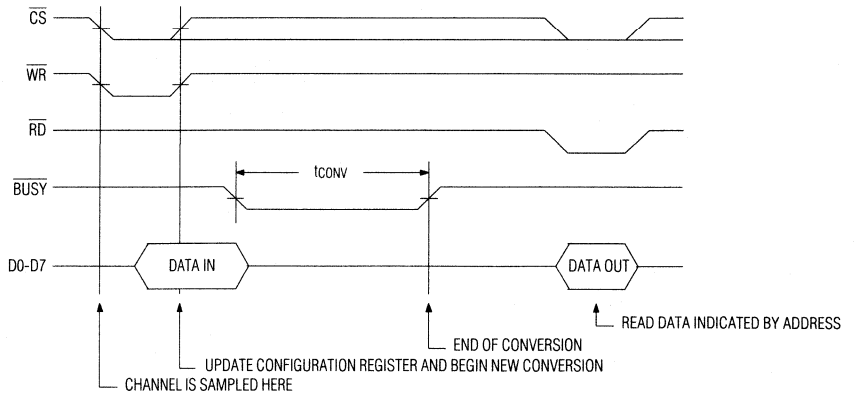
S = May be selected

Once the above data is loaded, all channels are converted with a single $\overline{WR}$ to any address (this is where the above timing diagram begins). With INH = 0, and $\overline{ALL}$ = 0:

A0	A1	A2	PD	INH	BIP	DIFF	$\overline{ALL}$
0	0	0	0	0	S	1	0

Figure 4b. Input/Output Mode Timing - Four Differential Conversions

8-/4-Channel ADCs with Simultaneous T/Hs and Reference

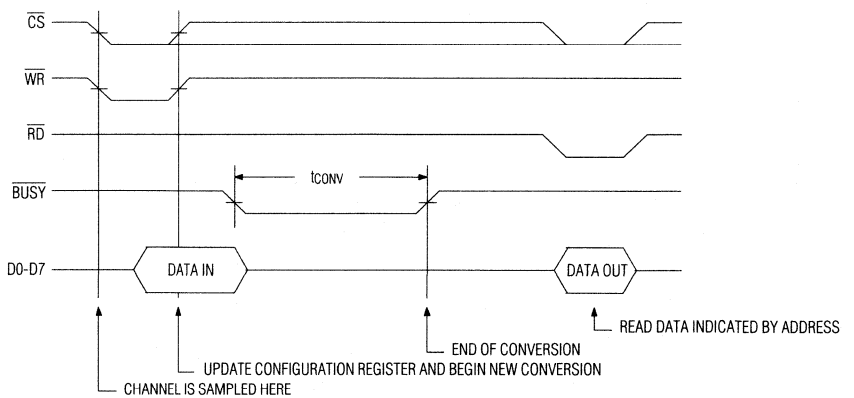


NOTE: A single-ended channel is converted by writing the following data into the configuration register (see Figure 3). The BIP and DIFF bits are not implemented until the next $\overline{WR}$.

A0	A1	A2	PD	INH	BIP	DIFF	$\overline{ALL}$
S	S	S	0	0	S	0	1

S = May be selected

Figure 5a. Input/Output Mode Timing - Single-Channel, Single-Ended Conversion

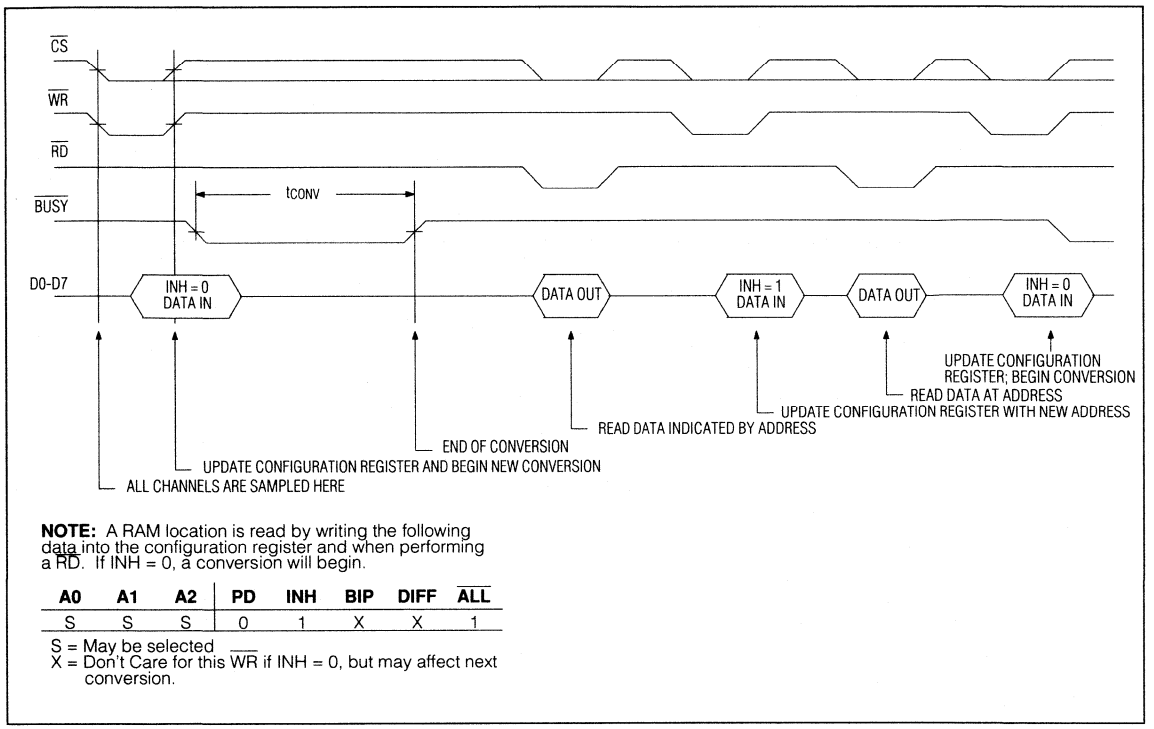


NOTE: A differential channel is converted by writing the following data into the configuration register (see Figure 3). The BIP and DIFF bits are not implemented until the next $\overline{WR}$.

A0	A1	A2	PD	INH	BIP	DIFF	$\overline{ALL}$
S	S	S	0	0	S	1	1

S = May be selected

Figure 5b. Input/Output Mode Timing - Single-Channel, Differential Conversion



NOTE: A RAM location is read by writing the following data into the configuration register and when performing a RD. If INH = 0, a conversion will begin.

A0	A1	A2	PD	INH	BIP	DIFF	ALL
S	S	S	0	1	X	X	1

S = May be selected
X = Don't Care for this WR if INH = 0, but may affect next conversion.

Figure 6. Input/Output Mode Timing - Reading Arbitrary RAM Locations

Hard-Wired Mode

For simpler applications, the MODE and VSS pins can be hard-wired to specify the type of conversion as outlined in Table 4. In this mode, the configuration register is not used, so input data on D0-D7 is ignored. For example, with MODE tied low, an 8-channel, single-ended conversion begins with WR. With MODE tied high, a 4-channel, differential conversion is initiated with WR. Again, the configuration register is not affected by the data present on D0-D7. These conversions are otherwise identical to those shown in Figure 4.

Analog Considerations

Internal Reference

The internal 2.5V reference (REFOUT) must be bypassed to AGND (Figure 8a) with a 4.7µF electrolytic and a 0.1µF ceramic capacitor to ensure stability.

External Reference

If an external voltage reference is used at REFIN, REFOUT must either be bypassed (Figure 8b) or disabled to prevent its output from oscillating and generating unwanted conversion noise elsewhere in the ADC. If component count is critical when using an external reference, REFOUT may be disabled by connecting it to VDD. In this case, the unused internal reference does not need a bypass cap. A disadvantage of tying REFOUT to VDD is that power-down current will be increased by about 250µA above the specification limits.

Table 4. Hard-Wired Mode - Multiplexer Selections

MODE	VSS	CONVERSION TYPE
OPEN CIRCUIT	X	Multiplexer configuration register determines conversion type. Not hard-wired.
0	AGND	8-Channel, Single-Ended, Unipolar Conversion
1	AGND	4-Channel, Differential, Unipolar Conversion
0	-5V	8-Channel, Single-Ended, Bipolar Conversion
1	-5V	4-Channel, Differential, Bipolar Conversion

8-/4-Channel ADCs with Simultaneous T/Hs and Reference

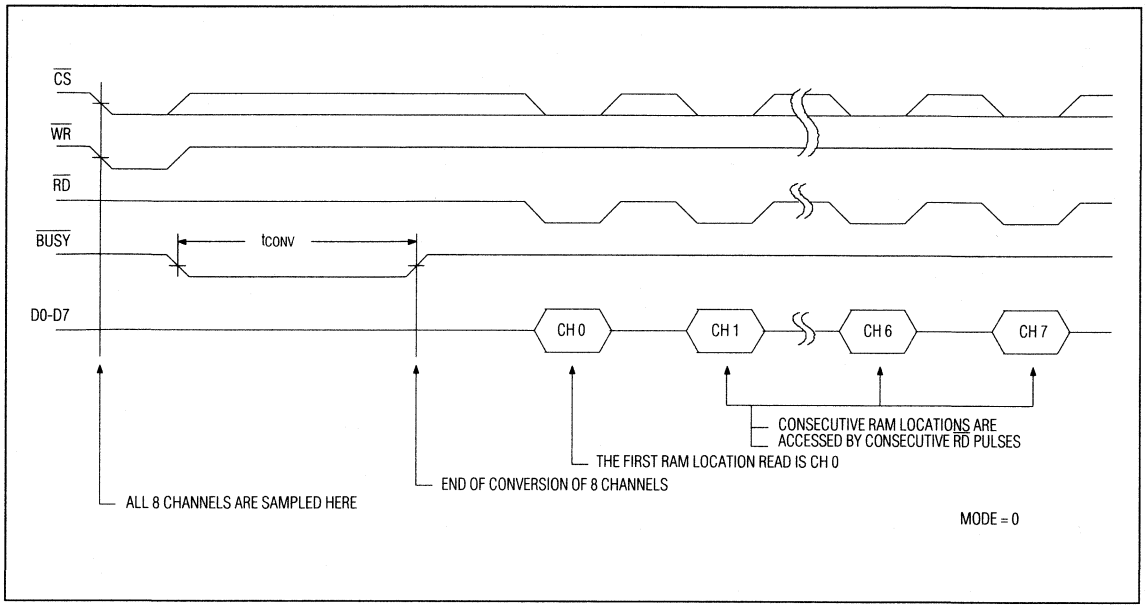


Figure 7a. Hard-Wired Mode Timing - Eight Single-Ended Conversions

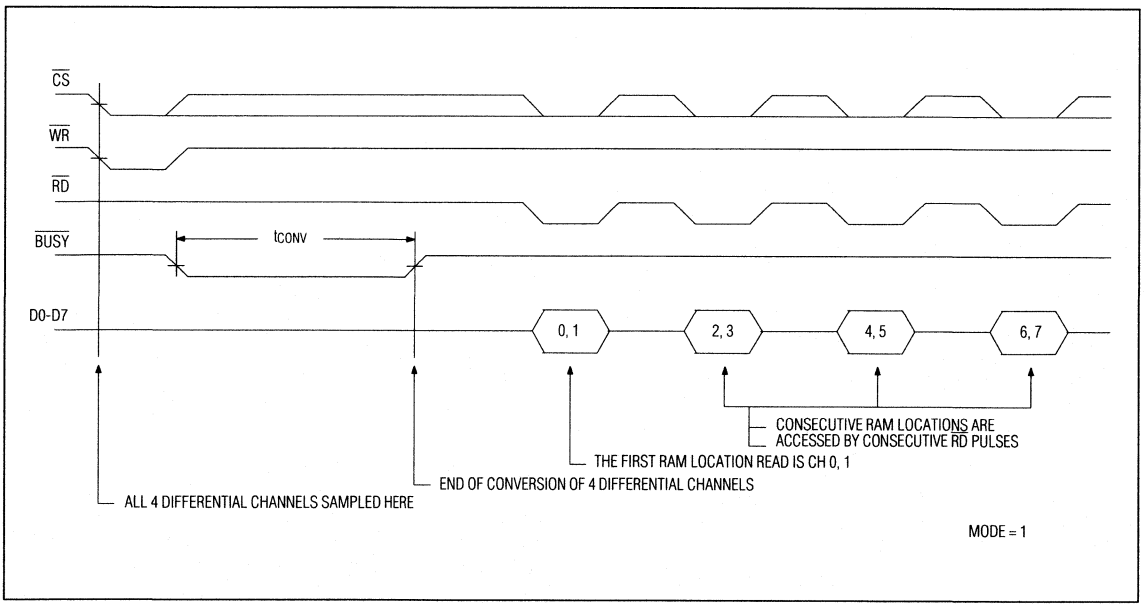


Figure 7b. Hard-Wired Mode Timing - Four Differential Conversions

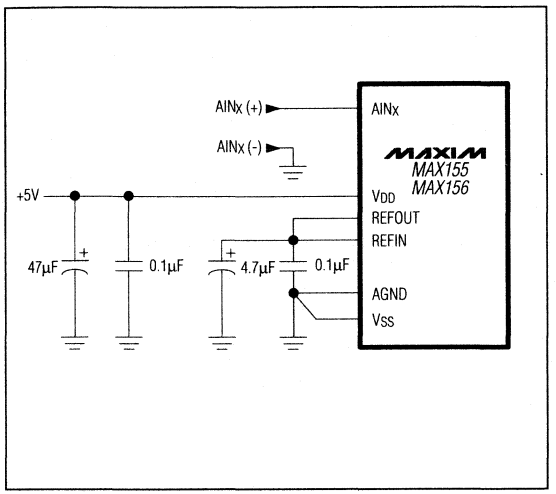


Figure 8a. Internal Reference

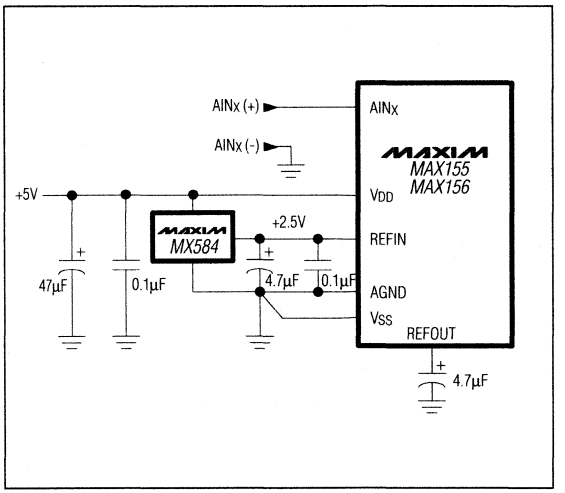


Figure 8b. External Reference, +2.5V Full Scale

Power-Down Mode

The MAX155/MAX156 may be placed in a powered-down state by writing a 1 to the PD location in the configuration register (Table 1). The register may be updated while in this state (to change mux configurations or exit power-down mode) and all register contents are retained; however, no data can be read from RAM and no conversions can be started. The power-down command is implemented on $\overline{WR}$'s rising edge.

To minimize current drain, the MAX155/MAX156 internal reference is turned off during power-down. When returning to normal operation (PD = 0), up to 5ms may be needed to allow the reference to recharge its 4.7µF bypass capacitor before a conversion is performed. If an external reference is used, and remains on during power-down, a conversion can be started within 50µs after loading PD with a 0.

Bypassing

A 47µF electrolytic and a 0.1µF ceramic capacitor should bypass V_{DD} to AGND. If input signals below ground are expected, a negative supply is necessary. In that case, V_{SS} should be bypassed to AGND with a 4.7µF and 0.1µF combination.

The internal reference requires a 4.7µF and 0.1µF combination. If an external voltage reference is used, bypass REFIN to AGND with a 4.7µF capacitor close to the chip. When an external reference is used, REFOUT must still be either bypassed or connected to V_{DD}.

Track/Hold Amplifiers

The MAX155/MAX156 T/H amplifiers' high input impedance usually requires no input buffering. All T/Hs sample simultaneously. For best results, the analog inputs should not exceed the power-supply rails (V_{DD}, V_{SS}) by more than 50mV.

The time required for the T/H to acquire an input signal for one channel is a function of how quickly the channel input capacitance is charged. If the source impedance of the input signal is high, acquisition takes longer, and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 8(R_S + R_{IN}) \times 4pF \text{ (but never less than 800ns)},$$

where R_{IN} = 15kΩ, and R_S = source impedance of the ADC's input signal.

Conversion Time

Conversion time is calculated by:

$$t_{CONV} = (9 \times N \times 2)/f_{CLK},$$

where N is the number of channels converted. This includes one clock cycle of uncertainty. For a single channel and 5MHz clock, the conversion time is (9 x 1 x 2)/5MHz = 3.6µs. For the MAX155, the maximum conversion time for 8 channels is (9 x 8 x 2)/5MHz = 28.8µs. In the application example (Figure 10), six conversions are configured, and the conversion time is (9 x 6 x 2)/5MHz = 21.6µs.

8-/4-Channel ADCs with Simultaneous T/Hs and Reference

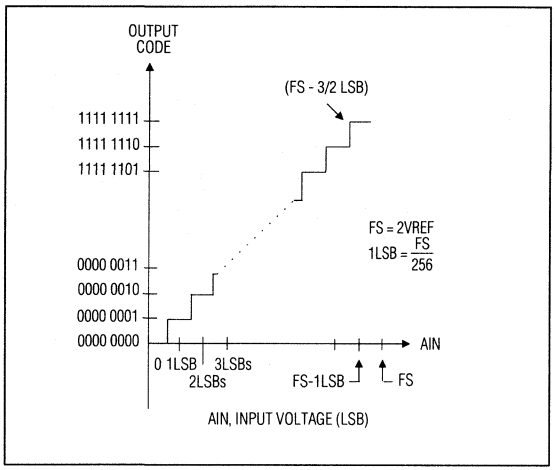


Figure 9a. Transfer Function - Unipolar Operation

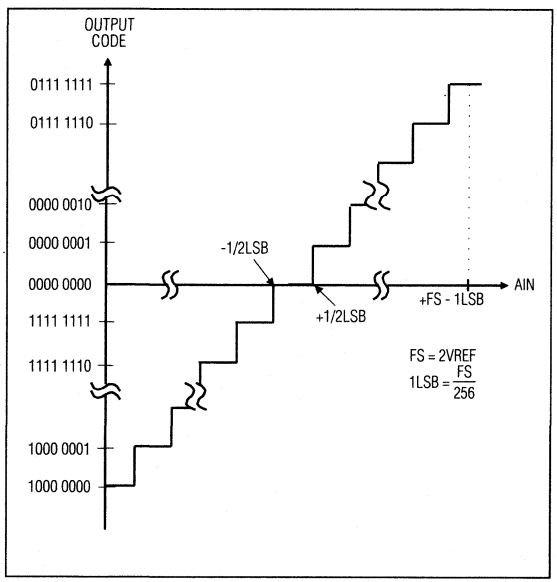


Figure 9b. Transfer Function - Bipolar Operation

Application Information

9-Bit A/D Conversion

In I/O Mode, a 9th bit of resolution can be created by performing two unipolar differential conversions with opposite input polarities (i.e. first with AIN0[+] and AIN1[-], then with AIN0[-] and AIN1[+]). Only the A0 bit must be changed to reverse input channel polarity (Table 3). The sign reversal also occurs on the current write without a one conversion delay. For a differential input signal, one of the two conversions will read 0 while the other will contain an 8-bit result. The input polarity that provides the 8-bit result indicates the 9th (sign) bit. 4 channels can be measured this way. A major drawback of this technique is that many of the sampling features of the MAX155/MAX156 are defeated since two separate samples are needed.

If only two 9-bit channels are needed, then two separate differential channels with reversed input polarities can be connected so that both input pairs sample at the same time. This way the simultaneous sampling advantages of the MAX155/MAX156 are retained.

Typical I/O Mode Application

MAX155/MAX156 address and configuration inputs for this example were determined by selecting the desired channel configurations in Tables 2 and 3. Figure 10 illustrates the configuration outlined in Table 5.

Table 5. Typical Multiplexer Configuration

A2	A1	A0	DIFF	BIP	FUNCTION
0	0	1	1	1	Channel (1, 0), Differential, Bipolar
0	1	0	0	0	Channel 2, Single-Ended, Unipolar
0	1	1	0	1	Channel 3, Single-Ended, Bipolar
1	0	0	0	1	Channel 4, Single-Ended, Bipolar
1	0	1	0	0	Channel 5, Single-Ended, Unipolar
1	1	0	1	0	Channel (6, 7), Differential, Unipolar

An A/D conversion in I/O Mode involves the following three steps:

1. Configure the mux by loading data into the configuration register based on selections from Table 2 and/or 3 (with INH = 1 and MODE = open circuit). For this example, 6 write operations (with each address and data setting in Table 5 above) load the mux after power-up.
2. Sample all selected channels with a $\overline{WR}$ pulse (and INH = 0), and update or rewrite any one location of the configuration register.

This write operation may be skipped by loading INH with a 0 on the last $\overline{WR}$ of the above step. The conversion then starts on the 6th $\overline{WR}$. DIFF and BIP cannot be changed on the 6th $\overline{WR}$ if the conversion is started at that time.

When the conversion starts, $\overline{BUSY}$ goes low while all selected channels are sequentially converted. Conversion results are stored in RAM and are ready to read when $\overline{BUSY}$ returns high.

3. Data is read from RAM with INH = L and consecutive $\overline{RD}$ strobes. Note that in the 6 channel configurations described in this example (Figure 10), 6 $\overline{RD}$ pulses access all available data, starting with the differential channel (1,0). Additional $\overline{RD}$ pulses loop around, accessing the lowest channel data again.
4. To start a new conversion cycle with the same mux configuration, repeat steps 2 and 3.

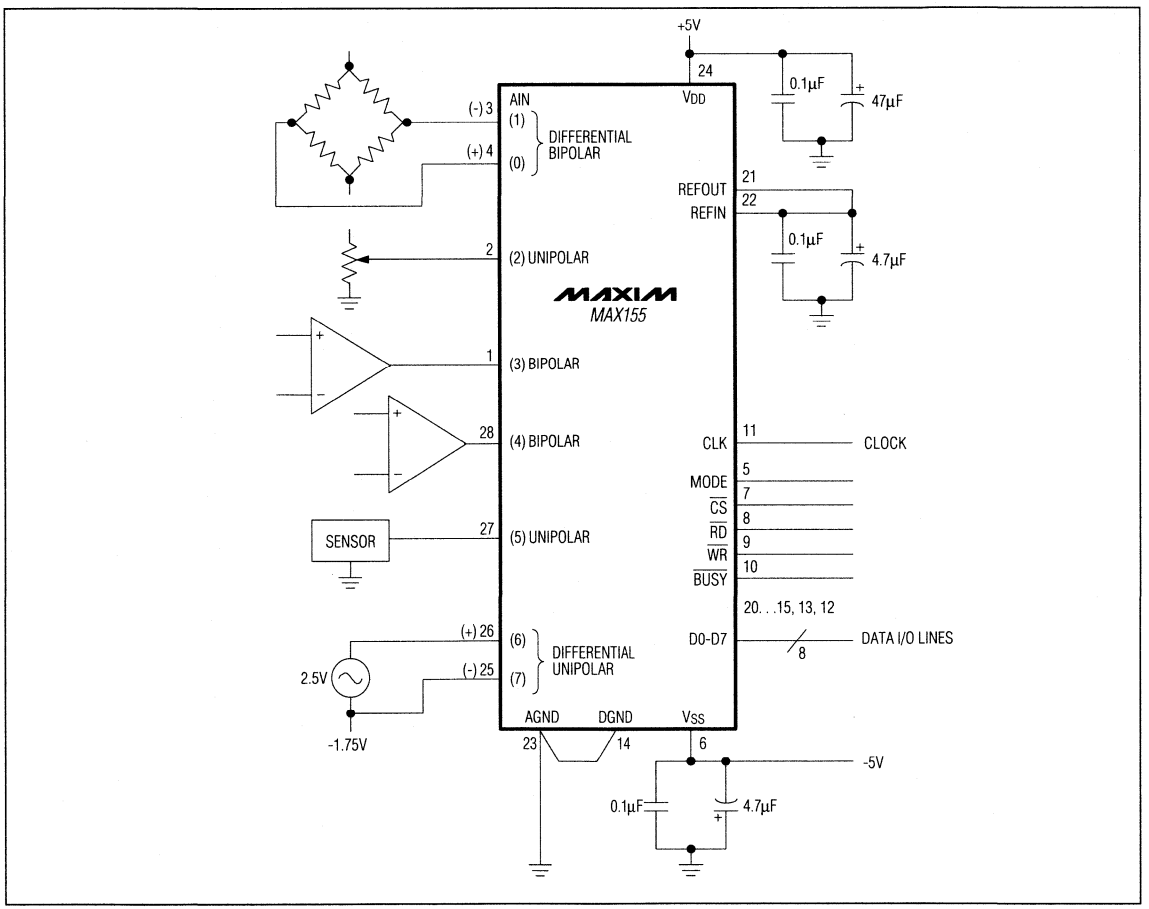


Figure 10. MAX155/MAX156 Typical Operating Circuit

8-/4-Channel ADCs with Simultaneous T/Hs and Reference

_ Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX155AEPI	-40°C to +85°C	28 Plastic DIP	±1/2
MAX155BEPI	-40°C to +85°C	28 Plastic DIP	±1
MAX155AEWI	-40°C to +85°C	28 Wide SO	±1/2
MAX155BEWI	-40°C to +85°C	28 Wide SO	±1
MAX155AMJI	-55°C to +125°C	28 CERDIP**	±1/2
MAX155BMJI	-55°C to +125°C	28 CERDIP**	±1
MAX156ACNG	0°C to +70°C	24 Plastic DIP†	±1/2
MAX156BCNG	0°C to +70°C	24 Plastic DIP†	±1
MAX156ACWI	0°C to +70°C	28 Wide SO	±1/2
MAX156BCWI	0°C to +70°C	28 Wide SO	±1
MAX156BC/D	0°C to +70°C	Dice*	±1
MAX156AENG	-40°C to +85°C	24 Plastic DIP†	±1/2
MAX156BENG	-40°C to +85°C	24 Plastic DIP†	±1
MAX156AEWI	-40°C to +85°C	28 Wide SO	±1/2
MAX156BEWI	-40°C to +85°C	28 Wide SO	±1

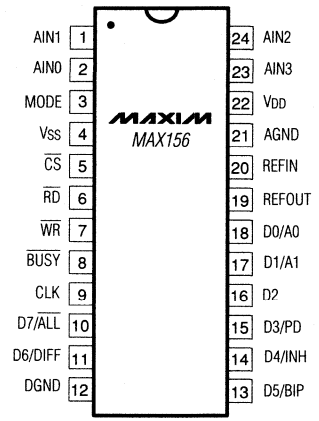
* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

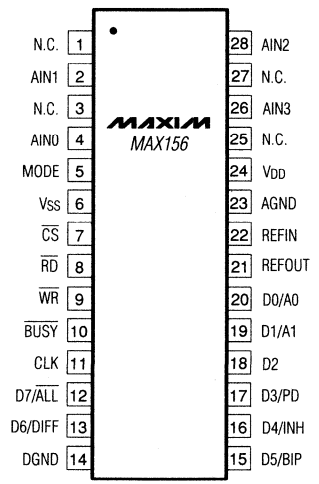
† *Narrow*

____Pin Configurations (continued)

TOP VIEW

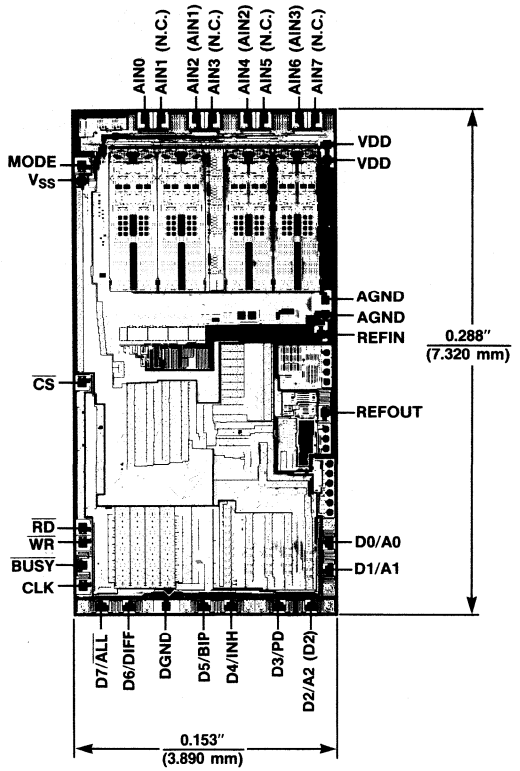


DIP



WIDE SO

Chip Topography



NOTE: LABELS IN ( ) ARE FOR MAX156.

19-1976; Rev 1; 6/92

MAXIM

CMOS µP-Compatible, 5µs, 8-Bit ADCs

General Description

The MAX165/MAX166 are high-speed (5µs) microprocessor (µP)– compatible, 8-bit ADCs with track/hold (T/H). The T/H function allows full-scale signals up to 50kHz (386mV/µs slew rate) to be acquired and digitized accurately. Both ADCs use a successive approximation technique to achieve fast conversions and low power dissipation. The MAX165/MAX166 operate with a +5V supply and an internal or external +1.23V reference, and accept single-ended (MAX165) or differential (MAX166) voltages ranging from 0V to 2VREF.

The MAX165/MAX166 are easily interfaced to all popular 8-bit µPs through standard $\overline{CS}$ and $\overline{RD}$ control signals. These signals control the start of conversions and data access. A $\overline{BUSY}$ signal indicates the beginning and end of conversions. Since all the data outputs are latched and three-state buffered, the MAX165/MAX166 can be directly tied to a µP data bus or system input/output port.

The MAX165 is a plug-in replacement for the MX7575, with the addition of an internal 1.23V reference. For applications that require a differential analog input and an internal reference, the MAX166 is recommended.

Applications

Digital-Signal Processing

High-Speed Data Acquisition

Telecommunications

Audio Systems

High-Speed Servo Loops

Low-Power Data Loggers

Features

- ♦ **5µs Conversion Time**
- ♦ **Built-In Track/Hold**
- ♦ **±1LSB Max Total Unadjusted Error**
- ♦ **50kHz Signal Bandwidth**
- ♦ **Internal 1.23V Bandgap Reference and Buffer**
- ♦ **Single +5V Supply Operation**
- ♦ **8-Bit µP Interface**
- ♦ **100ns Data-Access Time**
- ♦ **15mW Typ Power Consumption**
- ♦ **Small Footprint Packages**
- ♦ **Plug-In Upgrade to the MX7575 (MAX165)**

Ordering Information

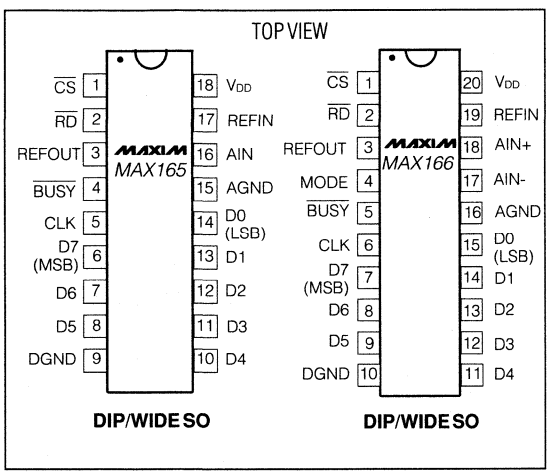
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX165ACPN	0°C to +70°C	18 Plastic DIP	±1/2
MAX165BCPN	0°C to +70°C	18 Plastic DIP	±1
MAX165ACWN	0°C to +70°C	18 Wide SO	±1/2
MAX165BCWN	0°C to +70°C	18 Wide SO	±1
MAX165BC/D	0°C to +70°C	Dice*	±1
MAX165AEPN	-40°C to +85°C	18 Plastic DIP	±1/2
MAX165BEPN	-40°C to +85°C	18 Plastic DIP	±1
MAX165AEWN	-40°C to +85°C	18 Wide SO	±1/2
MAX165BEWN	-40°C to +85°C	18 Wide SO	±1
MAX165AMJN	-55°C to +125°C	18 CERDIP**	±1/2
MAX165BMJN	-55°C to +125°C	18 CERDIP**	±1

Ordering Information continued on last page.

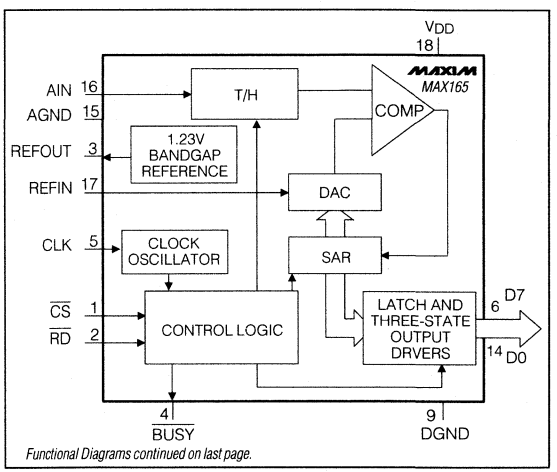
** Contact factory for dice specifications.*

***Contact factory for availability processing to MIL-STD-883.*

Pin Configurations



Functional Diagrams



Functional Diagrams continued on last page.

CMOS µP-Compatible 5µs, 8-Bit ADCs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +7V
V_{DD} to DGND ..... -0.3V, +7V
AGND to DGND ..... -0.3V, V_{DD} +0.3V
Digital Input Voltage to DGND
(MAX165 Pins 1, 2) ..... -0.3V, V_{DD} +0.3V
(MAX166 Pins 1, 2, 4) ..... -0.3V, V_{DD} +0.3V
Digital Output Voltage to DGND
(MAX165 Pins 4, 6-8, 10-14) ..... -0.3V, V_{DD} +0.3V
(MAX166 Pins 5, 7-9, 11-15) ..... -0.3V, V_{DD} +0.3V
CLK Input Voltage (MAX165 Pin 5) to DGND . -0.3V, V_{DD} +0.3V
CLK Input Voltage (MAX166 Pin 6) to DGND . -0.3V, V_{DD} +0.3V
REFIN, REFOUT to AGND ..... -0.3V, V_{DD} +0.3V
MAX165 AIN to AGND ..... -0.3V, V_{DD} +0.3V
MAX166 AIN+, AIN- to AGND ..... -0.3V, V_{DD} +0.3V

Continuous Power Disipation (T_A = +70°C)
18-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
18-Pin Wide SO (derate 9.52mW/°C above +70°C) ... 762mW
18-Pin CERDIP (derate 10.53mW/°C above +70°C) ... 842mW
20-Pin Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
20-Pin Wide SO (derate 10.00mW/°C above+70°C) ... 800mW
20-Pin CERDIP (derate 11.11mW/°C above +70°C) ... 889mW
Operating Temperature Ranges:
MAX16_ _C_ _ ..... 0°C to +70°C
MAX16_ _E_ _ ..... -40°C to +85°C
MAX16_ _M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, REFIN = +1.23V, AGND = DGND = 0V, AIN- = 0V (MAX166), f_{CLK} = 4MHz external, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				8			Bits
Total Unadjusted Error	TUE		MAX165A			±1	LSB
			MAX165B			±2	
			MAX166A/C			±1	
			MAX166B/D			±2	
Relative Accuracy			MAX165A			±1/2	LSB
			MAX165B			±1	
			MAX166A/C			±1/2	
			MAX166B/D			±1	
No-Missing-Codes Resolution				8			Bits
Full-Scale Error						±1	LSB
Full-Scale Tempco					±5		ppm/°C
Offset Error (Note 1)						±1/2	LSB
Offset Tempco					±5		ppm/°C
ANALOG INPUT							
Voltage Range		1LSB = 2VREF/256		0		2VREF	V
Voltage Range AIN+ (MAX166)				AIN-		V_{DD}	V
Voltage Range AIN- (MAX166)				0		AIN+	V
DC Input Impedance				10			MΩ
Slew Rate, Tracking				0.386			V/µs
SNR (Note 2)		V_{IN} = 2.46V_{p-p} at 10kHz (Figure 13)		45			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V, REFIN = +1.23V, AGND = DGND = 0V, AIN- = 0V (MAX166), f_{CLK} = 4MHz external, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE (Note 2)							
REFIN Range (Note 3)	VREF	±5% variation for specified performance		1.16	1.23	1.29	V
REFIN Current	I_{REF}					500	µA
REFOUT Voltage	REFOUT	T_A = +25°C		1.18	1.21	1.23	V
REFOUT Load Regulation		T_A = +25°C, I_L = 0mA to 1.5mA				3	mV
REFOUT Supply Sensitivity		V_{DD} ±5%				±1.5	mV
Temperature Drift			MAX165AC/AE/BC/BE		40	70	ppm/°C
			MAX165AM/BM		60	100	
			MAX166AC/AE/BC/BE		40	70	
			MAX166AM/BM		60	100	
External Capacitive Load Requirement				4.7			µF
LOGIC INPUTS							
$\overline{CS}$, $\overline{RD}$, MODE (MAX166)							
Input Low Voltage	V_{INL}					0.8	V
Input High Voltage	V_{INH}			2.4			V
Input Current	I_{IN}	V_{IN} = 0V or V_{DD}	T_A = +25°C			±1	mA
			T_A = T_{MIN} to T_{MAX}			±10	
Input Capacitance (Note 3)	C_{IN}					10	pF
CLOCK							
Input Low Voltage	V_{INL}					0.8	V
Input High Voltage	V_{INH}			2.4			V
Input Low Current	I_{INL}	V_{IN} = 0V	MAX16_ _C/E			700	µA
			MAX16_ _M			800	
Input High Current	I_{INH}	V_{IN} = V_{DD}	MAX16_ _C/E			700	µA
			MAX16_ _M			800	
LOGIC OUTPUTS							
$\overline{BUSY}$, D0 to D7							
Output Low Voltage	V_{OL}	I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	I_{SOURCE} = 40µA		4.0			V
D0 to D7							
Floating State Leakage Current		V_{OUT} = 0V to V_{DD}	MAX16_ _C/E			±1	mA
			MAX16_ _M			±10	
Floating State Output Capacitance (Note 3)						10	pF
CONVERSION TIME (Note 4)							
With External Clock		f_{CLK} = 4MHz			5		µs
With Internal Clock		Using recommended clock components R_{CLK} = 100kΩ, C_{CLK} = 100pF, T_A = +25°C		5		15	µs
POWER REQUIREMENTS (Note 5)							
Supply Voltage	V_{DD}	±5% for specified performance			5		V
Supply Current	I_{DD}		MAX16_ _C/E		3	6	mA
			MAX16_ _M		3	7	
Power Dissipation					15		mW
Power-Supply Rejection		4.75V < V_{DD} < 5.25V				±1/4	LSB

CMOS µP-Compatible 5µs, 8-Bit ADCs

TIMING CHARACTERISTICS (Note 6)

(V_{DD} = +5V, REFIN = +1.23V, AGND = DGND = 0V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C		T_A = T_{MIN} to T_{MAX}				UNITS
			ALL		MAX16_ _C/E		MAX16_ _M		
			MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0		0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Propagation Time	t_2			100		100		120	ns
Data-Access Time after $\overline{RD}$	t_3	(Note 7)		100		100		120	ns
$\overline{RD}$ Pulse Width	t_4		100		100		120		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0		0		0		ns
Data-Access Time after $\overline{BUSY}$	t_6	(Note 7)		80		80		100	ns
Data-Hold Time after $\overline{RD}$	t_7	(Note 8)	10	80	10	80	10	100	ns
$\overline{BUSY}$ to $\overline{CS}$ Delay	t_8		0		0		0		ns

Note 1: Offset Error is measured with respect to an ideal first code transition which occurs at 1/2LSB.
Note 2: REFOUT is not available for use in MAX166C/MAX166D. These parts must be used with an external reference.
Note 3: Guaranteed by design, not tested.
Note 4: Accuracy may degrade at conversion times other than those specified.
Note 5: Power-supply current is measured when MAX165/MAX166 are inactive, i.e.
for MAX165 $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = high;
for MAX166 CS = $\overline{RD}$ = $\overline{BUSY}$ = MODE = high.
Note 6: Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with t_r = t_f = 20ns (10% to 90% of +5V) and timed from a 1.6V voltage level.
Note 7: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 8: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.

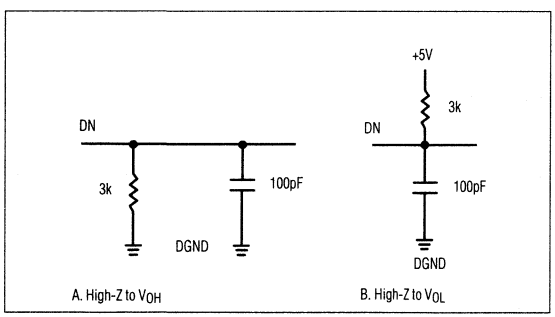


Figure 1. Load Circuits for Data-Access Time Test

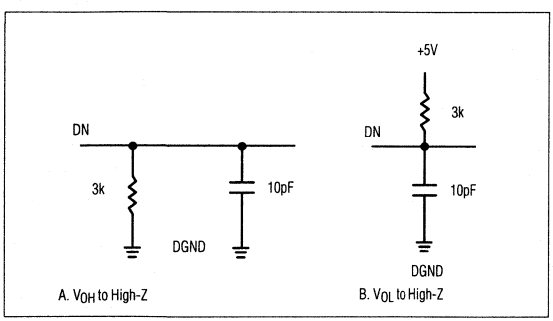


Figure 2. Load Circuits for Data-Hold Time Test

Detailed Description

Converter Operation

The MAX165/MAX166 use the successive approximation technique to convert an unknown analog input voltage to an 8-bit digital output code (see *Functional Diagrams*). The MAX165/MAX166 sample the input voltage on an internal capacitor once at the beginning of the conversion, (see *Track/Hold* section). The DAC is initially set to half scale, and the comparator determines whether the input signal is larger or smaller than half scale. If the input is larger, the DAC most significant bit (MSB) is kept; if it is smaller, the MSB is dropped. At the end of each comparison phase, the successive approximation register (SAR) stores the results of the previous decisions and determines the next trial bit. This information is loaded into the DAC after each decision. As the conversion proceeds, the analog input is approximated more closely as it is compared to the combined previous DAC bits and a new DAC trial bit. After 8 comparison cycles, the 8 bits stored in the SAR are latched into the output latches. At the end of the conversion, the $\overline{BUSY}$ signal goes high, and the data in the output latches is ready for µP access. Furthermore, the DAC is reset to half scale in preparation for the next conversion.

Microprocessor Interface

The $\overline{CS}$ and $\overline{RD}$ logic inputs are used to initiate conversions and to access data from the devices. The MAX165/

Pin Description

PIN		NAME	FUNCTION
MAX165	MAX166		
1	1	$\overline{CS}$	CHIP SELECT Input. $\overline{CS}$ must be low for the device to be selected, or to recognize the $\overline{RD}$ input.
2	2	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data. $\overline{RD}$ is also used to start conversions. See the *Digital Interface* section.
3	3	REFOUT	Output of the internal 1.23V bandgap reference
	4	MODE	MODE (MAX166). Mode = low puts the ADC into asynchronous-conversion mode. MODE has to be tied high for synchronous-conversion mode and ROM interface mode.
4	5	$\overline{BUSY}$	$\overline{BUSY}$ Output. $\overline{BUSY}$ going low indicates the start of a conversion. BUSY going high indicates the end of a conversion.
5	6	CLK	External Clock Input/Internal Oscillator Pin for frequency setting RC components.
6	7	D7 (MSB)	Three-State Data Output, bit 7 (MSB)
7	8	D6	Three-State Data Output, bit 6
8	9	D5	Three-State Data Output, bit 5
9	10	DGND	Digital Ground
10	11	D4	Three-State Data Output, bit 4
11	12	D3	Three-State Data Output, bit 3
12	13	D2	Three-State Data Output, bit 2
13	14	D1	Three-State Data Output, bit 1
14	15	D0 (LSB)	Three-State, Data Output, bit 0 (LSB)
15	16	AGND	Analog Ground
16		AIN	Analog Input – (single-ended with respect to AGND) 0V to 2VREF input range
	17	AIN–	Negative Analog Input – differential (MAX166)
	18	AIN+	Positive Analog Input – differential (MAX166)
17	19	REFIN	Reference Input +1.23V nominal
18	20	V_{DD}	Power-Supply Voltage +5V nominal

MAX166 have two common interface modes that will be referred to as slow-memory interface mode and ROM interface mode. In addition, the MAX166 has an asynchronous conversion mode (MODE pin = low) where continuous conversions are performed. In the slow-memory interface mode, $\overline{CS}$ and $\overline{RD}$ are taken low to start a conversion and remain low until the end of the conversion, at which time data is updated. This mode is designed for µPs that can be forced into a wait state. In ROM interface mode, however, the µP is not forced into a wait state. A conversion is started by taking $\overline{CS}$ and $\overline{RD}$ low, and data from the previous conversion is read. At the end of the most recent conversion, the µP executes a READ instruction and starts another conversion.

Slow-Memory Interface Mode

Figure 3 shows the timing diagram for slow-memory interface mode. This mode is used with µPs that have a wait state capability of at least 5µs (such as the 8085A), where a READ instruction is extended to accommodate slow-memory devices. A conversion is started by executing a memory READ to the device (taking $\overline{CS}$ and $\overline{RD}$ low). The $\overline{BUSY}$ signal (which is connected to the µP READY input) then goes low and forces the µP into a wait state. The T/H, which has been tracking the analog input signal, holds the signal on the third falling clock edge after $\overline{RD}$ goes low (Figure 12). At the end of the conversion, $\overline{BUSY}$ returns high, the output latches, and buffers are updated with the new conversion results. The µP then completes the memory READ by acquiring this new data.

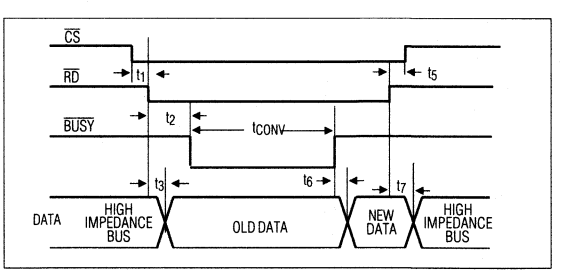


Figure 3. Slow-Memory Interface Mode Timing Diagram

CMOS µP-Compatible 5µs, 8-Bit ADCs

The MAX165/MAX166's fast conversion time ensures that the µP is not forced into a wait state for too long. Faster versions of many µPs, including the 8085A-2, test the status of the READY input right after the start of an instruction cycle. Therefore, for the MAX165/MAX166 to effectively place the µP in a wait state, their $\overline{BUSY}$ output should go low very early in the cycle. When using the 8085A-2, the earliest possible indication of an upcoming READ operation is provided by the S0 status signal. Thus, S0 (which is low for a READ cycle) should be connected to the $\overline{RD}$ input of the MAX165/MAX166. Figure 4 shows the connection diagram for the 8085A-2 to the MAX165/MAX166 in slow-memory interface mode.

ROM Interface Mode

Figure 5 shows the timing diagram for ROM interface mode. In this mode, the µP does not need to be placed in a wait state. A conversion is started with a READ instruction ($\overline{RD}$ and $\overline{CS}$ go low), and old data is accessed. The $\overline{BUSY}$ signal then goes low to indicate the start of a conversion. As before, the T/$\overline{H}$ acquires the signal on the third falling clock edge after $\overline{RD}$ goes low. At the end of conversion ($\overline{BUSY}$ going high), another READ instruction always accesses the new data and normally starts a second conversion. However, if $\overline{RD}$ and $\overline{CS}$ go low within one external clock period of $\overline{BUSY}$ going high, the second conversion is not started. For correct operation in this mode, $\overline{RD}$ and $\overline{CS}$ should not go low before $\overline{BUSY}$ returns high.

Figures 6 and 7 show the connection diagrams for interfacing the MAX165/MAX166 in ROM interface mode. Figure 6 shows the connection diagram to the 6502/6809 µPs, and Figure 7 shows interfacing to the Z-80.

Due to their fast interface timing, the MAX165/MAX166 will interface to the TMS32010 running at up to 18MHz. Figure 8 shows the connection diagram to the TMS32010. In this interface, the MAX165/MAX166 are mapped as a port address. A conversion is initiated by using an IN A and a PA instruction, and the conversion result is placed in the TMS32010 accumulator.

Asynchronous Conversion Mode (MAX166)

Tying the MODE pin low places the MAX166 into a continuous-conversion mode. The $\overline{RD}$ and $\overline{CS}$ inputs are only used for reading data from the converter. Figure 9 shows the timing diagram for this mode of operation, and Figure 10 shows the connection diagram of the converter to the 8085A. In this mode, the MAX166 appears like a ROM to the µP, in that data can be accessed independently of the clock. The output latches are normally

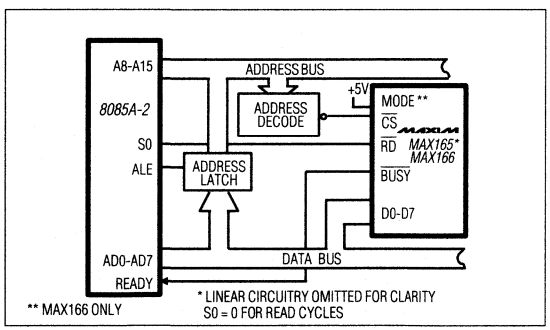


Figure 4. MAX165/MAX166 to 8085A-2 Slow-Memory Interface

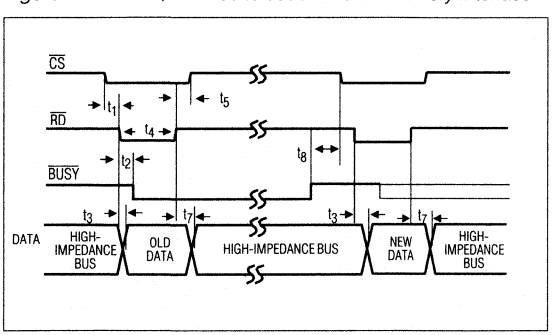


Figure 5. ROM Interface Timing Diagram

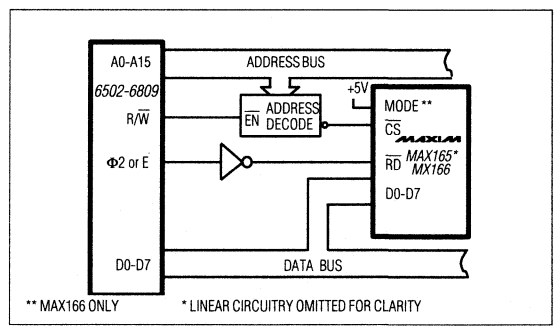


Figure 6. MAX165/MAX166 to 6502/6809 ROM Interface

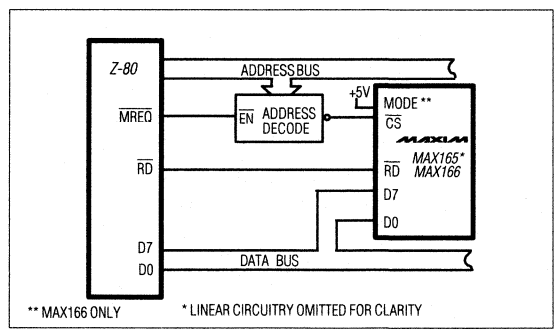


Figure 7. MAX165/MAX166 to Z-80 ROM Interface

updated on the rising edge of BUSY. But, if CS and RD are low when BUSY goes high, the data latches are not updated until one of these inputs returns high. Additionally, the MAX166 stops converting and BUSY stays high until RD or CS goes high. This mode of operation allows a simple µP interface.

Microprocessor Interface For Signal Acquisition

Many applications require sampling of the input signal at equal intervals to minimize errors caused by sampling uncertainty or jitter. To achieve this with the previously discussed interfaces, the user must match software delays or count the number of elapsed clock cycles. This becomes difficult in interrupt driven systems where the uncertainty in interrupt servicing delays is another complicating factor.

The solution is to use a real-time clock to control the start of a conversion. This should be synchronous with the clock input to the ADC (both should be derived from the same source) because the sampling instants occur three clock cycles after CS and RD go low. Therefore, the sampling instants occur at exactly equal intervals if the conversions are started at equal intervals. In this scheme, the output data is fed into a FIFO latch, which allows the µP to access data at its own rate. This guarantees that data is not read from the ADC in the middle of a conversion. If data is read from the ADC during a conversion, the conversion in progress may be disturbed, but the accessed data that belonged to the previous conversion will be correct.

The T/H starts holding the input on the third falling edge of the clock after CS and RD go low. If CS and RD go low within 20ns of a falling clock edge, the ADC may or may not consider this falling edge as the first of the three edges that determine the sampling instant. Therefore, the CS and RD should not be allowed to go low within this period when sampling accuracy is required.

Track/Hold

The T/H consists of a sampling capacitor and a switch to capture the input signal. The simplified diagram of this block is shown in Figure 11. At the beginning of the conversion, switch S1 is closed, and the input signal is tracked. The input signal is held (switch S1 opens) on the third falling edge of clock after CS and RD go low (Figure 12). This allows a minimum of two clock cycles for the input capacitor to be charged to the input voltage through the switch resistance. The time required for the hold capacitor to settle to ±1/4LSB is typically 7ns. Therefore, the input signal is allowed ample time to settle before it is acquired by the T/H. When a conversion ends, switch S1 closes, and the input signal is tracked.

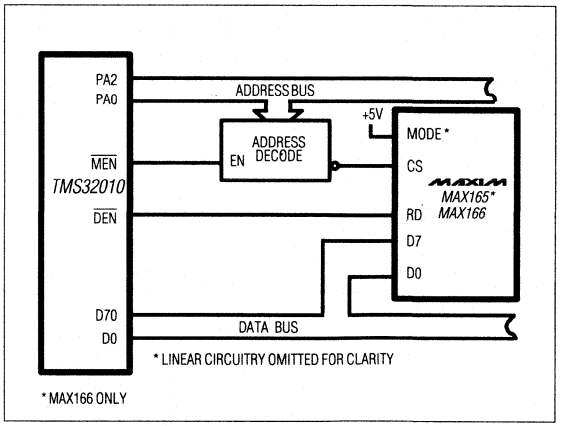


Figure 8. MAX165/MAX166 to TMS32010 ROM Interface

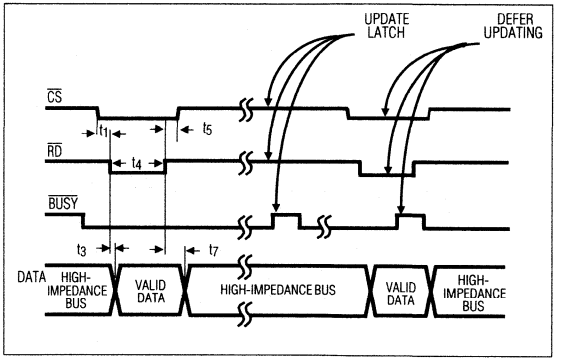


Figure 9. MAX166 Asynchronous-Conversion Mode Timing Diagram

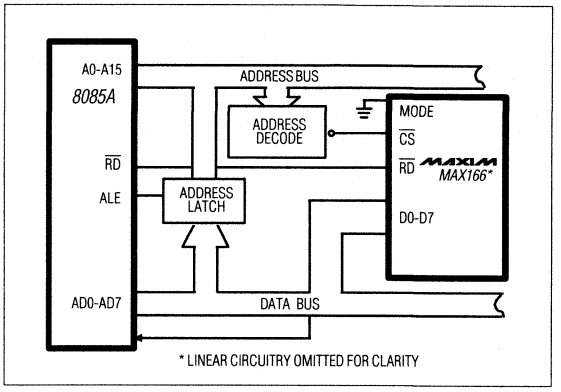


Figure 10. MAX166 to 8085A Asynchronous-Conversion Mode Interface

CMOS µP-Compatible 5µs, 8-Bit ADCs

The T/H can acquire signals with slew rates of up to 386mV/µs (or equivalently a 50kHz sine wave with $2.46V_{p-p}$ amplitude). Figure 13 shows the signal-to-noise ratio (SNR) versus input frequency for the ADC. The SNR plot is generated at a sampling rate of 200kHz using sinusoidal inputs with a $2.46V_{p-p}$ amplitude. The reconstructed sine wave is passed through a 50kHz, 8th-order Chebyshev filter. The improvement in SNR at high frequencies is due to the filter cutoff.

The switching nature of the analog input results in transient currents that charge the T/H's input capacitance. Keep the driving source impedance low (below 2kΩ) so the T/H's settling characteristics are not degraded. A low driving impedance also minimizes undesirable noise pick-up and reduces DC errors caused by transient currents at the analog input. As with any ADC, it is important to keep external noise sources to a minimum during a conversion. Keep the data bus as quiet as possible during a conversion, especially when the T/H is making a transition to hold mode.

Device accuracy may degrade slightly when conversion times are significantly longer than 5µs, as shown in Figure 14. This degradation is due to the charge that is lost from the hold capacacitor in the presence of small on-chip leakage currents.

Differential Input (MAX166)

The MAX166 converts differential inputs [(AIN+) - (AIN–)] in the 0V to 2VREF range. This can be especially useful in single-supply applications where the output swing requirements on the input amplifier are reduced. For example, if AIN- is tied to the reference output of the MAX166, the voltage swing on AIN+ must fall in the 1.23V to 3.69V range. Furthermore, the differential capability allows the converter to reject low-frequency common-mode signals.

The voltage at AIN+ is sampled at the beginning of the conversion and is referenced to AIN- during the conversion. Therefore, it is essential that the voltage on AIN- be relatively constant with respect to AGND during the conversion, otherwise conversion errors will result. If the AIN- input changes by a small voltage during the conversion, the conversion result can show an error in the same amount. For example, if the input has a 60Hz common-mode component of 0.5V with respect to AGND, an error of less than 0.1LSB is incurred during the 5µs conversion. Conversion errors increase with higher frequency or higher amplitude common-mode signals.

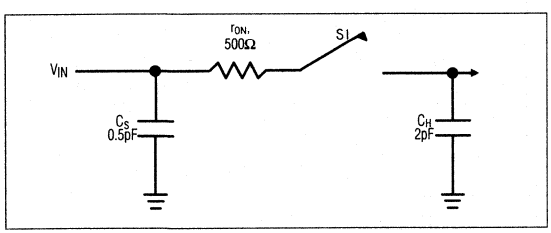


Figure 11. MAX165/MAX166 Equivalent Input Circuit

Reference Input

This ADC's high speed can be partially attributed to its DAC's "inverted-voltage output" topography. This topography provides low offset and gain errors and fast settling times. The input current to the DAC, however, is not constant. During a conversion, as different DAC codes are tried, the DAC's DC impedance can vary between 6kΩ and 18kΩ. Furthermore, when the DAC codes change, small amounts of transient current are drawn from the reference input. These characteristics require a low DC and AC driving impedance for the reference circuitry to minimize conversion errors.

Figure 15 shows the external reference circuitry recommended for driving the reference input of the MAX165/MAX166. The decoupling capacitors are necessary to provide a low AC source impedance.

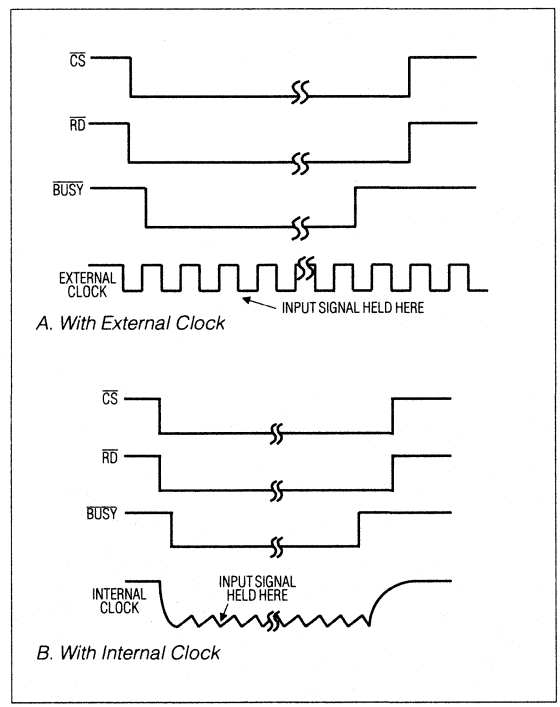


Figure 12. MAX165/MAX166 T/H Timing Diagrams (Slow-Memory Interface Mode)

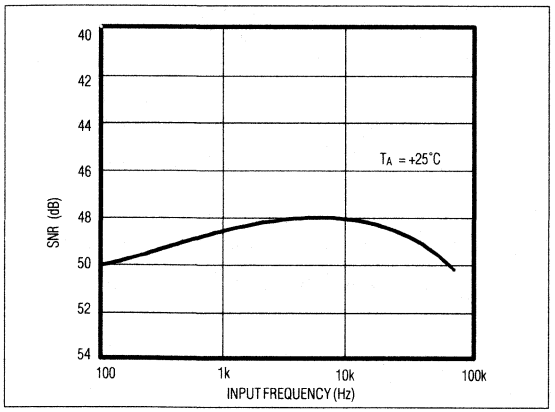


Figure 13. MAX165/MAX166 SNR vs. Input Frequency

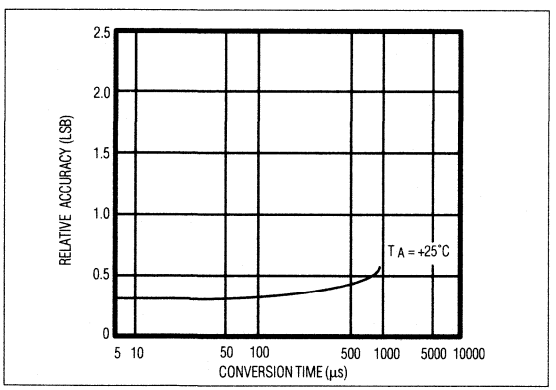


Figure 14. MAX165A/MAX166A Accuracy vs. Conversion Time

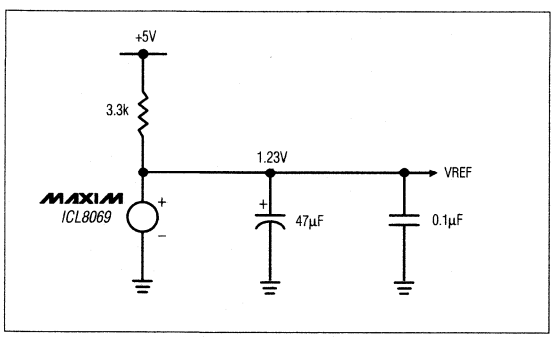


Figure 15. External Reference Circuit

Internal Reference

The MAX165/MAX166 have an internal 1.23V bandgap reference and buffer suitable for driving the reference input of the ADC. As discussed before, the reference input requires a low DC and AC driving impedance.

The reference buffer requires a 4.7µF low-ESR capacitor (tantalum or aluminum with additional 0.1µF ceramic) for compensation and to achieve low-AC impedance. If this capacitor is omitted, oscillations can occur on the REFOUT pin. If the user opts for an external reference, the REFOUT pin can be tied to V_{DD} to disable the internal reference.

Internal/External Clock

The MAX165/MAX166 can be run either with an externally applied clock or with their internal clock. In either case, the signal appearing at the clock pin is internally divided by two to provide an internal clock signal that is relatively insensitive to the input clock duty cycle. Therefore, a single conversion takes 20 input clock cycles, which corresponds to 10 internal clock cycles.

Internal Clock

The internal oscillator frequency is set by an external capacitor, C_{CLK}, and an external resistor, R_{CLK}, which are connected as shown in Figure 16a. During a conversion, a sawtooth waveform is generated on the CLK pin by charging C_{CLK} through R_{CLK} and discharging it through an internal switch. At the end of a conversion, the internal oscillator is shut down by clamping the CLK pin to V_{DD} through an internal switch. The circuit for the internal oscillator can be easily overdriven with an external clock source.

The internal oscillator provides a convenient clock source for the MAX165/MAX166. Typical conversion times versus temperature for the recommended R_{CLK} and C_{CLK} combination are shown in Figure 17. Due to process variations, the oscillation frequency for this R_{CLK}, C_{CLK} combination may vary by as much as ±50% from the nominal value shown in Figure 17. Therefore, an external clock should be used in the following situations:

1. Applications which require the conversion time to be within 50% of the minimum conversion time for the specified accuracy (5µs).
2. Applications in which time-related software constraints cannot accommodate conversion time differences, which may occur from unit to unit or over temperature for a given device.

External Clock

The CLK input of the MAX165/MAX166 may be driven directly by a 74HC or 4000B series buffer (e.g., 4049) or an LS TTL with a 5.6kΩ pullup resistor. At the end of a

CMOS µP-Compatible 5µs, 8-Bit ADCs

conversion, the device ignores the clock input and disables its internal clock signal. Therefore, the external clock may continue to run between conversions without being disabled. The duty cycle ratio of the external clock may vary from 70/30 to 30/70. As discussed previously, in order to maintain accuracy, clock rates significantly lower than the data sheet limits (4MHz) should not be used.

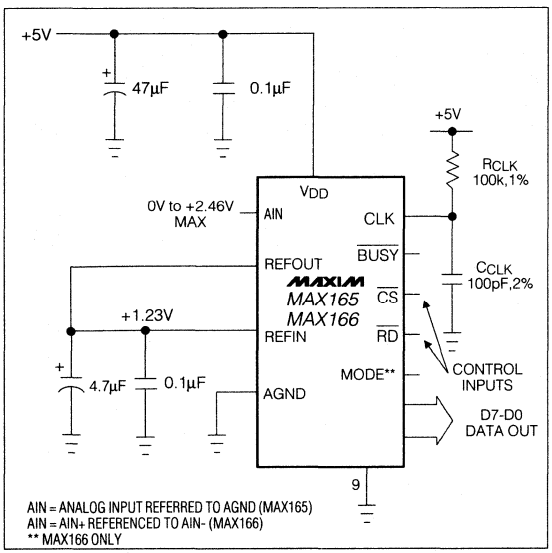


Figure 16a. MAX165/MAX166 Unipolar Configuration (Internal Reference)

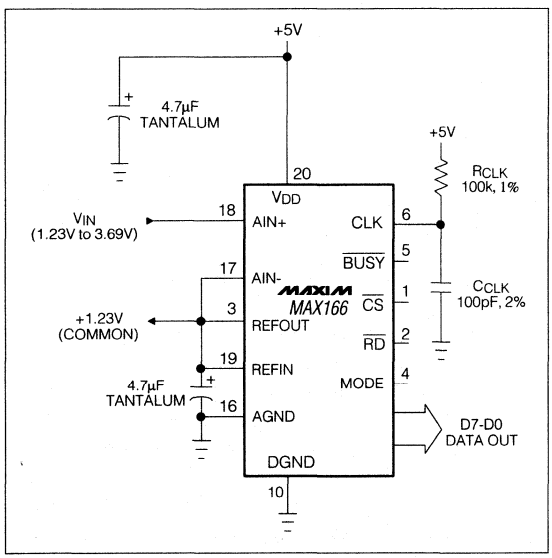


Figure 16b. MAX166 Unipolar Configuration

Applications Information

Unipolar Operation

Figures 16a and 16b show the analog circuit connections and nominal transfer characteristics (Figure 16c) for unipolar operation. Since the offset and full-scale errors of the MAX165/MAX166 are very small, it is not necessary to null these errors in most cases. If calibration is required, make adjustments as follows:

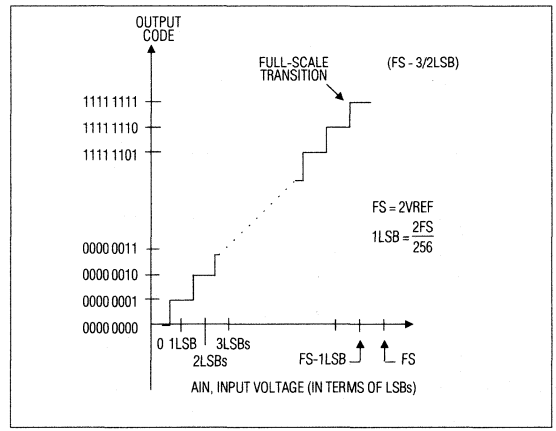


Figure 16c. Nominal Transfer Characteristic for Unipolar Operation

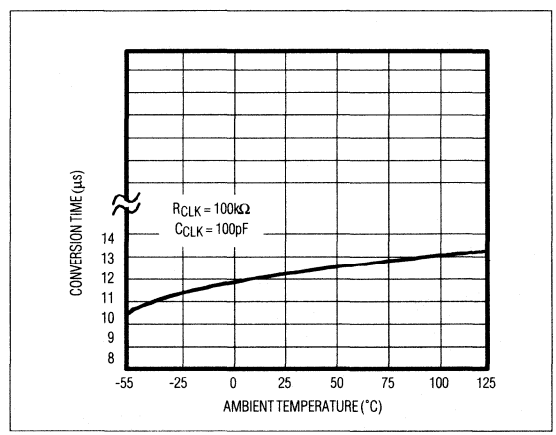


Figure 17. Typical Conversion Times vs. Temperature Using Internal Clock

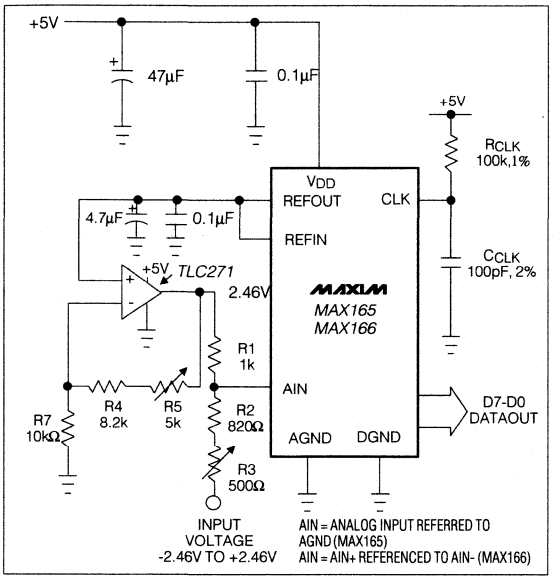


Figure 18a. MAX165/MAX166 Bipolar Configuration (Internal Reference)

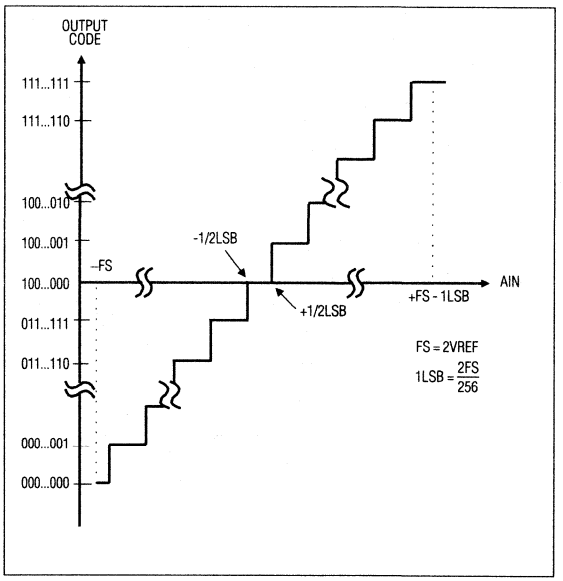


Figure 18b. Nominal Transfer Characteristic for Bipolar Operation

Offset Adjustment

The offset error can be easily adjusted using an op amp, as shown in Figure 18a. The op amp should have a common-mode input range that includes 0V. The op-amp input is initially set to +4.8mV (+1/2LSB), while its offset is varied until the ADC output code flickers between 0000 0000 and 0000 0001.

Full-Scale Adjustment

The full-scale adjustment is made by forcing the analog input, AIN, to +2.445V (FS - 3/2LSB). The reference input voltage is then varied until the ADC output code flickers between 1111 1110 and 1111 1111.

Bipolar Operation

Figure 18a shows an example of the circuit connections for bipolar operation and its nominal transfer characteristics (Figure 18B). The output code provided by the MAX165/MAX166 is offset binary. The analog input range for this circuit is ±2.46V (1LSB =19.22mV), even though the voltage appearing at the AIN pin is in the 0V to +2.46V range. In most cases, the MAX165/MAX166's accuracy is high enough that calibration will not be neccesary. If calibration is not needed, resistors R1 through R7 should have a 0.1% tolerance, with R4 and R5 replaced by one 10kΩ resistor, and R2 and R3 with one 1kΩ resistor. If calibration is required, make adjustments as follows:

Offset Adjustment

Adjust the offset error by applying an analog input voltage of +2.43V (+FS - 3/2LSB). Resistor R5 is then adjusted until the output code flickers between 1111 1110 and 1111 1111.

Full-Scale Adjustment

The full-scale errors are nulled by applying an analog input voltage of -2.45V (-FS + 1/2LSB). Resistor R3 is then adjusted until the output code flickers between 0000 0000 and 0000 0001.

Noise

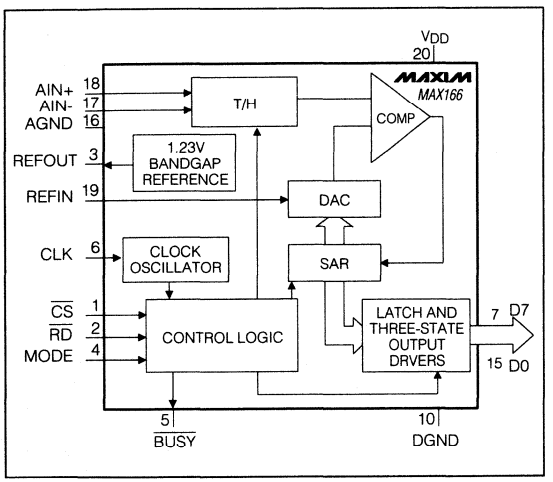
To minimize noise coupling, keep both the input signal lead to AIN and the signal return lead from AGND as short as possible. If this is not possible, a shielded cable or a twisted pair transmission line is recommended. Additionally, potential differences between the ADC ground and the signal source ground should be minimized since these voltage differences appear as errors super-imposed on the input signal. In order to minimize system noise pickup, the driving source resistance should be kept below 2kΩ.

CMOS µP-Compatible 5µs, 8-Bit ADCs

Proper Layout

For PC board layouts, take care to keep digital lines well separated from any analog lines. A single-point, analog ground, which is separate from the digital system ground, should be established near the MAX165/MAX166. Connect this analog ground point to the digital system ground through a single-track connection only. Any supply or reference bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point.

Functional Diagrams (continued)



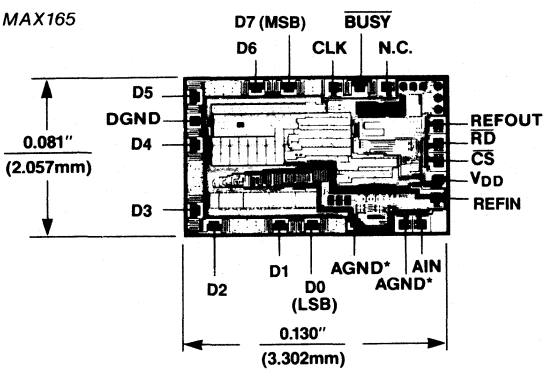
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSB)
MAX166ACPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX166BCPP	0°C to +70°C	20 Plastic DIP	±1
MAX166CCPP	0°C to +70°C	20 Plastic DIP	±1/2
MAX166DCPP	0°C to +70°C	20 Plastic DIP	±1
MAX166ACWP	0°C to +70°C	20 Wide SO	±1/2
MAX166BCWP	0°C to +70°C	20 Wide SO	±1
MAX166CCWP	0°C to +70°C	20 Wide SO	±1/2
MAX166DCWP	0°C to +70°C	20 Wide SO	±1
MAX166BC/D	0°C to +70°C	Dice*	±1
MAX166DC/D	0°C to +70°C	Dice*	±1
MAX166AEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX166BEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX166CEPP	-40°C to +85°C	20 Plastic DIP	±1/2
MAX166DEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX166AEWP	-40°C to +85°C	20 Wide SO	±1/2
MAX166BEWP	-40°C to +85°C	20 Wide SO	±1
MAX166CEWP	-40°C to +85°C	20 Wide SO	±1/2
MAX166DEWP	-40°C to +85°C	20 Wide SO	±1
MAX166AMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX166BMJP	-55°C to +125°C	20 CERDIP**	±1
MAX166CMJP	-55°C to +125°C	20 CERDIP**	±1/2
MAX166DMJP	-55°C to +125°C	20 CERDIP**	±1

*Contact factory for dice specifications.
**Contact factory for availability processing to MIL-STD-883.

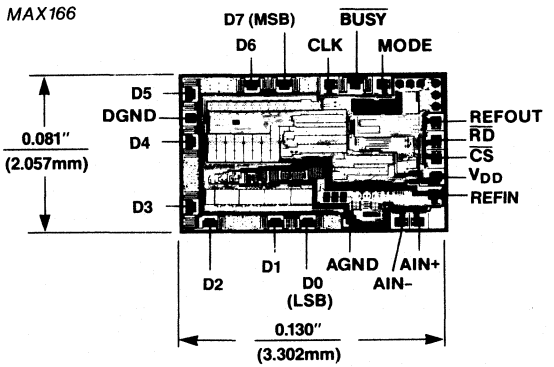
Chip Topographies

MAX165



*The two AGND pads must both be used (bonded together).

MAX166



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

14-Bit, 250ksps ADC with T/H and Voltage Reference

General Description

The MAX168 is a high-speed ,14-bit monolithic analog-to-digital converter (ADC) that includes track/hold (T/H), 20ppm/°C voltage reference, an internal clock oscillator, and an 8-bit microprocessor interface.

The MAX168 performs conversions in 3.5µs (max), and can be driven from its internal oscillator or from an external clock source. The T/H acquisition time is 500ns (max), providing a 250k samples per second (ksps) throughput rate. The device is fully tested and specified for dynamic parameters such as SNR, THD, and IMD, which are important in signal-processing applications. In addition, the part is monotonic over temperature to 14 bits, and has a maximum 1/2 LSB integral nonlinearity (INL).

The MAX168 operates from ±5V supplies and accepts bipolar analog inputs in the -3V to +3V range. The internal +3V reference can be overridden by an external reference voltage in the +2.5V to +3.1V range. Power consumption is 120mW (typ). The MAX168 is offered in 24-pin narrow DIP and wide SO packages. Contact factory for price and availability.

Features

- ♦ **14-Bit Resolution**
- ♦ **250ksps Throughput Rate**
- ♦ **3.5µs Max Conversion Time**
- ♦ **Internal Track/Hold**
- ♦ **20ppm/°C Voltage Reference**
- ♦ **1/2LSB INL Max**
- ♦ **Low Noise and Distortion:**
  -92dB THD
  81dB S/(N+D)
- ♦ **Operates from ±5V Supplies**
- ♦ **Low Power: 120mW**
- ♦ **24-Pin Narrow DIP/Wide SO Packages**

Applications

Digital-Signal Processing

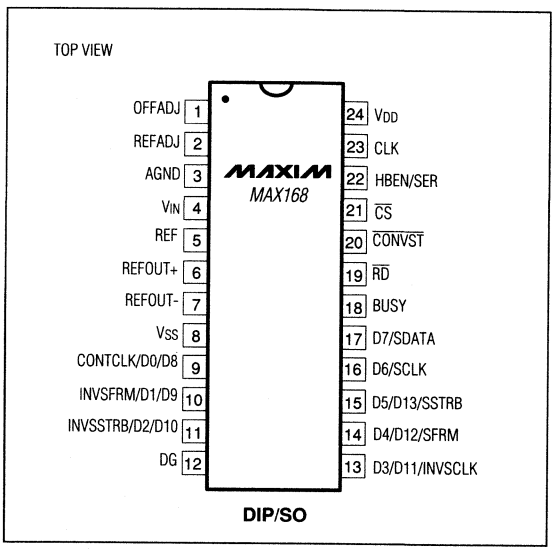
Spectrum Analysis

High-Speed Data Acquisition

Audio and Telecommunications

Industrial Process Control

Pin Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

EVALUATION KIT AVAILABLE

MAXIM

Serial-Output, 250ksps 12-Bit ADC with Reference

General Description

The MAX176 is a complete analog-to-digital converter (ADC) that achieves a 250k samples per second (ksps) sampling rate by combining a fast track/hold (0.4µs max acquisition time), a 3.5µs ADC, and a buried-zener reference. The device also saves space with serial interface and 8-pin DIP or 16-pin surface-mount SO packages.

Supply and reference decoupling capacitors are the only external components needed. The CLOCK input can be driven from an external divided-down microprocessor clock or from the serial-clock output of a microcontroller. The MAX176 works with +5V and -12V to -15V supply voltages (148mW typ power dissipation).

The MAX176's 3-wire serial interface works with general-purpose serial-to-parallel converters, such as the 74HC595, as well as with digital-signal processors and microcontrollers. Its serial 3-wire interface is fully compatible with SPI, QSPI and Microwire serial-interface standards.

Applications

Telecommunications

Digital-Signal Processing (DSP)

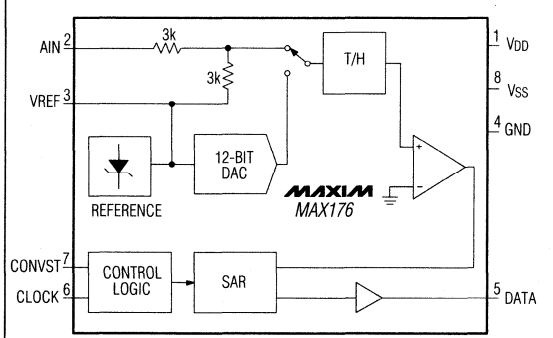
Sonar/Radar Signal Processing

Industrial Data Acquisition

Features

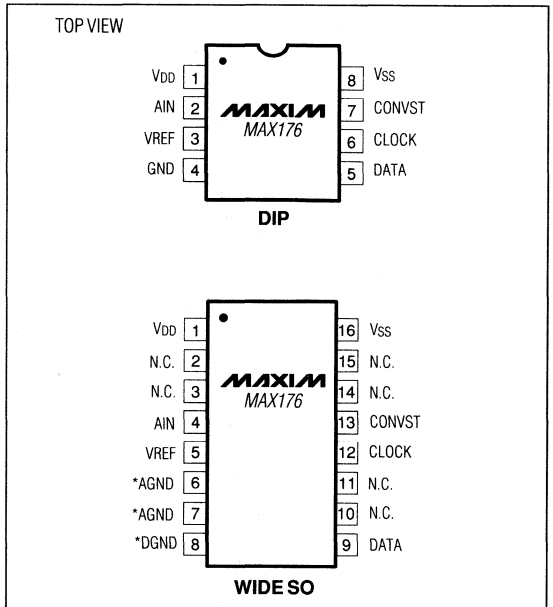
- ♦ **12-Bit Resolution and Linearity**
- ♦ **0.4µs Track/Hold Acquisition Time**
- ♦ **3.5µs Conversion Time**
- ♦ **250ksps Sampling Rate**
- ♦ **SPI-, QSPI- and Microwire-Compatible Serial Output**
- ♦ **±5V Input Voltage Range**
- ♦ **Complete with On-Chip Reference**
- ♦ **Low Power (148mW)**
- ♦ **Easy to Opto- or Transformer-Isolate**
- ♦ **Small-Footprint 8-Pin DIP, 16-Pin SO**

Functional Diagram



PIN CONFIGURATION IS 8-PIN DIP.

Pin Configurations



CONNECT PINS 6, 7, 8 TOGETHER AS CLOSE TO THE PACKAGE AS POSSIBLE.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

8-Channel, 133ksps, 12-Bit DAS with Serial Output and Reference

General Description

The MAX186/MAX188 are 133k samples per second (ksps) data-acquisition systems (DAS) that combine a 12-bit analog-to-digital converter (ADC) with 6µs conversion time, a programmable multi-channel single-ended and differential multiplexer, a 1.5µs acquisition time track/hold, and serial interface. The MAX186 has the additional benefit of an internal 4.096V reference. MAX186/MAX188 inputs are configurable for both unipolar (0V to VREF) and bipolar ($-\frac{VREF}{2}$ to $+\frac{VREF}{2}$) signals.

The MAX186/MAX188 dissipate only 12.5mW when powered from either a single +5V supply or dual ±5V supplies. To further reduce power dissipation, the devices can be instructed to fully or partially power down between conversions.

The DAS can be clocked by the serial interface for maximum throughput, or driven by the internal clock.

Features

- ♦ **8-Channel Single-Ended or 4-Channel Differential Inputs**
- ♦ **Single +5V Operation, 2.5mA Max Current**
- ♦ **133kHz Sampling Rate**
- ♦ **Built-In Track/Hold**
- ♦ **Reduced Power at Lower Sampling Rates**
- ♦ **Internal 4.096V Reference (MAX186 only)**
- ♦ **Serial Interface**
- ♦ **20-Pin Narrow DIP and Wide SO Packages**

Applications

Battery-Powered Data Logging

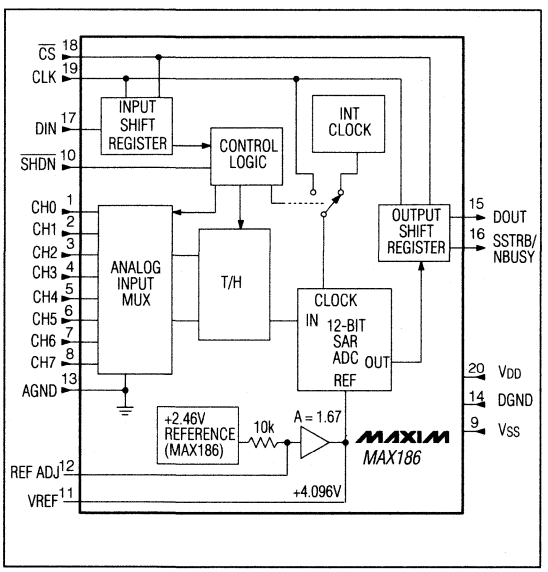
Data-Acquisition Boards for PCs

High-Accuracy Process Control

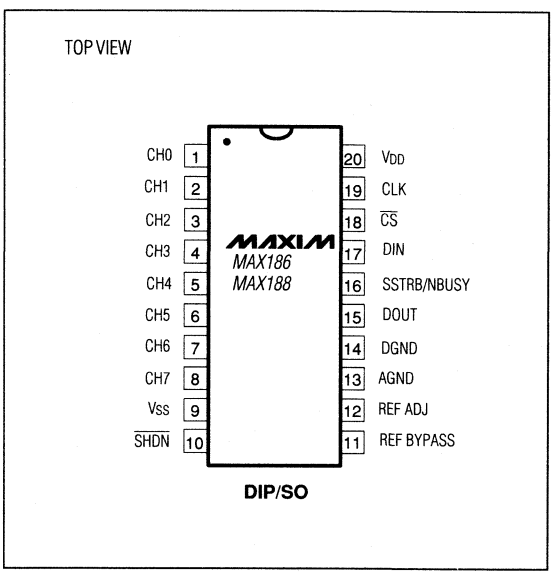
Automatic Testing Systems

Robotics

Block Diagram



Pin Configuration



DIP/SO

19-4506; Rev 0;10/91

EVALUATION KIT AVAILABLE

MAXIM

Low-Power Single-Supply 12-Bit Sampling ADC

General Description

The MAX190 is a complete monolithic CMOS 12-bit analog-to-digital converter (ADC) that features a differential input, track-and-hold (T/H), adjustable voltage reference, internal or external clock, and both parallel and serial µP interfaces. It has a conversion time of 7.5µs and tested sampling rate of 76kHz while requiring only 5mA from a single 5V supply. A 50µA power-down mode saves power in slow sampling rate applications.

No external components are needed other than decoupling capacitors for the power supply and reference. This ADC operates with an internal or external reference. The internal reference features an adjustment input for trimming system gain errors.

The MAX190 provides three interface modes. Two 8-bit parallel modes, and a serial interface mode that is compatible with common serial interface standards.

Applications

Battery-Powered Data Logging
High-Accuracy Process Control
Electro-Mechanical Systems
Data-Acquisition Boards for PCs
Automatic Testing Systems
Telecommunications
Digital-Signal Processing (DSP)

Features

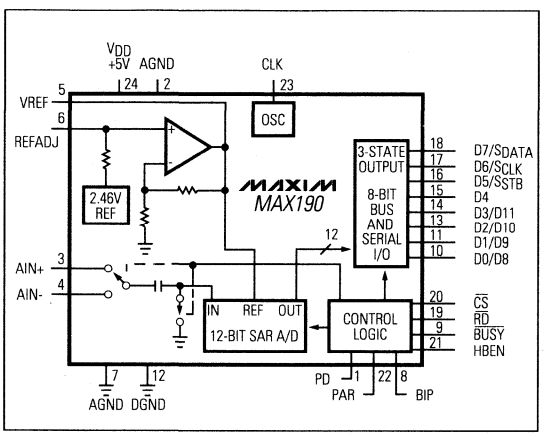
- **12-Bit Resolution, 1/2LSB Linearity**
- **Single +5V Operation 5mA Max Current**
- **Power-Down Mode-50µA Max**
- **Built-In Track-and-Hold**
- **7.5µs Conversion Time (12.5µs including T/H Acquisition)**
- **Internal Reference with Adjustment Capability**
- **Serial and 8-Bit Parallel µP Interface**
- **24-Pin Narrow DIP and Wide SO Packages**

Ordering Information

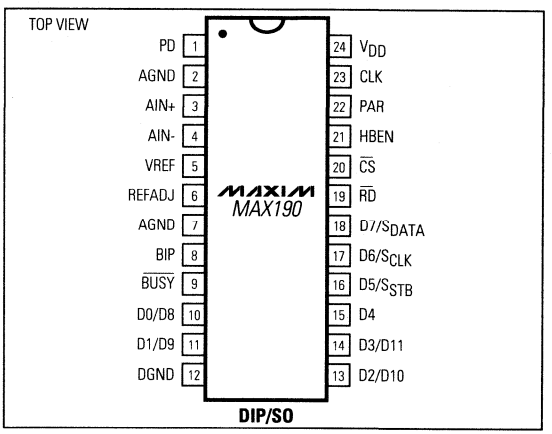
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX190ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX190BCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX190ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX190BCWG	0°C to +70°C	24 Wide SO	±1
MAX190BC/D	0°C to +70°C	Dice*	±1
MAX190AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX190BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX190AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX190BEWG	-40°C to +85°C	24 Wide SO	±1
MAX190AMRG	-55°C to +125°C	24 Narrow CERDIP	±1/2
MAX190BMRG	-55°C to +125°C	24 Narrow CERDIP	±1

Contact factory for dice specifications.

Functional Diagram



Pin Configuration



7

Low-Power Single-Supply 12-Bit Sampling ADC

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... - 0.3V, +7V

AGND, VREF, REFADJ to DGND ..... - 0.3V, V_{DD} + 0.3V
AIN+, AIN-, PD to V_{SS} ..... - 0.3V, V_{DD} + 0.3V
$\overline{CS}$, $\overline{RD}$, CLK, BIP, HBEN,
PAR to DGND ..... - 0.3V, V_{DD} + 0.3V
$\overline{BUSY}$, D0-D7 to DGND ..... - 0.3V, V_{DD} + 0.3V

Continuous Power Dissipation (any package)
to +75 °C 941mW
derate above +75°C ..... 12mW/°C
Operating Temperature Ranges:
MAX190_C__ ..... 0°C to +70°C
MAX190_E__ ..... -40°C to +85°C
MAX190_M__ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, f_{CLK} = 1.6MHz, 50% duty cycle, AIN– = AGND, BIP = GND, Slow-Memory Mode, Internal Reference Mode, External Compensation Mode, Synchronous Operation, Figure 6, T_A = T_{MIN} to T_{MAX}, unless otherwise noted). (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY (Note 2)							
Resolution				12			Bits
Integral Nonlinearity	INL		MAX190A			±1/2	LSB
			MAX190B			±1	
Differential Nonlinearity	DNL	Monotonic over temperature				±1	LSB
Offset Error			MAX190A			±1	LSB
			MAX190B			±2	
Full-Scale Error (Note 3)		T_A = +25°C, includes reference error	MAX190A			±2	LSB
			MAX190B			±3	
Full-Scale Tempco (Note 4)		Excludes internal reference drift			±0.2		ppm/°C
Conversion Time (Note 5)	t_{CONV}	Synchronous CLK (12 to 12.5 CLKs)		7.50		7.81	µs
		Internal CLK, C_L = 120pf		6	12	18	
DYNAMIC ACCURACY (sample rate = 76kHz)							
Signal-to-Noise plus Distortion Ratio	SINAD	1kHz input signal, T_A = +25°C		70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD	1kHz input signal, T_A = +25°C				-80	dB
Spurious-Free Dynamic Range	SFDR	1kHz input signal, T_A = +25°C		80			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ± 5%, f_{CLK} = 1.6MHz, 50% duty cycle, AIN– = AGND, BIP = GND, Slow-Memory Mode, Internal Reference Mode, External Compensation Mode, Synchronous Operation, Figure 6, T_A = T_{MIN} to T_{MAX}, unless otherwise noted). (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT						
Input Voltage Range (Note 6)			0		5	V
Input Leakage Current		AIN+, AIN- = 0V to 5V			±10	µA
Input Capacitance (Note 7)				45	80	pF
Track/Hold Acquisition Time					5	µs
Small-Signal Bandwidth				2		MHz
REFERENCE INPUT						
Input Voltage Range			2.5		5	V
Input Current		External reference = 5V			1	mA
Input Resistance			5	10		kΩ
INTERNAL REFERENCE						
VREF Output Voltage		T_A = +25°C	4.076	4.096	4.116	V
VREF Output TC (Note 8)		MAX190_C			50	ppm/°C
		MAX190_E			60	
		MAX190_M			80	
Output-Current Source Capability (Note 9)		T_A = +25°C			2	mA
Load Regulation		T_A = +25°C, I_{OUT} = 0mA to 2mA			4	mV
Output Short-Circuit Current				18		mA
Capacitive Load Required			4.7			µF
Power-Supply Rejection		V_{DD} = ±5%		±300		µV
REFADJ Input Adjustment Range (Note 10)			-60		30	mV
REFADJ Disable Threshold			4.5			V
REFADJ Output Voltage				2.4		V
REFADJ Input Current		REFADJ = 5V			60	µA

Low-Power Single-Supply 12-Bit Sampling ADC

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, f_{CLK} = 1.6MHz, 50% duty cycle, AIN– = AGND, BIP = GND, Slow-Memory Mode, Internal Reference Mode, External Compensation Mode, Synchronous Operation, Figure 6, T_A = T_{MIN} to T_{MAX}, unless otherwise noted). (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INPUTS							
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, CLK, HBEN, PAR, BIP				0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, CLK, HBEN, PAR, BIP		2.4			V
Input Current	I_{IN}	V_{IN} = 0V to V_{DD}				±10	µA
Input Capacitance (Note 7)	C_{IN}					10	pF
PD Input Low Voltage	V_{IL}					0.5	V
PD Input High Voltage	V_{IH}			4.5			V
PD Input Current	I_{IN}	PD = 0V to V_{DD}				±20	µA
PD External Leakage for Float State (Note 11)		Maximum current allowed for floating state				±100	nA
PD Floating State Voltage	V_{FLT}	External Compensation Mode			2.8		V
LOGIC OUTPUTS							
Output Low Voltage	V_{OL}	$\overline{BUSY}$, D0/D8-D7/S_{DATA} I_{OUT} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	$\overline{BUSY}$, D0/D8-D7/S_{DATA} I_{OUT} = -200µA		4.0			V
Three-State Leakage Current	I_L	D0/D8-D7/S_{DATA}				±10	µA
Three-State Output Capacitance (Note 7)	C_{OUT}					15	pF
POWER REQUIREMENTS							
Supply Voltage	V_{DD}	±5% for specified performance			5		V
Supply Current Internal Compensation Mode	I_{DD}	D0/D8-D7/S_{DATA} = 0V or V_{DD}, $\overline{CS}$ = $\overline{RD}$ = V_{DD}, HBEN = PAR = BIP = 0V or V_{DD}	PD = high		3.00	5.00	mA
Supply Current Power-Down Mode			PD = low CLK = low		0.02	0.05	mA
Supply Rejection (Note 12)		FS change, V_{DD} = 5.0 ±5%				±1/2	LSB
Power Dissipation		V_{DD} = 5V			15	25	mW

Note 1: Performance at power-supply tolerance limits guaranteed by power-supply rejection test.
Note 2: V_{DD} = +5V, FS = VREF.
Note 3: FS = VREF, offset nulled, ideal last code transition = FS - 3/2LSB.
Note 4: Full-Scale Tempco = ΔFS/ΔT, where ΔFS is full-scale change from T_A = +25°C to T_{MIN} or T_{MAX}.
Note 5: Conversion time defined as the number of clocks times clock period, deck has 50% duty cycle.
Note 6: AIN+, AIN- must not exceed VREF for specified accuracy.

TIMING CHARACTERISTICS (see Figures 6-10)

(V_{DD} = +5V ± 5%, f_{CLK} = 1.6MHz, 50% duty cycle , AIN– = AGND, BIP = GND, Slow-Memory Mode, Internal Reference Mode, External Compensation Mode, Synchronous Operation, Figure 6, T_A = T_{MIN} to T_{MAX}, unless otherwise noted). (Note 13)

PARAMETER	SYMBOL	CONDITIONS	T_A = +25°C			MAX190C/E		MAX190M		UNITS
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay	t_2	C_L = 50pF			120		140		160	ns
Data-Access Time (Notes 14)	t_3	C_L = 100pF			120		140		160	ns
$\overline{RD}$ Pulse Width	t_4		150			150		150		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0		0		ns
Data-Setup Time After $\overline{BUSY}$ (Note 14)	t_6				80		100		120	ns
Bus-Relinquish Time (Note 15)	t_7				100		110		120	ns
HBEN to $\overline{RD}$ Setup Time	t_8		80			100		120		ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0		0		ns
Delay Between READ Operations (Note 7)	t_{10}		200			200		200		ns
Delay Between Conversions	t_{11}		5			5		5		µs
Aperture Delay	t_{12}	Jitter < 50ps		25						ns
CLK to $\overline{BUSY}$ Delay (Note 7)	t_{13}				200		230		260	ns
S_{CLK} to S_{STB} Rise Delay	t_{14}				100		130		150	ns
S_{CLK} to S_{STB} Fall Delay	t_{15}				100		130		150	ns
$\overline{CS}$ or $\overline{RD}$ to CLK Hold Time	t_{16}		5			5		5		ns
$\overline{CS}$ or $\overline{RD}$ to CLK Setup Time (Note 7)	t_{17}				50		50		50	ns
$\overline{CS}$ to Data-Access Serial Mode	t_{18}				180		230		250	ns
$\overline{CS}$ to S_{DATA} Three-State	t_{19}				100		110		120	ns
S_{CLK} to CLK Delay	t_{20}				160		180		200	ns
S_{CLK} to S_{DATA} Delay	t_{21}				100		130		150	ns
S_{DATA} to CLK Delay	t_{22}				260		310		350	ns
S_{STB} to CLK Delay	t_{23}				260		310		350	ns

Note 7: Guaranteed by design, not subject to test.

Note 8: VREF TC = ΔVREF/ΔT, where ΔVREF is reference-voltage change from T_A = +25°C to T_{MIN} or T_{MAX}, IREF = 0mA.

Note 9: Output current should not change during conversion. This current is in addition to current required by internal DAC.

Note 10: REFADJ adjustment range is defined as the allowed voltage excursion on REFADJ relative to its unadjusted value. This will typically result in a 1.7 times larger change in the REF output. (Figure 12a).

Note 11: Floating the PD pin guarantees External Compensation Mode.

Note 12: VREF = 4.096V, External Reference.

Note 13: All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.

Note 14: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross +0.8V or +2.4V.

Note 15: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

Low-Power Single-Supply 12-Bit Sampling ADC

Pin Description

PIN	NAME	FUNCTION
1	PD	Power-Down Input: Low - power down, only the bandgap reference is active High - normal operation, internal reference compensation. Open - normal operation, external reference compensation
2	AGND	Analog Ground
3	AIN+	Sampled Analog Input
4	AIN-	Analog Input Return - pseudo-differential (see *Gain and Offset Adjustment* section)
5	VREF	Reference Buffer Output for external reference input when REFADJ is connected to V_{DD}
6	REFADJ	Reference Adjust
7	AGND	Analog Ground
8	BIP	LOW - Unipolar Inputs HIGH - Bipolar Inputs (see *Gain and Offset Adjustment* section)
9	$\overline{BUSY}$	$\overline{BUSY}$ Output is low during a conversion.
10	D0/D8	Three-State Data Outputs: LSB = D0
11	D1/D9	Three-State Data Outputs
12	DGND	Digital Ground
13	D2/D10	Three-State Data Outputs
14	D3/D11	Three-State Data Outputs: MSB = D11
15	D4	Three-State Data Output
16	D5/S_{STB}	Three-State Data Output/Strobe Output in serial mode
17	D6/S_{CLK}	Three-State Data Output/Clock Output in serial mode
18	D7/S_{DATA}	Three-State Data Output/Data Output in serial mode
19	$\overline{RD}$	READ Input. In parallel mode, low signal starts a conversion when $\overline{CS}$ and HBEN are low (memory mode). $\overline{RD}$ also enables the outputs when $\overline{CS}$ is low. In serial mode, $\overline{RD}$ = Low enables S_{CLK} and S_{STB}, $\overline{RD}$ = High forces S_{CLK} and S_{STB} into a high-impedance state
20	$\overline{CS}$	CHIP SELECT Input. Must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs in parallel mode. The falling edge of $\overline{CS}$ starts a conversion in serial mode
21	HBEN	High-Byte Enable Input. In parallel mode, HBEN = High multiplexes the 4 MSBs of the conversion result into the lower bit outputs. HBEN = High also disables conversion starts. In serial mode, HBEN = Low enables S_{CLK} to operate during the conversion only, HBEN = High enables S_{CLK} to operate continuously.
22	PAR	Sets the output mode. PAR = High selects parallel output mode. PAR = Low selects serial output mode.
23	CLK	CLOCK Input. An external TTL/CMOS compatible clock may be applied to this pin, or a capacitor (120pF nominal) may be connected between CLK and DGND to operate the internal oscillator.
24	V_{DD}	Power Supply, +5V

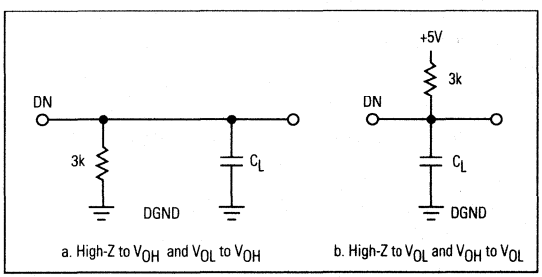


Figure 1. Load Circuits for Access Time

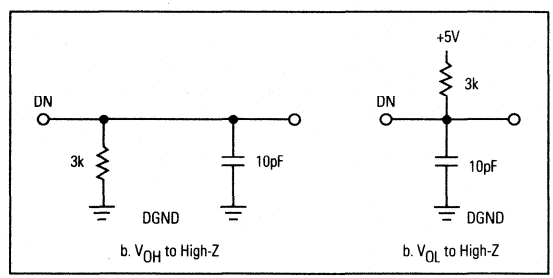


Figure 2. Load Circuits for Bus-Relinquish Time

Detailed Description

ADC Operation

The MAX190 uses successive approximation and input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. Flexible control logic provides easy interface to microprocessors (µPs), so most applications require only passive components to perform high-speed analog-to-digital (A/D) conversions. No external hold capacitor is required. Figure 3 shows the MAX190 in its simplest operational configuration.

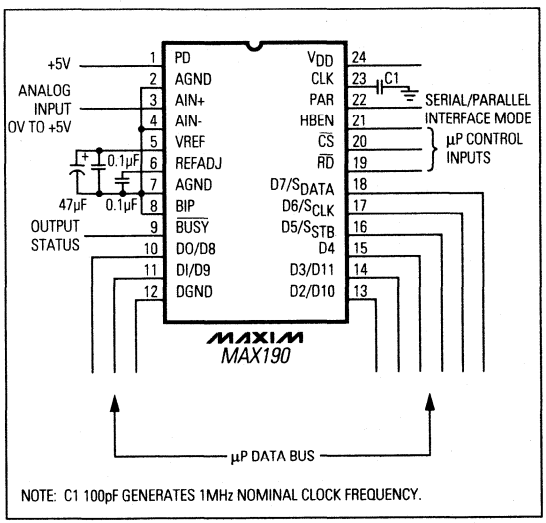


Figure 3. MAX190 Operational Diagram

Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in the Equivalent Input Circuit (Figure 4). An input signal looks at the ADC's analog input as a capacitor switching between AIN+ and AIN-. The capacitor connects to the input signal (AIN+) between conversions. When a conversion starts, the capacitor disconnects from AIN+ (thus sampling the input) and is discharged to the input return (AIN-). The ADC measures the difference in potential from AIN+ and AIN-. At the end of the conversion, the capacitor reconnects to AIN+ and charges to the input signal. An external input buffer is usually NOT needed for low-bandwidth input signals (<100Hz) because the ADC disconnects from the input during the conversion. In unbuffered applications, an input filter capacitor reduces conversion noise, but also may limit input bandwidth.

When converting a single-ended input signal, AIN- should be connected to AGND. If a differential signal is connected, consider that the configuration is pseudo-differential— only the signal side of the input channel is held by the T/H. The return side (AIN-) must remain stable within ±0.5LSB (±0.1LSB for best results) during a conversion.

Analog Input – Track/Hold

The T/H enters its tracking mode when the ADC is deselected (CHIP SELECT (CS) is high and BUSY is high). Hold mode starts approximately 25ns after a conversion is initiated. The variation in this delay from one conversion to the next (aperture jitter) is about 50ps. Figures 6–10 detail the T/H and interface timing for the various interface modes.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$$t_{ACQ} = 10(R_S + R_{IN})32pF \text{ (but never less than 5µs)}$$

where R_{IN} = 10kΩ, and R_S = source impedance of the input signal.

Input Bandwidth

The ADC's input tracking circuitry has excellent large-signal and wide-bandwidth characteristics, and is not slew limited like previous ADC T/Hs. It is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sample rate (76kHz) by using undersampling techniques. Note that if undersampling is used to measure high-frequency signals, special care must be taken to avoid aliasing errors. Without adequate input filtering, high-frequency noise may be aliased into the measurement band.

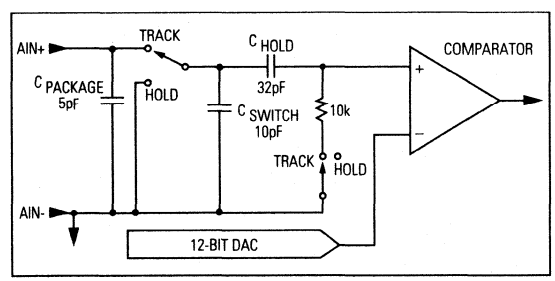


Figure 4. Equivalent Input Circuit

Low-Power Single-Supply 12-Bit Sampling ADC

Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow AIN+ to swing from -0.3V to V_{DD}+0.3V with no risk of damage to the ADC. However, for accurate conversions near full scale, AIN+ should not exceed V_{DD} or AGND by more than 50mV because A/D accuracy is affected when the protection diodes are even slightly forward biased.

Starting a Conversion

The ADC is controlled by the $\overline{CS}$, $\overline{READ}$ ($\overline{RD}$), and High-Byte Enable (HBEN) inputs as shown in Figure 6. The T/H enters hold mode and a conversion starts at the falling edge of $\overline{CS}$ and $\overline{RD}$ while HBEN is low. $\overline{BUSY}$ goes low as soon as the conversion starts. On the falling edge of the 13th input clock pulse after the conversion starts, $\overline{BUSY}$ goes high and the conversion result is latched into three-state output buffers.

Internal/External Clock

Figure 5 shows the MAX190 clock circuitry. The ADC includes internal circuitry to generate a clock with an external capacitor. 120pF connected between CLK and DGND generates a 1MHz nominal clock frequency. Alternatively, an external clock (up to 1.6MHz) can be applied to CLK. When using an external clock source, acceptable clock duty cycles are between 45% and 55%.

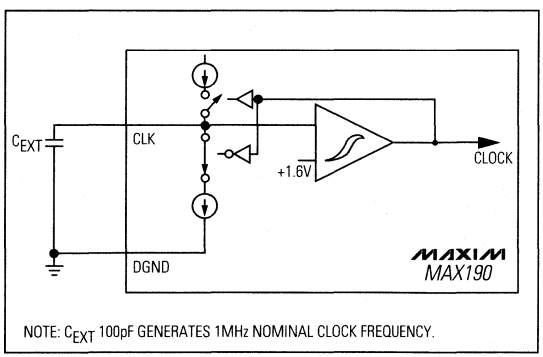


Figure 5. Internal Clock Circuit

Digital Interface

Clock and Control Synchronization

For best analog performance, the MAX190 clock should be synchronized to the conversion start signals ($\overline{CS}$ and $\overline{RD}$) as shown in Figure 6. At least 100ns should separate the start of a conversion from the nearest clock edge. This ensures that CLK transitions are not coupled to the analog input and sampled by the T/H. The magnitude of this feedthrough is only a few millivolts. When the clock and conversion start signals are synchronized, small end-point errors (offset and full-scale) are the most that can be generated by clock feedthrough. Even these errors (which can be trimmed out) can be avoided by ensuring that the start of a conversion ($\overline{RD}$ or $\overline{CS}$ falling edge) does not occur within 100ns of a clock transition (Figure 6).

In asynchronous mode, where CLK and conversion start signals ($\overline{CS}$ and $\overline{RD}$) are not synchronous, full-accuracy specification perfomances are realized with 0.8MHz clock; this insures a full 625ns for the MSB decision. In asynchronous mode, with clock frequencies greater than 0.8MHz, less than 625ns MSB decision times can occur. This shortened decision time can result in linearity errors at mid-scale. This linearity error can appear in the synchronous mode when the $\overline{CS}$ and $\overline{RD}$ to CLK hold (t_{16}) and setup (t_{17}) times are violated (Figure 6). Frequency components caused by clock and conversion start signals' overlap can increase the apparent input noise.

Output Data Format

The data output from the MAX190 is straight binary in unipolar mode. The 12 data bits can be output either in two 8-bit bytes or as a serial output. The data-bus output format is shown in Table 1.

A 2-byte read uses outputs D7–D0. Byte selection is controlled by HBEN. When HBEN is low, the lower 8 bits appear at the data outputs. When HBEN is high, the upper 4 bits appear at D0–D3 with the leading 4 bits low in locations D4–D7.

Timing and Control

Conversion start and data read operations are controlled by the HBEN, $\overline{CS}$, and $\overline{RD}$ digital inputs. A logic low is required on all three inputs to start a conversion, and once the conversion is in progress it cannot be restarted. $\overline{BUSY}$ remains low during the entire conversion cycle.

Two parallel interface modes and one serial mode are outlined in the timing diagrams of Figures 7–10.

Slow-Memory Mode

In slow-memory mode, the device appears to the µP as a slow peripheral or memory. Conversion is initiated with a read instruction (see Figure 7 and Table 2). PAR is set high. Taking $\overline{CS}$ and $\overline{RD}$ low starts the conversion. The input is sampled on the falling edge of $\overline{RD}$. $\overline{BUSY}$ remains

low while the conversion is in progress. The previous conversion result appears at the digital outputs until the end of conversion when BUSY returns high. The output latches are then updated with the newest results of the 8 LSBs on D7–D0. A second read operation with HBEN high places the 4 MSBs, with 4 leading 0s, on data outputs D7–D0. The second read operation does not start a new conversion because HBEN is high.

ROM Mode

As in slow-memory mode, D7–D0 are used for 2-byte reads. A conversion starts with a read instruction with HBEN and $\overline{CS}$ low. The T/H samples the input on the falling edge of $\overline{RD}$ (see Figure 8 and Table 3). PAR is set high. At this point the data outputs contain the 8 LSBs from the previous conversion. Two more read operations

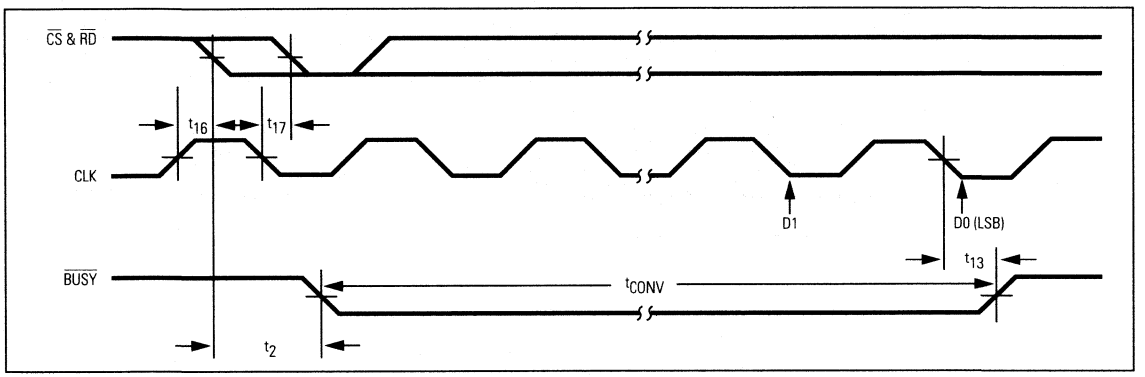


Figure 6. $\overline{CS}$, $\overline{RD}$, HBEN and CLK Synchronous Operation

Table 1. Data-Bus Output, $\overline{CS}$ = $\overline{RD}$ = Low

PIN NAME	D7/ S_{DATA}	D6/ S_{CLK}	D5/ S_{STB}	D4	D3/ D11	D2/ D10	D1/ D9	D0/ D8
HBEN = 0, PAR = 1, PARALLEL MODE	D7	D6	D5	D4	D3	D2	D1	D0
HBEN = 1, PAR = 1, PARALLEL MODE	Low	Low	Low	Low	D11	D10	D9	D8
HBEN = X, PAR = 0, SERIAL MODE, $\overline{RD}$ = 0	S_{DATA}	S_{CLK}	S_{STB}	Low	Low	Low	Low	Low
HBEN = X, PAR = 0, SERIAL MODE, $\overline{RD}$ = 1	S_{DATA}	Three-Stated	Three-Stated	Low	Low	Low	Low	Low

Note: D7/S_{DATA} – D0/D8 are the ADC data output pins.
D11 – D0 are the 12-bit conversion results, D11 is the MSB.

S_{DATA} = Three-state data output. Data output in serial mode.
S_{CLK} = Three-state data output. Clock output in serial mode.
S_{STB} = Three-state data output. Strobe output in serial mode.

Table 2. Slow-Memory Mode, Two-Byte Read Data-Bus Status

PIN NAME	D7/ S_{DATA}	D6/ S_{CLK}	D5/ S_{STB}	D4	D3/ D11	D2/ D10	D1/ D9	D0/ D8
FIRST READ (New Data)	D7	D6	D5	D4	D3	D2	D1	D0
SECOND READ (New Data)	Low	Low	Low	Low	D11	D10	D9	D8

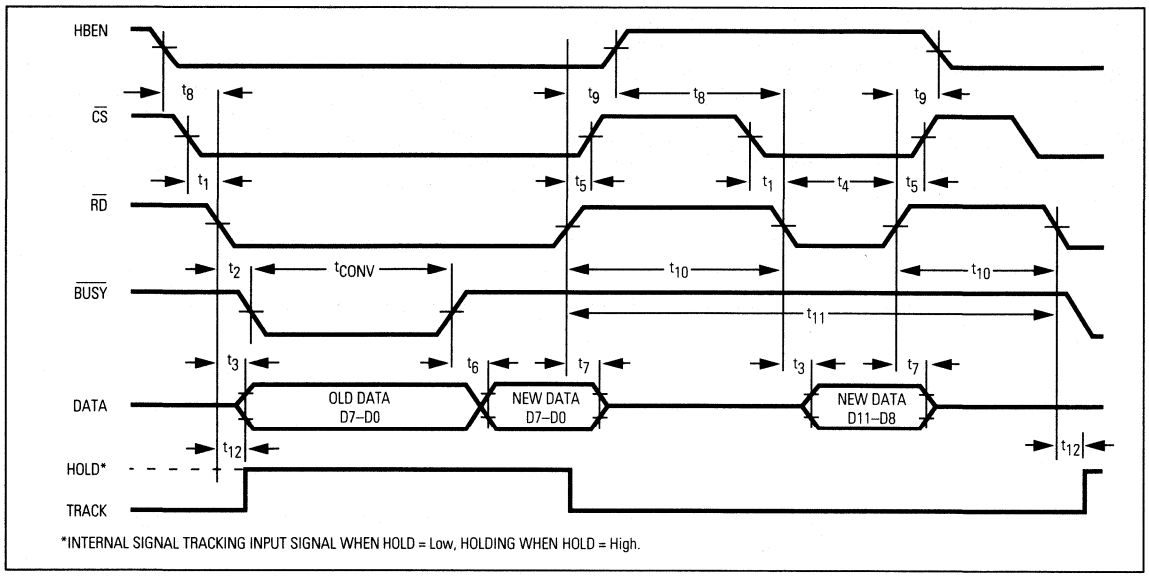


Figure 7. Slow-Memory Mode, Two-Byte Read Data-Bus Status

are needed to access the conversion result. The first occurs with HBEN high, where the 4 MSBs with 4 leading 0s are accessed. The second read, with HBEN low, outputs the 8 LSBs and also starts a new conversion.

Figure 9 and Table 4 show how to read output data within one conversion cycle without starting another conversion. Trigger the falling edge of read on the rising edge of the first clock cycle after conversion end (when $\overline{BUSY}$ goes high). As mentioned previously, two more read operations (after $\overline{BUSY}$ goes high) are needed to access the conversion results. The only difference is that now the low byte can be read first. This happens by allowing the first read operation to occur with HBEN low, where the 8 LSBs are accessed. The second read, with HBEN high, accesses the 4 MSBs with 4 leading zeros.

Serial-Interface Mode

The serial mode is compatible with MicroWire and SPI serial interfaces. In addition, a framing signal (S_{STB}) is provided that allows the device to interface with the TMS320 family of µPs. Conversion begins when $\overline{CS}$ goes low, causing the T/H to sample the input (Figure 10). PAR is set low. The $\overline{CS}$ signal is internally latched on the first falling edge of CLK, and the conversion begins. The S_{DATA} line remains in a high-impedance state until conversion begins. During the MSB decision, S_{DATA} remains low, while S_{STB} goes high to indicate that a data frame is beginning. The data is then shifted out serially until the end of conversion. Trailing 0s are inserted indefinitely in the data stream until $\overline{CS}$ returns high. The S_{CLK} output is synchronous with the internal or external clock.

For interface flexibility, S_{DATA}, S_{CLK} and S_{STB} signals enter a high-impedance state when $\overline{RD}$ is set high, and are enabled when $\overline{RD}$ is set low. Also, when HBEN is set high, S_{CLK} drives continuously regardless of conversion status. This is useful with µPs that require a continuous serial clock. On the other hand, HBEN may be set low so that S_{CLK} is output only during the conversion cycle, while the converter internal clock runs continuously.

Application Information

Power-Down Mode/ Initialization After Power-Up

In some battery-powered systems, it is desirable to power down or to remove power from the ADC during inactive periods. To power down the MAX190, Power Down (PD) should be set to low. In this mode, all internal ADC circuitry is off except the reference circuit, which consumes less than 50µA (assuming all signals $\overline{CS}$, $\overline{RD}$, CLK, and HBEN are static and within 200mV of the supplies. To initialize the MAX190 at power up, perform one read operation with HBEN low and disregard the data outputs. Figure 11 shows a practical way to drive the PD pin.

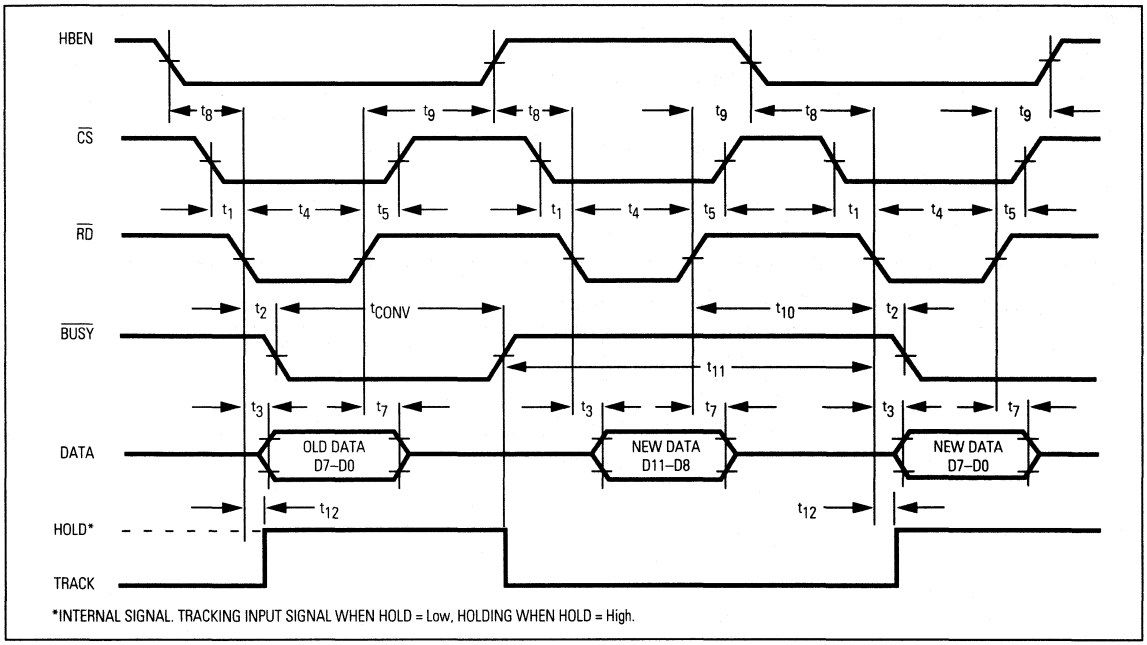


Figure 8. ROM Mode, Two-Byte Read Data-Bus Status

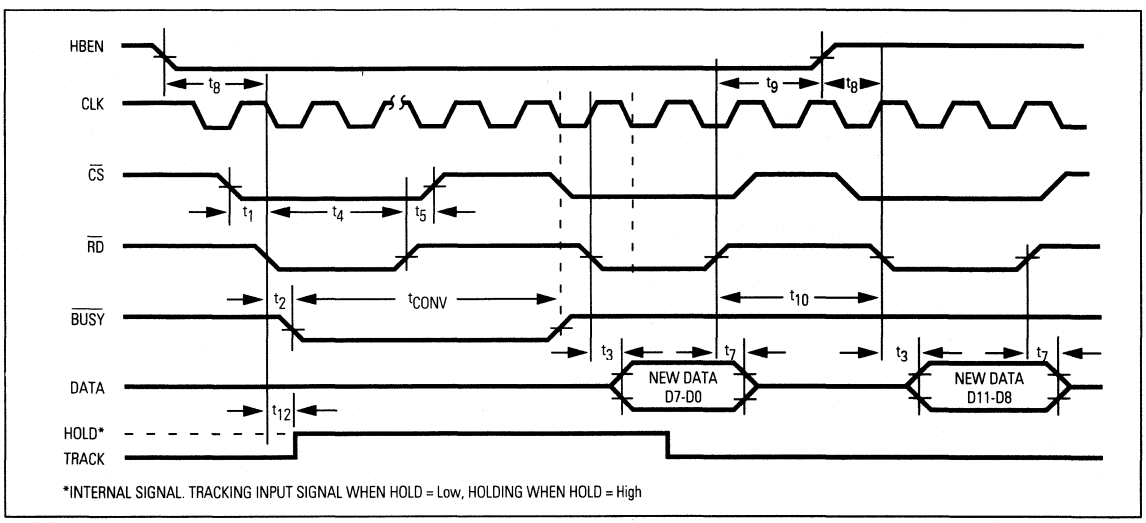


Figure 9. ROM Mode, Two-Byte Read within One Conversion Timing Diagram

Table 3. ROM Mode, Two-Byte Read Data-Bus Status

PIN NAME	D7/ S_{DATA}	D6/ S_{CLK}	D5/ S_{STB}	D4	D3/ D11	D2/ D10	D1/ D9	D0/ D8
FIRST READ (Old Data)	D7	D6	D5	D4	D3	D2	D1	D0
SECOND READ (New Data)	Low	Low	Low	Low	D11	D10	D9	D8
THIRD READ (New Data)	D7	D6	D5	D4	D3	D2	D1	D0

Table 4. ROM Mode, Two-Byte Read Data-Bus Status without Starting a Conversion Cycle

PIN NAME	D7/ S_{DATA}	D6/ S_{CLK}	D5/ S_{STB}	D4	D3/ D11	D2/ D10	D1/ D9	D0/ D8
FIRST READ (Old Data)	D7	D6	D5	D4	D3	D2	D1	D0
SECOND READ (New Data)	D7	D6	D5	D4	D3	D2	D1	D0
THIRD READ (New Data)	Low	Low	Low	Low	D11	D10	D9	D8

In the MAX190, power-down performance can be optimized for a given conversion rate by selecting either internal or external reference compensation:

Internal Compensation

The connection for internal compensation with reference adjustment is shown in Figure 12a. In this mode, the reference stabilizes quickly enough so that a conversion typically starts within 35µs after the ADC is reactivated (PD pulled high). In this compensation mode, the reference buffer requires longer recovery time from SAR transients, therefore requiring a slower clock rate (and conversion time). With internal reference compensation, the typical conversion time rises to 24µs (Figure 12b).

External Compensation

Figure 13a shows the connection for external compensation. In this mode, an external 4.7µF capacitor compensates the reference output amplifier, allowing for maximum conversion time and lowest conversion noise. However, when reactivating the ADC after power- down, the reference takes typically 2ms to charge the 4.7µF capacitor, so more time is required before a conversion can start (Figure 13b). Thus, the average current consumed in power-up/power-down operations is higher in external compensation mode than in internal compensation mode.

Internal Reference

The internal 4.096V reference is available at VREF and must be bypassed to AGND with a 4.7µF capacitor with low ESR (less than 1/2Ω) in parallel with a 0.1µF capacitor. This minimizes noise and maintains a low reference impedance at high frequencies. The reference output can be disabled by connecting REFADJ to V_{DD} when using an external reference.

Gain and Offset Adjustment

Figure 14 plots the nominal, unipolar input/output (I/O) transfer function of the MAX190. Code transitions occur halfway between successive-integer LSB values. Output coding for unipolar operation is straight binary with 1LSB = 1.00mV (4.096V/4096).

Figures 15a and 12a show how to adjust the ADC gain in applications that require full-scale range adjustment. The connection shown in Figure 15a provides ±0.5% or ±20 LSBs of adjustment range and is recommended for applications that use an external reference. On the other hand, Figure 12a is recommended for applications that use the internal reference because it uses fewer external components.

If both offset and full scale need adjustment, the circuit in Figure 15b is recommended. For single-supply ADCs, it is virtually impossible to null system negative offset errors. However, the MAX190 input configuration is pseudo-differential—only the difference in voltage be-

tween AIN+ and AIN- will be converted into its digital representation. By applying a small positive voltage to AIN-, the zero input voltage at AIN+ can be adjusted to above or below AIN- voltage, thus nulling positive or negative system offset errors. R9 and R10 can be removed for applications that require only positive system errors to be nulled. For the 0V to +4.096V input range, apply 1/2 LSB (0.50mV) to the analog input and adjust R5 so the digital output code changes between 0000 0000 0000 and 0000 0000 0001. To adjust full scale, apply FS-1 1/2 LSB (4.09525V) and adjust R2 until the output code changes between 1111 1111 1110 and 1111 1111 1111. Because interaction occurs between adjustments, offset should be adjusted before gain. If an input gain of 2 is acceptable, the connection in Figure 15b can be simplified by removing R7 and R8.

The MAX190 input accepts input voltages between GND and V_{CC}; therefore, bipolar input signals around ground cannot be converted. The MAX190 can be configured for bipolar operation on its pseudo-differential input. Instead of using AIN- as an analog input return, AIN- can be set to a different **positive** potential voltage above ground (BIP pin is set high). The sampled analog input (AIN+) can swing to any positive voltage above and below AIN- and the ADC performs bipolar conversions with respect to AIN-. Figure 16 shows the bipolar input transfer function with AIN- connected up to mid-scale (VREF/2V).

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, crosstalk from the data pins to the ADC

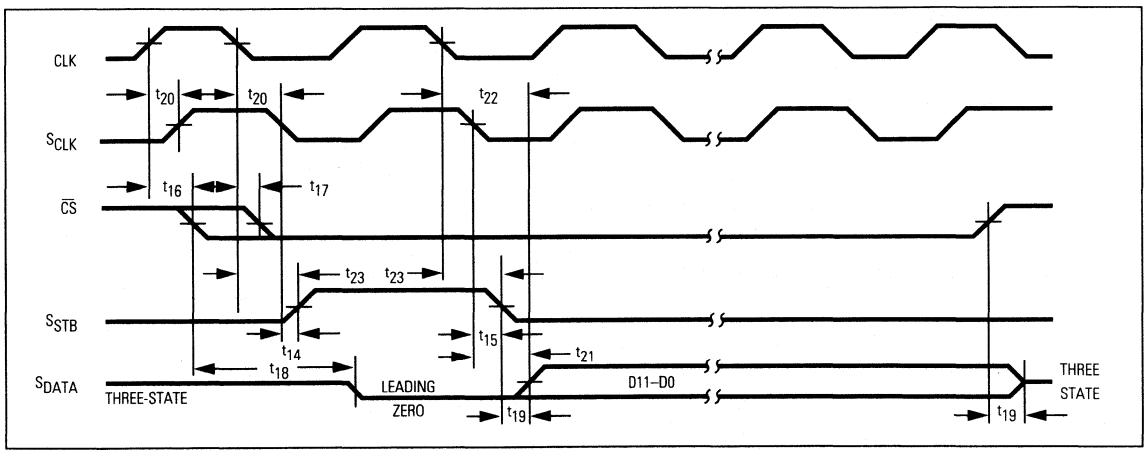


Figure 10. Serial-Interface Mode Timing Diagram

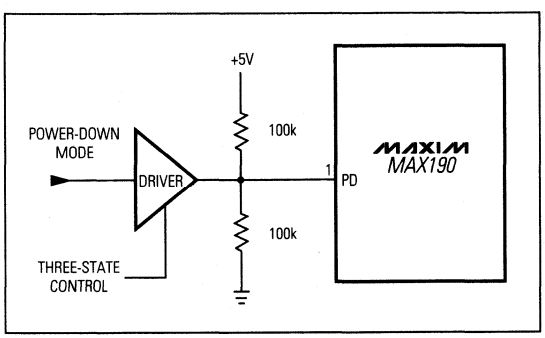


Figure 11. Drive Circuit for PD Pin

comparator may generate error. Slow-memory mode avoids this problem by placing the µP in a wait state during the conversion. In ROM mode, if the data bus is active during the conversion, it should be isolated from the ADC using three-state drivers.

The ADC generates considerable digital noise in ROM mode when $\overline{RD}$ or $\overline{CS}$ go high and the output data drivers are disabled after a conversion has started. This noise can cause large errors if it occurs when the SAR latches a comparator decision. To avoid this problem, $\overline{RD}$ and $\overline{CS}$ should be active for less than one clock cycle. If this is not possible, $\overline{RD}$ or $\overline{CS}$ should go high at the rising edge of CLK, since the comparator output is always latched on falling edges of CLK.

Low-Power Single-Supply 12-Bit Sampling ADC

Layout, Grounding, Bypassing

Printed circuit boards should be used for best system performance. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Take care not to run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 17 shows the recommended system ground connections. A single-point analog ground ("star" ground point) should be established at AGND, separate from the logic ground. All other analog grounds and DGND should be connected to this ground. No other digital system grounds should be connected to this single-point analog ground. The ground return to the power supply from this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the high-speed comparator in the ADC. These supplies should be bypassed to the single-point analog ground with 0.1µF and 10µF bypass capacitors. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected as a lowpass filter to filter out supply noise (Figure 17).

Dynamic Performance

High-speed sampling capability and 76kHz throughput make the MAX190 ideal for wideband-signal processing. To support these and other related applications, Fast Fourier Transform (FFT) test techniques guarantee the ADC's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low-distortion sine wave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm which determines its spectral content. Conversion errors are then seen as spectral elements outside the fundamental input frequency.

ADCs have traditionally been evaluated by specifications such as Zero and Full-Scale Error, Integral Nonlinearity (INL), and Differential Nonlinearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals, but are less useful in signal-processing applications where the ADC's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

Signal-to-Noise Ratio and Effective Number of Bits

Signal-to-Noise Ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals, except signal harmonics. Signal-to-Noise + Distortion ratio (SINAD) is the same as the SNR, but includes signal harmonics.

The theoretical minimum A/D noise is caused by quantization error and is a direct result of the ADC's resolution: SNR = (6.02n + 1.76)dB where n is the number of bits of resolution. 74dB is the SNR of a perfect 12-bit ADC.

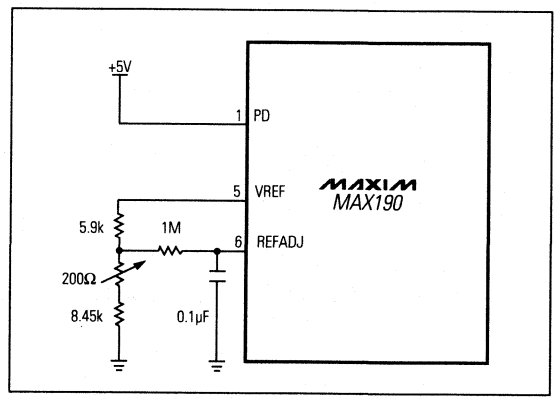


Figure 12a. Internal Compensation Mode with Internal Reference Adjustment Circuit

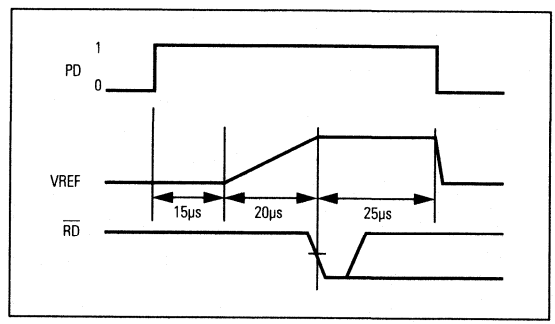


Figure 12b. Low Average Power Mode Operation (Internal Compensation)

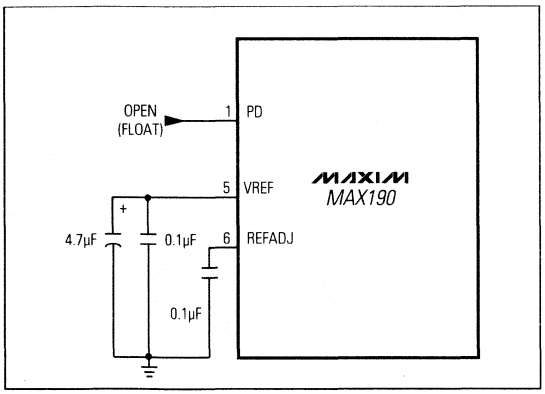


Figure 13a. External Compensation Mode Circuit

By transposing the equation that converts resolution to SNR we can compute the effective resolution or the "effective number of bits" the ADC provides from the measured SNR:

$$n = (SNR - 1.76)/6.02$$

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one-half the sample rate) to the fundamental itself. This is expressed as:

$$THD = 20Log[\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_5^2 + ... + V_N^2)}/V_1]$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through nth harmonics.

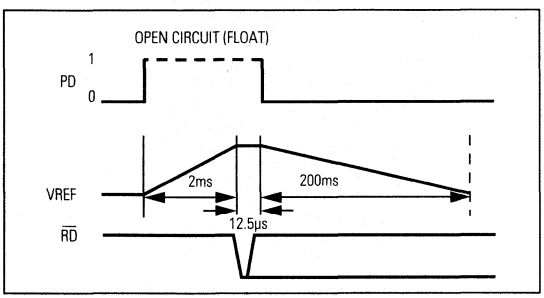


Figure 13b. Low Average Power Mode Operation (External Compensation)

Spurious-Free Dynamic Range

Spurious-free dynamic range is the ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one-half the sample rate). Usually this peak occurs at some harmonic of the input frequency. But if the ADC is exceptionally linear, it can occur at a random peak in the ADC's noise floor.

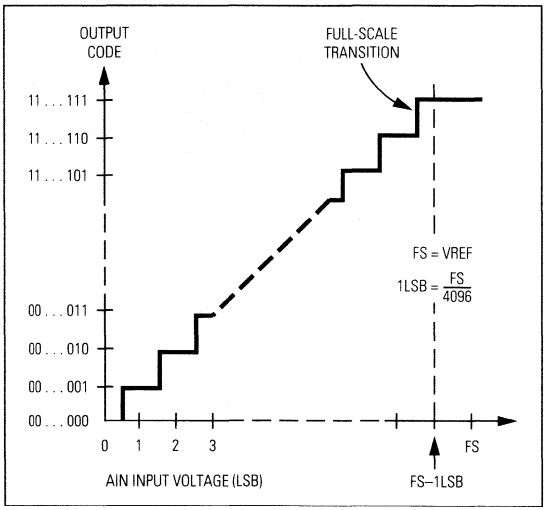


Figure 14. MAX190 Unipolar Transfer Function

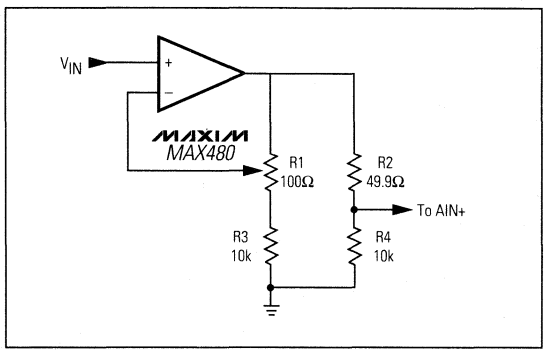


Figure 15a. Trim Circuit for Gain (±0.5%)

Low-Power Single-Supply 12-Bit Sampling ADC

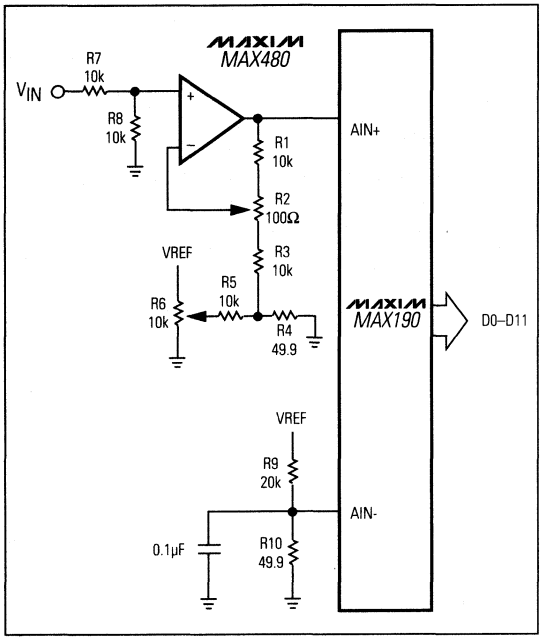


Figure 15b. Offset (±10mV) and Gain (±1%) Trim Circuit

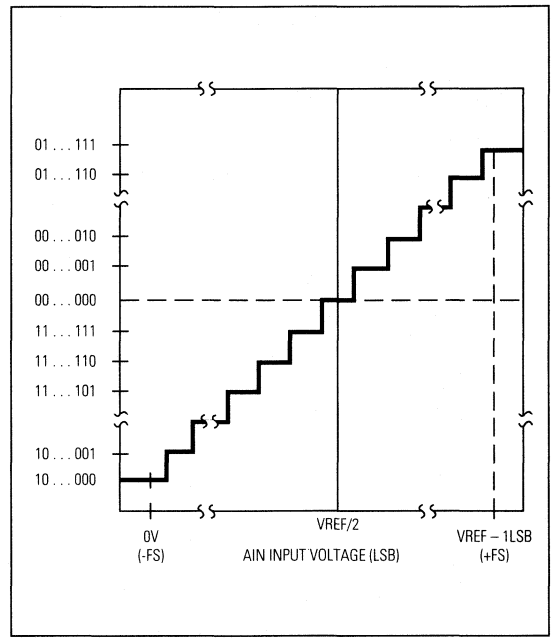


Figure 16. MAX190 Bipolar Transfer Function

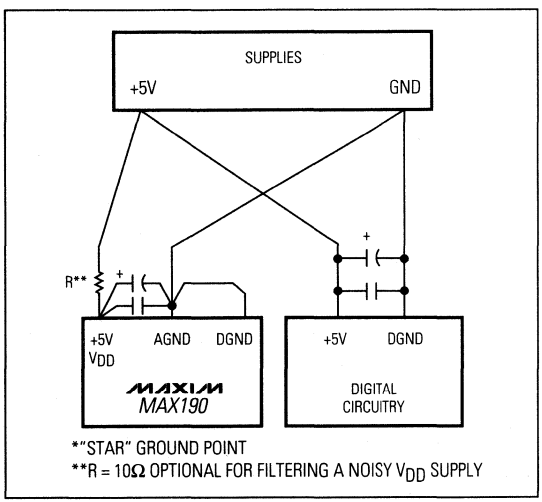
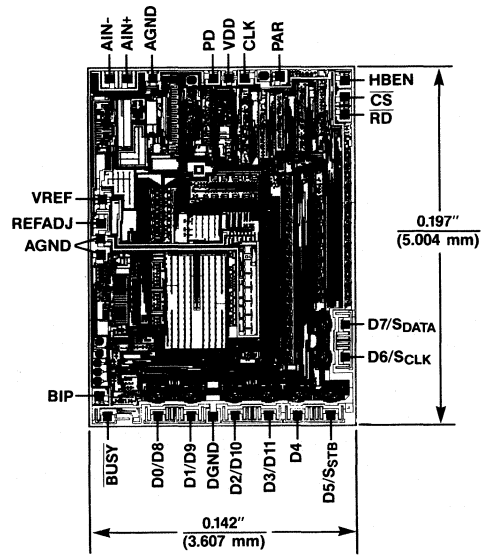


Figure 17. Power-Supply Grounding Connection

Chip Topography



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

Low-Power, Single-/Dual-Supply, 12-Bit Sampling ADC

General Description

The MAX191 is a complete monolithic CMOS 12-bit analog-to-digital converter (ADC) that features a differential input, track-and-hold (T/H), adjustable voltage reference, internal or external clock, and both parallel and serial µP interfaces. It has a conversion time of 7.5µs and tested sampling rate of 100kHz while requiring only 5mA from a single 5V supply. A 50µA power-down mode saves power in a slow sampling rate applications.

No external components are needed other than decoupling capacitors for the power supply and reference. This ADC operates with an internal or external reference. The internal reference features an adjustment input for trimming system gain errors.

The MAX191 provides three interface modes. Two 8-bit parallel modes, and a serial-interface mode that is compatible with common serial-interface standards.

Applications

Battery-Powered Data Logging

High-Accuracy Process Control

Electro-Mechanical Systems

Automatic Testing Systems

Data-Acquisition Boards for PCs

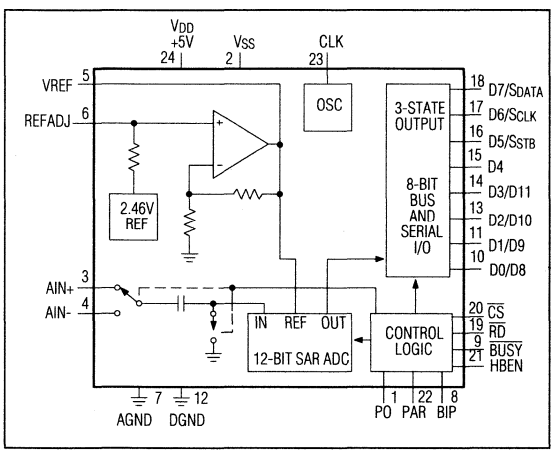
Telecommunications

Digital-Signal Processing (DSP)

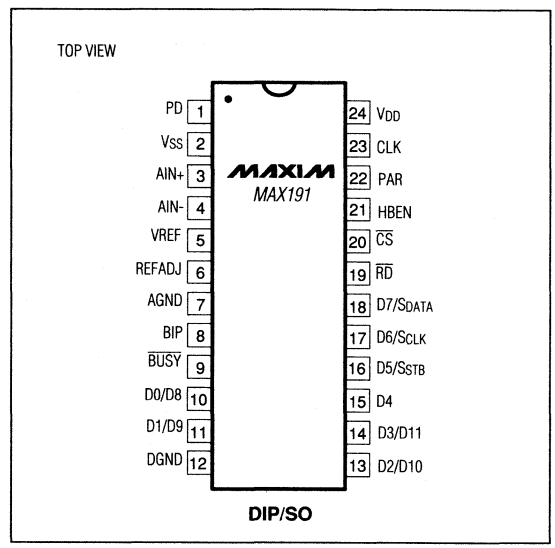
Features

- **12-Bit Resolution,1/2LSB Linearity**
- **Single +5V or Dual ±5V Operation 5mA Max Current**
- **Power-Down Mode – 50µA Max**
- **Built-In Track-and-Hold**
- **7.5µs Conversion Time (9.5µs Including T/H Acquisition)**
- **Internal Reference with Adjustment Capability**
- **Serial and 8-Bit Parallel µP Interface**
- **24-pin Narrow DIP and Wide SO Packages**

Functional Diagram



Pin Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

16-Bit, Self-Calibrating, 10µs Sampling ADC

MAX195

General Description

The MAX195 is a 16-bit successive-approximation analog-to-digital converter (ADC) that combines high speed, high accuracy, and low power consumption. Internal calibration circuitry corrects linearity/offset errors and maintains full 16-bit performance over the full operating temperature range without external adjustments. The capacitor-DAC architecture provides an inherent 100k samples per second (ksps) track/hold function.

The MAX195, with an external reference (+4V to +5V), offers a unipolar (0V to REF+) or bipolar (REF- to REF+) pin-selectable input range. Separate analog and digital supplies minimize digital-noise coupling.

The chip-select ($\overline{CS}$) input controls the three-state serial-data output. The output can be read either during conversion as the bits are determined, or following conversion at up to 5MHz using the serial clock (SCLK). Calibration is performed at power-up and can be initiated at any time using the $\overline{RESET}$ pin. The end- of-conversion (EOC) output can be connected directly to the convert (CONV) input for continuous, full-speed conversions.

Applications

Industrial Controls

Robotics

Multiple Transducer Measurements

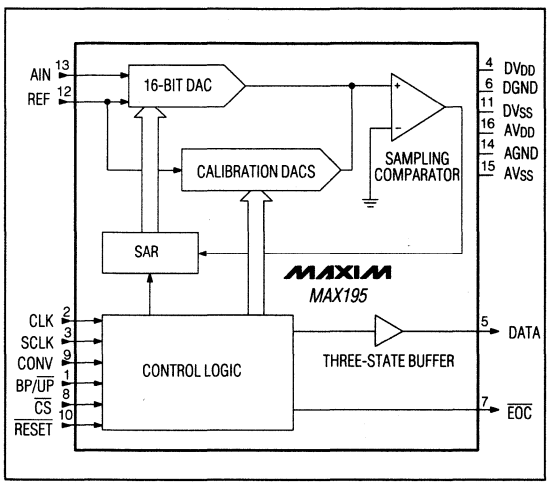
Vibrational Analysis

Analytical Instruments

Audio

Digital-Signal Processing

Functional Diagram

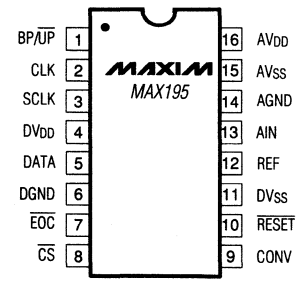


Features

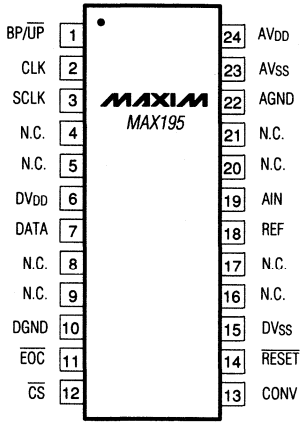
- ♦ **16-Bit Resolution and Linearity**
- ♦ **Internal Calibration of Linearity and Offset**
- ♦ **100ksps Sampling ADC**
- ♦ **Built-In Track/Hold**
- ♦ **AC and DC Specified**
- ♦ **Unipolar (0V to REF+) and Bipolar (REF- to REF+) Input Range**
- ♦ **100mW Max Power Consumption**
- ♦ **Three-State Serial-Data Output**
- ♦ **Small 16-Pin DIP Package**

Pin Configurations

TOP VIEW



DIP



SO

7

Video Products

8

* Advance Information – first page of data sheet in preparation.

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	V_{OS} (mV max)	Output Current (mA max)	Supply Voltage (V)	I_{BIAS} (nA max)	Features	Price† 1000-up ($)
VIDEO AMPLIFIERS								
MAX404	80 ($A_V \geq 2$)	500	8	50	±5	3µA	Broadcast-quality video op amp, 0.01°/0.05% diff phase/gain, symmetrical inputs, 70dB CMRR, 66dB A_{VOL}	2.68
MAX408/428/448	100($A_V \geq 3$)	90	6 to 12	50/amp.	±5	1.1µA	Single/dual/quad op amps, high output drive	3.02/4.06/6.74
MAX452	50	300	5	14	±5	10	Unity-gain stable, drives 75Ω coax cable	2.40
MAX457	70	300	5	15	±5	1	Dual, unity-gain stable, drives 75Ω coax cable	4.45
VIDEO BUFFERS								
MAX405	180	650	4	60	±5	2µA	Broadcast quality, 0.99V/V gain guaranteed over temp, 0.01°/0.03% diff phase/gain	4.25
MAX460	140	1500	5 to 10	100	±15	0.05 to 0.1	FET input, EL2005, LH0033 upgrade	19.78
LH0033	100	1400 to 1500	5 to 20	100	±15	0.1 to 0.5	FET input, improved industry-standard	13.67
LH0063/BB3553	300	2000	25 to 50	200	±15	0.2 to 0.5	FET input, industry-standard	23.51/24.99
VIDEO MULTIPLEXER/AMPLIFIER								
MAX440	160 110($A_V \geq 2$)	370	10	24	±5	2µA	Video amp with 8-channel mux, 0.03°/0.04% diff phase/gain, 15ns switch time, high-Z output state	8.95
MAX441	160 110($A_V \geq 2$)	370	10	24	±5	2µA	Video amp with 4-channel mux, 0.03°/0.04% diff phase/gain, 15ns switch time	5.90
MAX442	160	370	5	24	±5	2µA	Video amp with 4-channel mux, 15ns switch time, 8-pin DIP/SO	4.45
MAX453	50	300	5	14	±5	10	Video amp with 2-channel video mux	3.94
MAX454	50	300	5	14	±5	10	Video amp with 4-channel video mux	5.25
MAX455	50	300	5	14	±5	10	Video amp with 8-channel video mux	8.75

Part Number	Unity GBW (MHz)	Slew Rate (V/µs)	V_{OS} (mV max)	OFF Isolation (dB at 5MHz)	Crosstalk (dB at 5MHz)	Features	Price† 1000-up ($)
VIDEO CROSSPOINT SWITCH							
MAX456	35	250	5	80	70	8x8 crosspoint switch array with 8 output buffers, three-state capability	19.98

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

250MHz Wideband Transconductance Amplifiers

General Description

The MAX435 and MAX436 are high-speed, wideband transconductance amplifiers (WTA) with true differential, high-impedance inputs. The WTA's unique architecture provides accurate gain without feedback, eliminating closed-loop phase shift – a primary cause of circuit oscillation in conventional high-speed amplifiers. The WTA's output is a current proportional to the applied differential input voltage, providing inherent short-circuit protection for the outputs. Circuit gain is set by the ratio of two impedances and an internally set current-gain factor (K).

The absence of feedback allows a 250MHz bandwidth that is independent of the circuit gain, a 700V/µs slew rate, and a 1% settling time of 14ns to a 0.5V step input. With a CMRR of 50dB at 10MHz, the WTA offers exceptional wideband common-mode rejection. 1mV input offset voltage provides a level of DC precision rarely found in high-speed op amps.

Unlike current feedback amplifiers, the MAX435/MAX436 have fully symmetric, high-impedance inputs that tolerate wide differential input voltages without destructive failure or amplifier saturation, virtually eliminating overload recovery time. The WTA's unique performance features are well suited to a wide variety of applications, such as high-speed instrumentation amplifiers and wideband, high-gain bandpass amplifiers. The MAX435's differential output is ideal for high-speed differential line drivers and receivers.

Applications

Differential Line Drivers

Differential Line Receivers

Wideband Instrumentation Amplifiers

High-Speed Filters

High-Speed Bandpass Amplifiers

Features

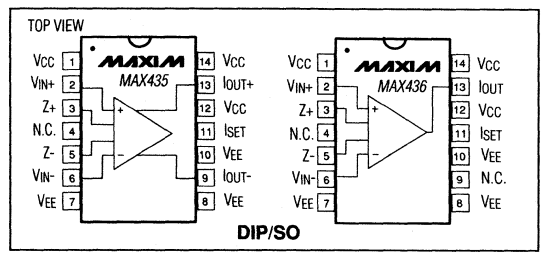
- ♦ **250MHz Bandwidth**
- ♦ **700V/µs Slew Rate**
- ♦ **14ns Settling Time**
- ♦ **50dB CMRR at 10MHz**
- ♦ **Wideband Gain Independent of Bandwidth**
- ♦ **No Feedback**
- ♦ **True Differential High-Impedance Inputs**

Ordering Information

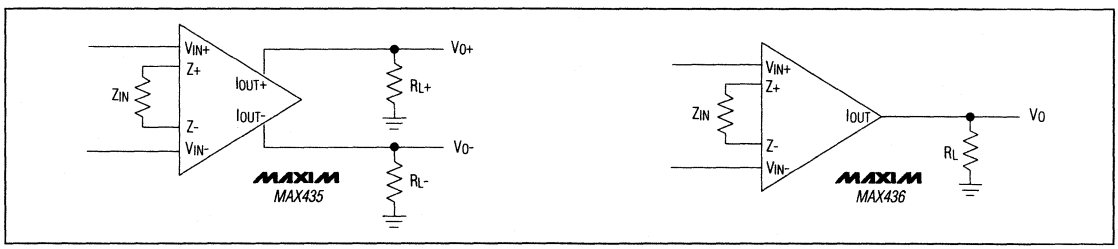
PART	TEMP. RANGE	PIN-PACKAGE
MAX435CPD	0°C to +70°C	14 Plastic DIP
MAX435CSD	0°C to +70°C	14 SO
MAX435C/D	0°C to +70°C	Dice*
MAX435EPD	-40°C to +85°C	14 Plastic DIP
MAX435ESD	-40°C to +85°C	14 SO
MAX435MJD	-55°C to +125°C	14 CERDIP
MAX436CPD	0°C to +70°C	14 Plastic DIP
MAX436CSD	0°C to +70°C	14 SO
MAX436C/D	0°C to +70°C	Dice*
MAX436EPD	-40°C to +85°C	14 Plastic DIP
MAX436ESD	-40°C to +85°C	14 SO
MAX436MJD	-55°C to +125°C	14 CERDIP

** Dice are specified at T_A = +25°C, DC parameters only.*

Pin Configurations



Typical Operating Circuits



19-4701; Rev 0; 3/92

MAXIM

High-Speed Video Multiplexer/Amplifier

General Description

The MAX440 and MAX441 combine a unity-gain stable, wideband video amplifier with a high-speed, 8- or 4-channel multiplexer (mux). The mux's fast 15ns switching time and the amplifier's low differential gain and phase errors (0.04% and 0.03°, respectively) make the MAX440/MAX441 ideal for broadcast-quality video applications. Both devices operate from ±5V power supplies and typically consume only 350mW.

The on-board video amplifier features a 160MHz unity-gain bandwidth, 250V/µs slew rate, and directly drives a 150Ω load to ±3V. Pin-selectable frequency compensation allows the amplifier's AC response to be optimized without external compensation components or complex calculations. Slew rates of 370V/µs are obtainable for applications with a closed-loop gain of 6dB or greater. An enable control on the MAX440 places the amplifier output into a high-impedance state, allowing multiple devices to be paralleled to form larger switch matrices.

The mux's low channel-input capacitance (4pF with channel on or off) maximizes high-speed performance. No input channels are located on adjacent package pins, minimizing crosstalk and simplifying board layout.

Applications

Video Signal Multiplexing

Video Crosspoint Switches

Coaxial-Cable Drivers

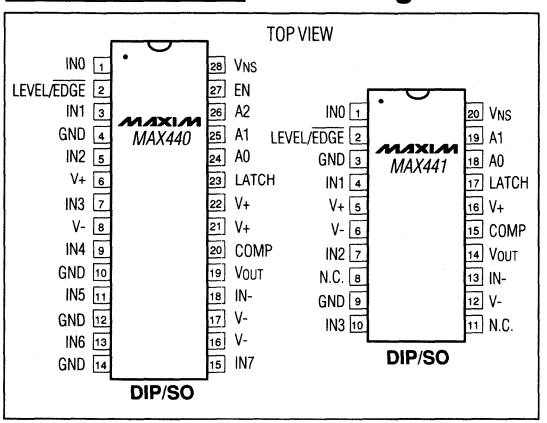
Video Editing

Video Security Systems

Medical Imaging

High-Speed Signal Processing

Pin Configurations



Features

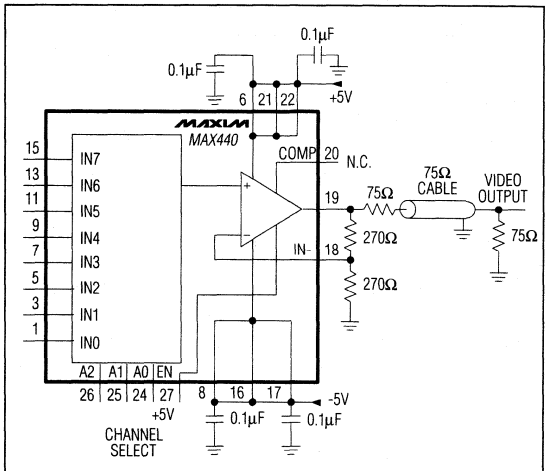
- ♦ **160MHz Unity Gain Bandwidth**
- ♦ **110MHz Bandwidth (A_V = 6dB)**
- ♦ **0.03°/0.04% Differential Phase/Gain Error**
- ♦ **15ns Channel Switch Time**
- ♦ **370V/µs Slew Rate**
- ♦ **Directly Drives 50Ω Cables**
- ♦ **4pF On/Off Input Capacitance**
- ♦ **No External Compensation Components**
- ♦ **Pin-Selectable Frequency Compensation**
- ♦ **Expandable for Larger Switch Matrices**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX440CPI	0°C to +70°C	28 Plastic DIP
MAX440CWI	0°C to +70°C	28 Wide SO
MAX440C/D	0°C to +70°C	Dice*
MAX440EPI	-40°C to +85°C	28 Plastic DIP
MAX440EWI	-40°C to +85°C	28 Wide SO
MAX440MDI	-55°C to +125°C	28 Ceramic SB**
MAX441CPP	0°C to +70°C	20 Plastic DIP
MAX441CWP	0°C to +70°C	20 Wide SO
MAX441EPP	-40°C to +85°C	20 Plastic DIP
MAX441EWP	-40°C to +85°C	20 Wide SO

** Dice are specified at +25°C, DC parameters.*
***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



8

High-Speed Video Multiplexer/Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-) 12V
Analog Input Voltage ..... (V+ + 0.3V) to (V- - 0.3V)
Digital Input Voltage ..... -0.3V to (V+ + 0.3V)
Short-Circuit Current Duration ..... 1 minute
Input Current to Any Pin, Power On or Off ..... ±50mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin Plastic DIP (derate 8.00mW/°C above +70°C) ... 640mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) ... 800mW
28-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) ... 1000mW
28-Pin Ceramic SB (derate 16.67mW/°C above +70°C) . 1333mW

Operating Temperature Ranges:
MAX44_C__ ..... 0°C to +70°C
MAX44_E__ ..... -40°C to +85°C
MAX440MDI ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, V_{NS} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE							
Input Voltage Range	V_{IN}	T_A = T_{MIN} to T_{MAX}		-2		2	V
Input Offset Voltage (All Channels)	V_{OS}	T_A = +25°C			±2.5	±10	mV
		0°C to +70°C				±10	
		-40°C to +85°C				±15	
		-55°C to +125°C				±20	
Input Bias Current (Channel On)	I_B	V_{IN} = 0V	T_A = +25°C		±1	±2	µA
			0°C to +70°C			±5	
			-40°C to +85°C			±5	
			-55°C to +125°C			±20	
Input Leakage Current (Channel Off)	I_{LKG}	V_{IN} = 0V	T_A = +25°C		±0.5	±50	nA
			T_A = T_{MIN} to T_{MAX}			±1	µA
Input Resistance (Channel On)	R_{IN}	-2V ≤ V_{CM} ≤ 2V	T_A = +25°C	0.5	2		MΩ
			T_A = T_{MIN} to T_{MAX}	0.2			
Input Capacitance	C_{IN}	Channel on or off			4		pF
DC Output Resistance	R_{OUT}	A_V = 0dB			25		mΩ
Disabled Output Resistance	R_{OUTdis}	MAX440 only, EN = 0V			130		kΩ
Disabled Output Capacitance	C_{OUTdis}	MAX440 only, EN = 0V			15		pF
Open-Loop Voltage Gain	A_{VOL}	R_L = 75Ω, -2V ≤ V_{OUT} ≤ +2V	T_A = +25°C	50	60		dB
			T_A = T_{MIN} to T_{MAX}	46			
Common-Mode Rejection Ratio	CMRR	-2V ≤ V_{IN} ≤ +2V	T_A = +25°C	46	50		dB
			T_A = T_{MIN} to T_{MAX}	40			
Power-Supply Rejection Ratio	PSRR	±4.75V to ±5.25V	T_A = +25°C	54	80		dB
			T_A = T_{MIN} to T_{MAX}	54			
Output Voltage Swing	V_{OUT}	T_A = +25°C		±3			V
		T_A = T_{MIN} to T_{MAX}		±2			

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, V_{NS} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

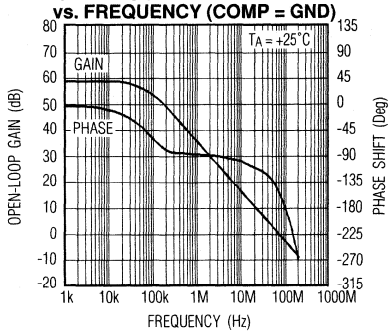
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
-3dB Bandwidth	BW1	A_V = 0dB, COMP = GND, R_L = 75Ω			160		MHz
	BW2	A_V = 6dB, COMP = OPEN, R_L = 150Ω			110		
Slew Rate	SR1	A_V = 0dB, COMP = GND, R_L = 75Ω			250		V/µs
	SR2	A_V = 6dB, COMP = OPEN, R_L = 150Ω			370		
Differential Phase Error (Note 1)	DP	V_{NS} = -2.5V to -5V, COMP = OPEN, A_V = 6dB, R_L = 150Ω			0.03		deg
Differential Gain Error (Note 1)	DG	V_{NS} = -2.5V to -5V, COMP = OPEN, A_V = 6dB, R_L = 150Ω			0.04		%
Settling Time	t_S	To 0.1% of final value, A_V = 6dB, COMP = OPEN, 1V step input			65		ns
Adjacent Channel Crosstalk (Note 2)	X_{TALK}	f = 10MHz, R_S = 75Ω, A_V = 0dB	MAX440		-66		dB
			MAX441		-70		
Non-Adjacent Channel Crosstalk (Note 2)	X_{TALK}	f = 10MHz, R_S = 75Ω, A_V = 0dB			-77		dB
Feedthrough with Amplifier Disabled (Note 2)	FT	MAX440 only, f = 10MHz, A_V = 0dB	CH0 -CH6 driven		-71		dB
			CH0 -CH7 driven		-63		
Input Noise-Voltage Density	e_n	f = 10kHz			12		nV/√Hz
POWER-SUPPLY REQUIREMENTS							
Operating Supply-Voltage Range	V_S			±4.75		±5.25	V
Positve Supply Current	I_{CC}	V_{IN} = 0V	T_A = +25°C	33	40	50	mA
			0°C to +70°C	30		52	
			-40°C to +85°C	27		54	
			-55°C to +125°C	27		54	
Negative Supply Current	I_{EE}	V_{IN} = 0V	T_A = +25°C	24	30	40	mA
			0°C to +70°C	20		42	
			-40°C to +85°C	17		44	
			-55°C to +125°C	17		44	
SWITCHING CHARACTERISTICS (see Figure 10)							
Logic Low Threshold	V_{IL}	T_A = T_{MIN} to T_{MAX}				0.8	V
Logic High Threshold	V_{IH}	T_A = T_{MIN} to T_{MAX}		2.4			V
Address Setup Time (Note 3)	t_{AS}					10	ns
Address Hold Time (Note 3)	t_{AH}					10	ns
Address Propagation Delay	t_{APD}				20		ns
Latch Propagation Delay	t_{LPD}				20		ns
Channel Switching Time (Note 4)	t_{SW}	V_{NS} = -2.5V			15		ns
		V_{NS} = -5V			25		ns
Enable Propagation Delay	t_{ENPD}	MAX440 only			15		ns
Output Disable Time	t_{DA}	MAX440 only			10		ns
Output Enable Time	t_{EN}	MAX440 only			40		ns
Switching Transient (Note 5)		R_L = 75Ω	V_{NS} = -2.5V		100		mV_{p-p}
			V_{NS} = -5V		800		

Note 1: Input test signal: 3.58MHz sine wave of amplitude 40IRE superimposed on a linear ramp (0IRE to 100IRE). IRE is a unit of video signal amplitude developed by the International Radio Engineers. 140IRE = 1.0V.
Note 2: See Figure 9, *Dynamic Test Circuits.*
Note 3: Guaranteed by design.
Note 4: Channel switching time specified for switching between 2 grounded input channels; does not include signal rise/fall times for switching between channels with different input voltages.
Note 5: Measured while switching between 2 grounded channels.

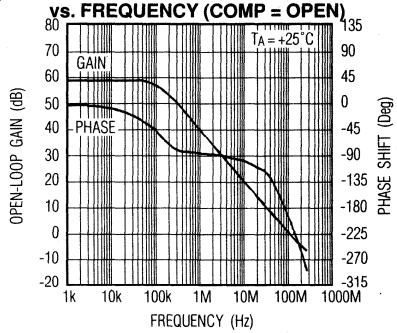
High-Speed Video Multiplexer/Amplifier

Typical Operating Characteristics

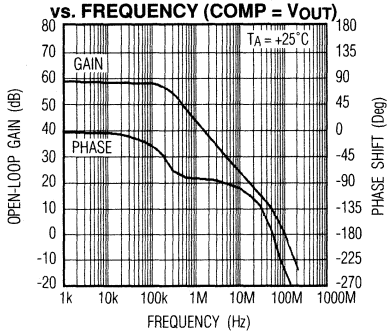
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (COMP = GND)



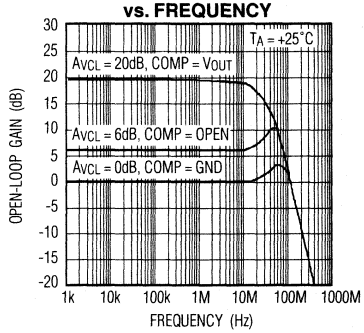
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (COMP = OPEN)



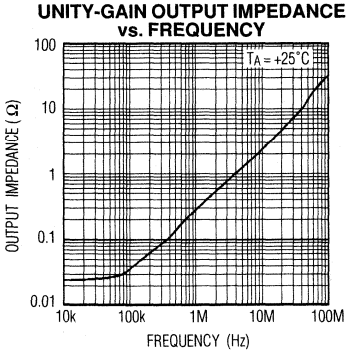
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (COMP = VOUT)



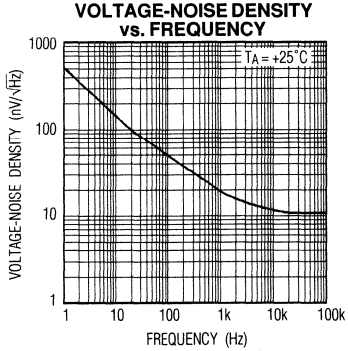
CLOSED-LOOP GAIN vs. FREQUENCY



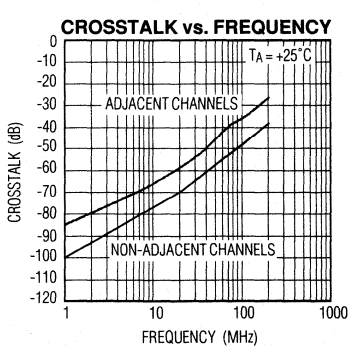
UNITY-GAIN OUTPUT IMPEDANCE vs. FREQUENCY



VOLTAGE-NOISE DENSITY vs. FREQUENCY

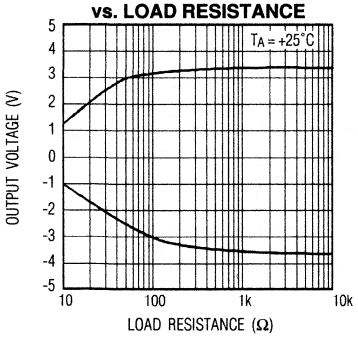


CROSSTALK vs. FREQUENCY

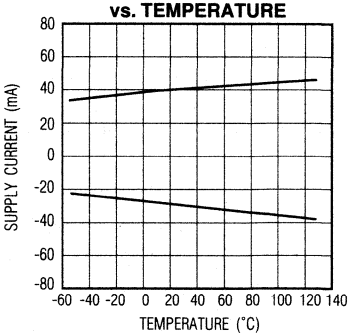


Typical Operating Characteristics (continued)

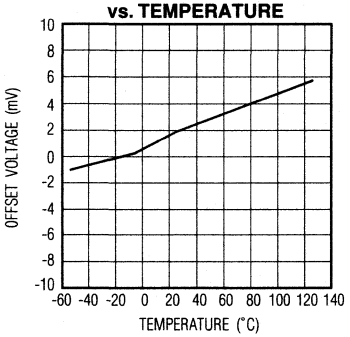
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



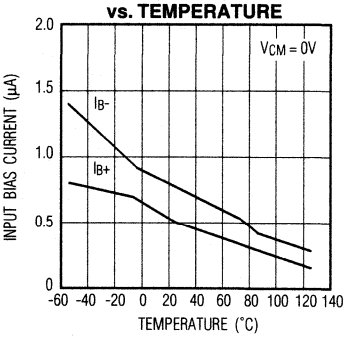
SUPPLY CURRENT vs. TEMPERATURE



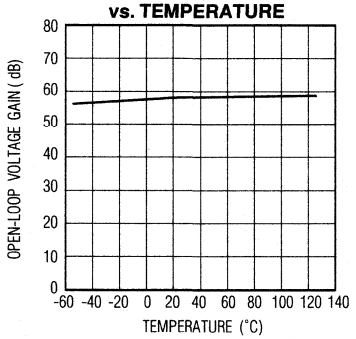
INPUT OFFSET VOLTAGE vs. TEMPERATURE



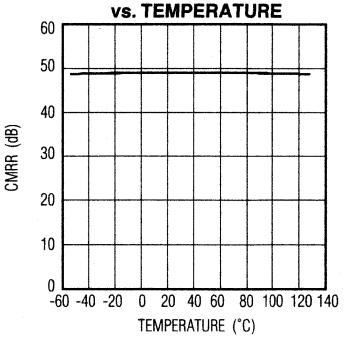
INPUT BIAS CURRENT vs. TEMPERATURE



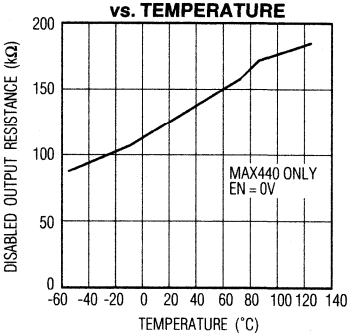
OPEN-LOOP VOLTAGE GAIN vs. TEMPERATURE



COMMON-MODE REJECTION RATIO vs. TEMPERATURE



DISABLED OUTPUT RESISTANCE vs. TEMPERATURE



High-Speed Video Multiplexer/Amplifier

Pin Description

PIN		NAME	FUNCTION
MAX440	MAX441		
1	1	IN0	Analog Input, Channel 0
2	2	LEVEL/$\overline{\text{EDGE}}$	Digital input that controls the operation of LATCH input as follows: When LEVEL/$\overline{\text{EDGE}}$ = 0V, input data is latched on the rising edge of the LATCH input (edge triggered); when LEVEL/$\overline{\text{EDGE}}$ = 5V, input data is latched when LATCH = 5V (level triggered). Hardwire to +5V or GND for improved crosstalk.
3	4	IN1	Analog Input, Channel 1
4, 10, 12, 14	3, 9	GND	Ground
5	7	IN2	Analog Input, Channel 2
6, 21, 22	5, 16	V+	Positive Power Supply, +5V
7	10	IN3	Analog Input, Channel 3
8, 16, 17	6, 12	V-	Negative Power Supply, -5V
9	–	IN4	Analog Input, Channel 4
11	–	IN5	Analog Input, Channel 5
13	–	IN6	Analog Input, Channel 6
15	–	IN7	Analog Input, Channel 7
18	13	IN-	Amplifier Inverting Input
19	14	V_{OUT}	Amplifier Output
20	15	COMP	Amplifier Compensation Input. Ground for unity-gain application, or use to adjust compensation for higher-gain applications (see text).
23	17	LATCH	Latch control for digital inputs. If LEVEL/$\overline{\text{EDGE}}$ = 0V, data is latched on the rising edge of LATCH. If LEVEL/$\overline{\text{EDGE}}$ = 5V, the input register is transparent when LATCH = 0V and latched when LATCH = 5V.
24	18	A0	Channel Address Input 0, LSB
25	19	A1	Channel Address Input 1, MSB for MAX441
26	–	A2	Channel Address Input 2, MSB
27	–	EN	Amplifier Output Enable control, active high. This is internally latched, along with A0 to A2.
28	20	V_{NS}	Normally -5V, minimize switching time and transients by tying this pin to -2.5V. Analog input voltage must never be more negative than the voltage on this pin.
–	8, 11	N.C.	No Internal Connection

Applications Information

The MAX440/MAX441 are wideband, monolithic video multiplexer/amplifiers with 8 and 4 input channels, respectively. The output amplifier is used in the noninverting configuration and features pin-selectable frequency compensation.

The MAX440/MAX441's bipolar construction results in a typical channel input capacitance of only 4pF, whether the channel is on or off. The mux's input capacitance forms a single-pole RC lowpass filter with the output impedance of the signal source. This filter can limit the system's signal bandwidth if the RC product becomes too large. The MAX440/MAX441's low-channel input capacitance allows the amplifier's full AC performance to be realized, even with source impedances as great as 250Ω.

Feedback resistors should be limited to no more than 500Ω to ensure that the RC time constant formed by the resistors, the circuit board's capacitance, and the capacitance of the amplifier input pins does not limit the system's high-speed performance.

Power-Supply Bypassing and Board Layout

Realizing the full potential AC performance of high-speed amplifiers requires careful attention to power-supply bypassing and board layout. Use a large, low-impedance ground plane with the MAX440/MAX441. With multi-layer boards, the ground plane should be located on the PC board's component side to minimize impedance between the components and the ground plane. For single-layer printed circuit (PC) boards, components should be mounted on the board's copper side and the ground plane should include the entire portion of the PC board that is not dedicated to a specific signal trace.

To prevent oscillation and unwanted signal coupling, minimize trace area at critical high-impedance nodes of the circuit, especially the amplifier summing junction. These critical nodes should also be surrounded by a ground trace. Ground traces should be included between all signal traces to minimize parasitic coupling that can degrade crosstalk and/or stability of the amplifier. Signal paths should be kept as short as possible to minimize inductance, and all input channel traces should be of equal length to maintain the phase relationship between the input channels.

All power-supply pins should be bypassed directly to the ground plane with 0.1µF ceramic capacitors, placed as close to the supply pins as possible. For high-current loads, it may be necessary to include 1µF tantalum or aluminum electrolytic capacitors in parallel with the 0.1µF ceramics. Capacitor lead lengths should be kept as

short as possible to minimize series inductance; surface-mount (chip) capacitors are ideal for this application.

Frequency Compensation

Three different frequency compensation modes are available for the MAX440/MAX441. The compensation is determined by the closed-loop gain of the application circuit and is selected by the state of the COMP pin as shown in Table 1. For closed-loop gains below 6dB, the COMP pin should be tied to ground to ensure sufficient phase margin for stable circuit operation.

Table 1. COMP Pin State vs. Closed-Loop Gain

Closed-Loop Gain		COMP Pin State
V/V	dB	
$1 \le A_{VCL} \le 2$	$0 \le A_{VCL} \le 6$	GND
$2 \le A_{VCL} \le 10$	$6 \le A_{VCL} \le 20$	OPEN
$A_{VCL} \ge 10$	$A_{VCL} \ge 20$	V_{OUT}

For closed-loop voltage gains from 6dB up to 20dB, the COMP pin should be left open to maximize the amplifier's AC performance (slew rate, bandwidth, differential gain and phase errors). The COMP pin can also be grounded to increase phase margin for minimizing overshoot and/or ringing of the output pulse response or for driving capacitive loads. The amplifier's AC performance will be slightly degraded if COMP is grounded.

For applications with closed-loop voltage gains of 20dB or more, the COMP pin should be tied to the amplifier output to obtain the maximum high-speed response from the amplifier. Phase margin can be progressively increased by leaving the COMP pin open or tying it to ground.

Plots of the open-loop gain and phase response for the three different compensation modes are shown in the *Typical Operating Characteristics* section. Closed-loop gain plots are also included for each of the three compensation modes at a typical operating closed- loop gain (COMP = GND, A_{VCL} = 0dB; COMP = OPEN, A_{VCL} = 6dB; and COMP = V_{OUT}, A_{VCL} = 20dB).

Figure 1 shows photographs of the amplifier's large-signal pulse response for each of the three compensation modes. In each of these photographs, the MAX440/MAX441 is driving a back-terminated 50Ω cable, so the output amplitude shown at the end of the cable is attenuated by 6dB from the amplifier output.

Differential Gain and Phase Errors

In color-video applications, differential gain and phase errors are critical specifications for an amplifier, because these errors directly correspond to changes in the contrast and color of the displayed picture. The MAX440/MAX441 have a differential gain error of 0.04% and a differential phase error of 0.03°, making them ideal for use in broadcast-quality color-video systems.

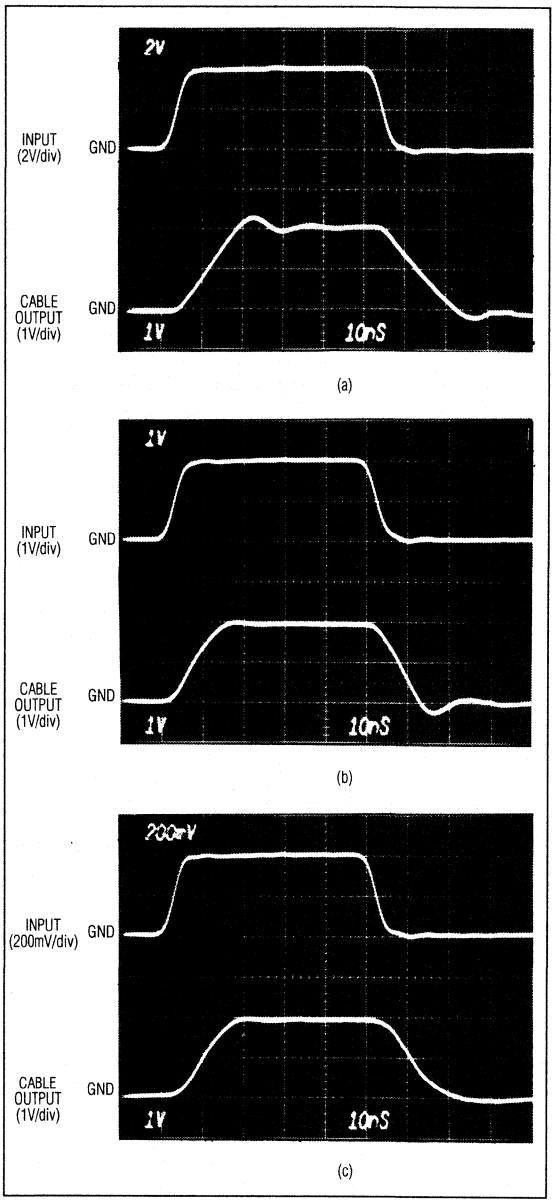


Figure 1. (a) Pulse response with R_L = 100Ω (50Ω back-terminated cable), A_{VCL} = +1V/V , and COMP = GND; (b) Pulse response with R_L = 100Ω (50Ω back-terminated cable), A_{VCL} = +2V/V, and COMP = OPEN; (c) Pulse response with R_L = 100Ω (50Ω back-terminated cable) A_{VCL} = +10V/V, and COMP = V_{OUT}.

8

High-Speed Video Multiplexer/Amplifier

The MAX440/MAX441's differential gain and phase error are measured with the Tektronix VM700 Video Measurement Set, with the input test signal provided by the Tektronix 1910 Digital Generator. Figure 2 shows the test circuit used. The level of differential gain and phase error will vary slightly with the voltage applied at the V_{NS} pin, as shown in Table 2.

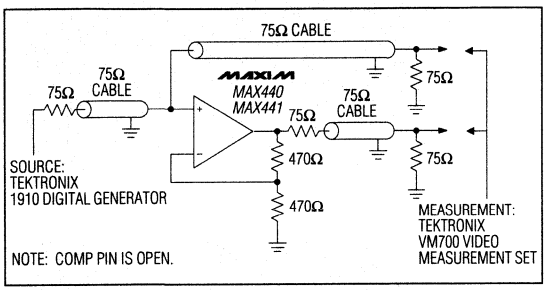


Figure 2. Differential Gain and Phase Error Test Circuit

Table 2. Differential Gain and Phase Error vs. V_{NS} Voltage

V_{NS} VOLTAGE (V)	DIFFERENTIAL GAIN ERROR (%)	DIFFERENTIAL PHASE ERROR (°)
-1.0	0.05	0.04
-1.5	0.04	0.04
-2.0	0.04	0.03
-2.5	0.04	0.03
-5.0	0.04	0.03

Coaxial-Cable Drivers

High-speed performance and excellent output current capability make the MAX440/MAX441 ideal for driving 50Ω or 75Ω coaxial cables. The MAX440/MAX441 will drive a 150Ω load (75Ω back-terminated cable) to ±3V.

Figure 3 shows a MAX440 driving a back-terminated 75Ω video cable. The back-termination resistor (at the MAX440 output) is included to match the impedance at each end of the cable to the characteristic impedance of the cable itself. This practice eliminates signal reflections at the end of the cable. The back-termination resistor forms a voltage divider with the load impedance, which attenuates the signal at the cable output by one-half. The amplifier is operated with a 2V/V closed-loop gain to provide unity gain at the cable's output. The photograph in Figure 1b shows the large-signal pulse response of the MAX440 when driving a back-terminated 50Ω cable, with a 2V/V closed-loop gain and the COMP pin left open.

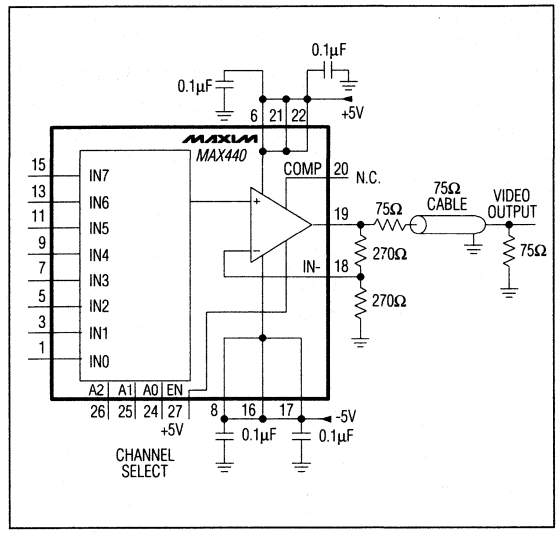


Figure 3. Coaxial-Cable Driver

Capacitive-Load Driving

Driving large capacitive loads increases the likelihood of oscillation in most amplifier circuits. This is especially true for circuits with high loop-gains, like voltage followers. The amplifier's output impedance and the capacitive load form an RC filter that adds a pole to the loop response. If the pole frequency is low enough, as when driving a large capacitive load, the circuit phase margin is degraded and oscillation may occur.

The MAX440/MAX441 phase margin and capacitive-load driving performance is optimized when the amplifier is fully compensated internally. This is accomplished by connecting the COMP pin to circuit ground. When driving large (>50pF) capacitive loads in voltage-follower circuits, an isolation resistor should be added between the amplifier output and the capacitive load, as shown in Figure 4.

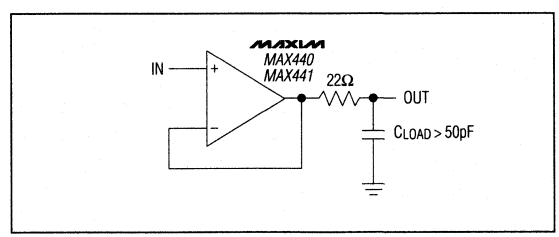


Figure 4. Capacitive-Load Driving Circuit

For improved capacitive-load driving performance without the series isolation resistor, the MAX440/MAX441 should be operated with a closed-loop gain of 6dB (+2V/V) or greater, and the COMP pin should be grounded.

Digital Interface

The multiplexer architecture ensures that no two input channels are ever connected together. Channel selection is performed by applying a binary code to the address inputs A0, A1, and A2 (A0 and A1 only for MAX441). The address decoder selects input channels, as shown in Table 3. All digital inputs are compatible with TTL and CMOS logic levels.

Table 3. Channel Selection

MAX440					MAX441		
EN	A2	A1	A0	SELECTED CHANNEL	A1	A0	SELECTED CHANNEL
0	X	X	X	High-Z-Output	0	0	0
1	0	0	0	0	0	1	1
1	0	0	1	1	1	0	2
1	0	1	0	2	1	1	3
1	0	1	1	3			
1	1	0	0	4			
1	1	0	1	5			
1	1	1	0	6			
1	1	1	1	7			

An address latch, which retains channel selection data while the data bus is used for other purposes, is provided on the MAX440/MAX441. The latch is in either an edge-triggered mode or a level-triggered mode, depending on the state of the LEVEL/$\overline{\text{EDGE}}$ control input. If LEVEL/$\overline{\text{EDGE}}$ is low, the latch operates in edge-triggered mode, with the latch occuring on the rising edge of the LATCH input. If LEVEL/$\overline{\text{EDGE}}$ is high, then the latch operates in level-triggered mode and input data is latched when LATCH is high. If LEVEL/$\overline{\text{EDGE}}$ is high and LATCH is low, the input register is transparent.

Channel Switching Time and Transient

When switching between input channels, the transient voltage at the output of the MAX440/MAX441 depends on the voltage level at the V_{NS} pin. The voltage at this pin should lie within the -1V to -5V range, and is adjusted using Figure 5's circuit. **Note: The input voltage must never be allowed to be more negative than the voltage at V_{NS}.**

The switching transient's magnitude and the channel switching time both increase as the V_{NS} voltage gets more negative. The photos in Figures 6 and 7 illustrate this phenomenon. In Figure 6, the V_{NS} voltage is -2.5V, and the switching transient peak level is 100mV$_{p-p}$. In Figure 7, with V_{NS} at -5V, the switching transient is about 800mV$_{p-p}$. The typical channel switching time increases from 15ns to 25ns as the V_{NS} voltage decreases from

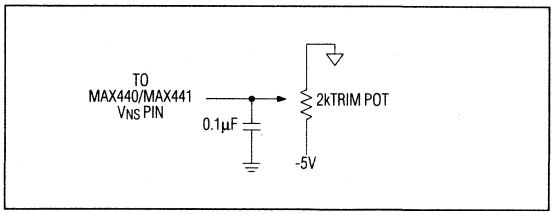


Figure 5. V_{NS} Pin-Voltage Adjustment

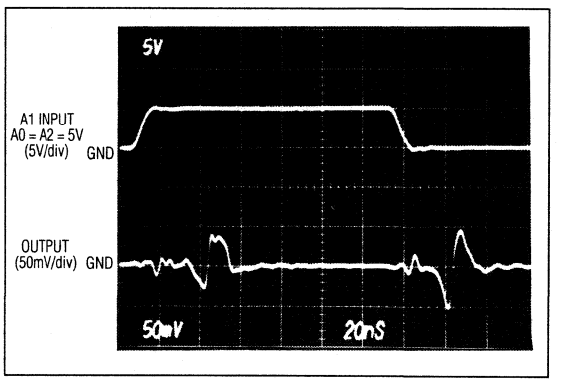


Figure 6. Output Transient When Switching Between Two Grounded Inputs with R_L = 75Ω and V_{NS} = -2.5V

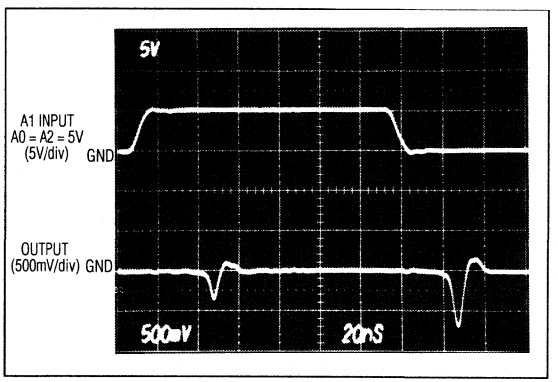


Figure 7. Output Transient When Switching Between Two Grounded Inputs with R_L = 75Ω and V_{NS} = -5.0V

High-Speed Video Multiplexer/Amplifier

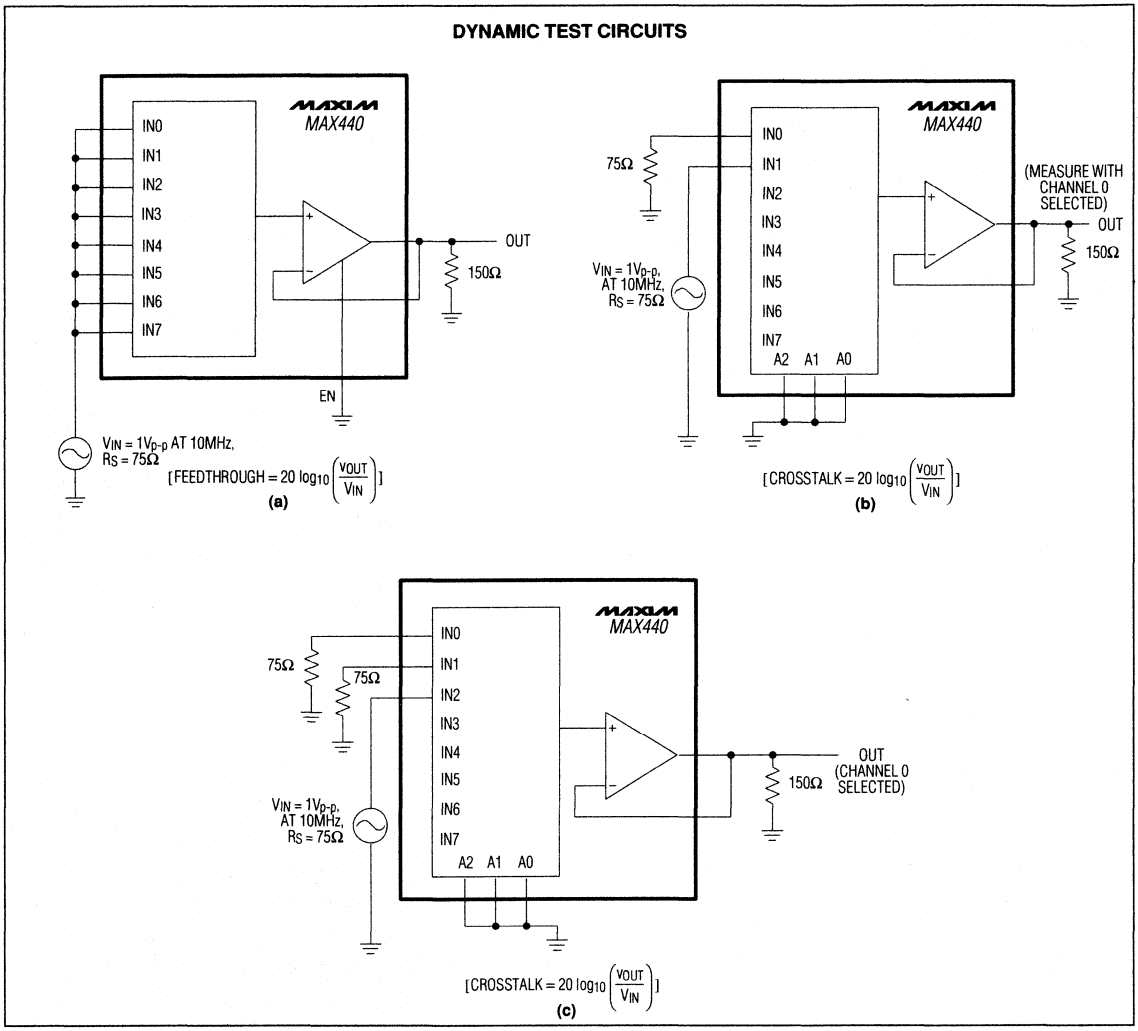


Figure 8. (a) Disabled Amplifier Feedthrough; (b) Adjacent Channel Crosstalk; (c) Non-Adjacent Channel Crosstalk

-2.5V to -5V. Figure 10 shows the MAX440/MAX441 timing diagram.

Output Disable (MAX440 Only)

The EN pin is provided on the MAX440 to enable the amplifier output when driven to a TTL high state. When EN is driven low, the MAX440's output becomes a high-impedance load with a 130kΩ typical resistance and a 15pF typical capacitance. When disabled, the signal feedthrough from the mux inputs to the amplifier output is -63db at 10MHz, with all 8 input channels driven with a $1V_{p-p}$ sine wave and a 150Ω load impedance. Figure 8a shows the test circuit used to measure feedthrough.

The output disable capability allows several MAX440s to be paralleled to form larger switch matrices, by tying the outputs together and disabling all but one of the paralleled amplifier outputs. Figure 9 shows the 1-of-16 video mux/amp circuit that uses this feature. In this example, the EN inputs of the MAX440s are used as a 4th address

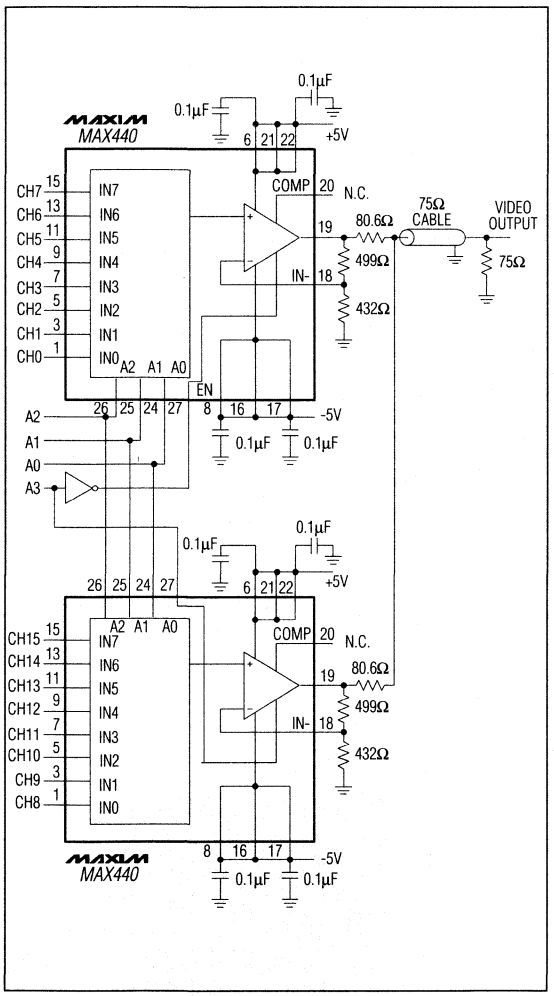


Figure 9. 1-of-16 Video Multiplexer

Table 4. 1-of-16 Video Mux/Amp Channel Selection

A3	A2	A1	A0	SELECTED CHANNEL
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

bit (A3), with an inverter added to ensure the amplifiers are not simultaneously enabled. The amplifier outputs are connected after the back-termination resistors, so that the active amplifier output is isolated from the capacitive load (15pF typ) presented by the inactive output of the second MAX440. This will minimize ringing in the output signal.

The disabled amplifier's back-termination and gain resistors form a voltage divider with the back-termination resistor at the active amplifier's output. The amplifier closed-loop gains have been set slightly greater than 6dB to compensate for the signal attenuation caused by this divider. The value of the back-termination resistors has been increased to 80.6Ω so the parallel combination of the resistors at the cable's input equals 75Ω.

With proper selection of resistor values, this configuration can be expanded to form larger switch matrices. The number of paralled devices is limited primarily by the MAX440's disabled feedthrough. Table 4 shows the relationship between the digital input code and the selected output channel for Figure 9's circuit.

High-Speed Video Multiplexer/Amplifier

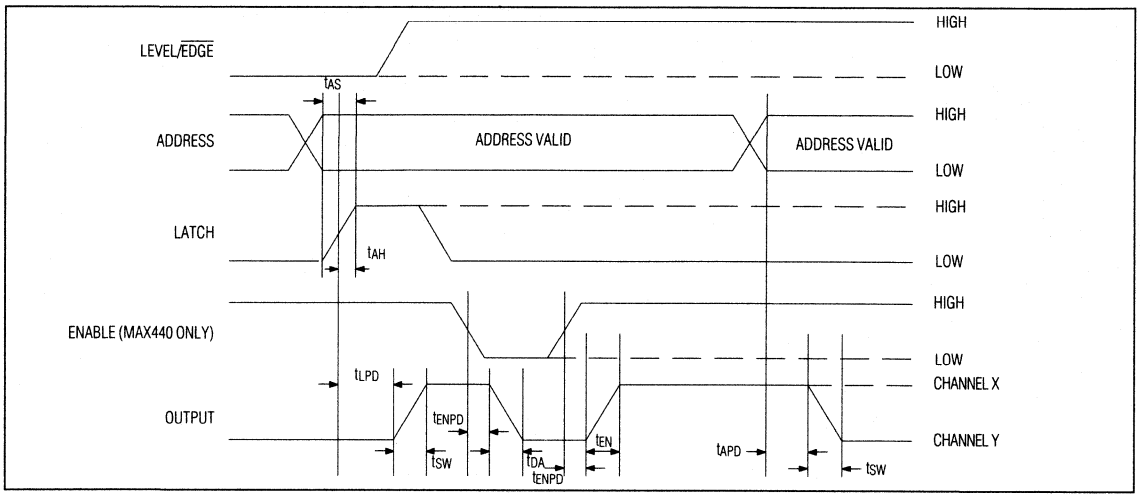
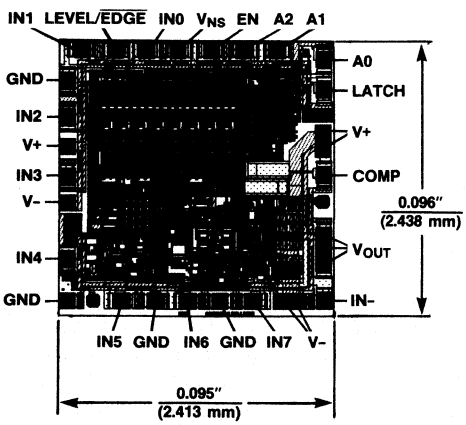


Figure 10. MAX440/MAX441 Timing Diagram

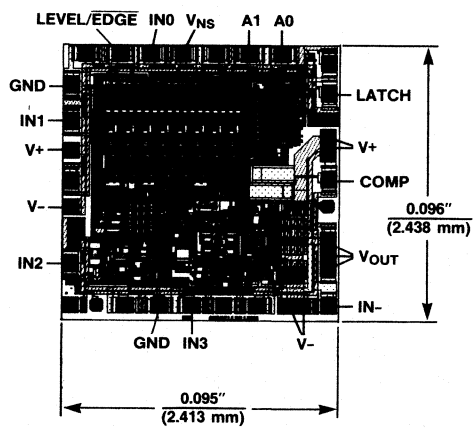
Chip Topographies

MAX440



TRANSISTOR COUNT: 564

MAX441



TRANSISTOR COUNT: 564

19-0016; Rev 0; 6/92

MAXIM

140MHz, 2-Channel, Video Multiplexer/Amplifier

General Description

The MAX442 combines a 140MHz video amplifier with a high-speed, 2-channel multiplexer in an 8-pin package. The MAX442 is ideal for broadcast-quality video applications, with 36ns switching speed and low differential gain (0.07%) and phase (0.09°) errors. The device is designed to drive both 50Ω and 75Ω cables, and can directly drive a 75Ω load to ±3V.

The MAX442 video amplifier is compensated for unity-gain stability, and features 140MHz bandwidth and 250V/µs slew rate. The multiplexer's low input capacitance (4pF with the channel on or off) maximizes high-speed performance, and a ground pin separating the two input channels minimizes crosstalk and simplifies board layout.

The device operates from 5V supplies and typically consumes 300mW.

For 2-channel applications that require greater slew rate and wider bandwidth at closed-loop gains of 2 or greater (≥6dB), see the MAX443 data sheet. For applications that require more input channels, see the data sheet for the MAX440 8-channel mux/amp and the MAX441 4-channel mux/amp.

Applications

Broadcast-Quality Video-Signal Multiplexing

Coaxial-Cable Drivers

Video Editing

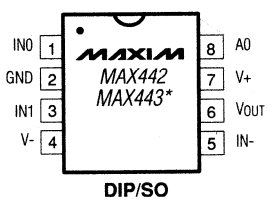
Video Security Systems

Medical Imaging

High-Speed Signal Processing

Pin Configuration

TOP VIEW



DIP/SO

** Contact factory for availability*

Features

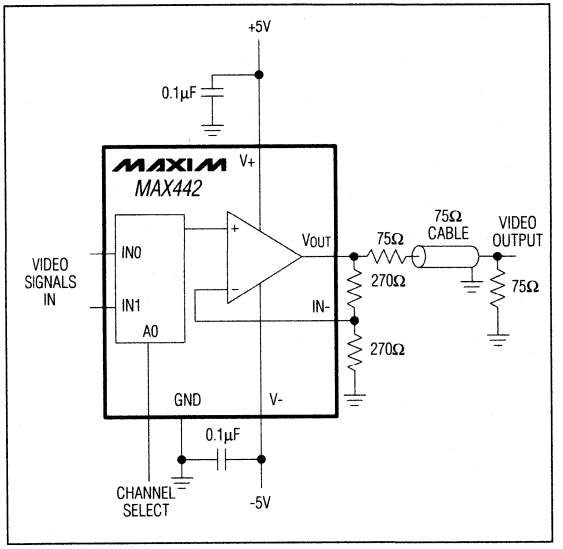
- ♦ **140MHz Unity-Gain Bandwidth**
- ♦ **250V/µs Slew Rate**
- ♦ **0.07%/0.09° Differential Gain/Phase Error**
- ♦ **36ns Channel Switch Time**
- ♦ **No External Compensation Components**
- ♦ **8-Pin DIP and SO Packages**
- ♦ **Directly Drives 50Ω and 75Ω Cables**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX442CPA	0°C to +70°C	8 Plastic DIP
MAX442CSA	0°C to +70°C	8 SO
MAX442C/D	0°C to +70°C	Dice*
MAX442EPA	-40°C to +85°C	8 Plastic DIP
MAX442ESA	-40°C to +85°C	8 SO

** Dice are specified at T_A = +25°C, DC parameters only.*

Typical Operating Circuit



8

140MHz, 2-Channel, Video Multiplexer/Amplifier

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-) 12V
Analog Input Voltage ..... (V+ + 0.3V) to (V- - 0.3V)
Digital Input Voltage ..... -0.3V to (V+ + 0.3V)
Short-Circuit Current Duration ..... 1 minute
Input Current to Any Pin, Power On or Off ..... ±50mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Ranges:
MAX442C_ _ ..... 0°C to +70°C
MAX442E_ _ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5V, V- = -5V, R_L = 150Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE							
Input Voltage Range	V_{IN}			-2		2	V
Input Offset Voltage (All Channels)	V_{OS}	T_A = +25°C			±1.5	±7.0	mV
		MAX442C				±10	
		MAX442E				±12	
Offset Matching (V_{OS0} - V_{OS1})		T_A = +25°C			±1.0	±2.5	mV
		T_A = T_{MIN} to T_{MAX}				±5.0	
Input Bias Current (Channel On)	I_B	V_{IN} = 0V	T_A = +25°C		±1	±2	µA
			T_A = T_{MIN} to T_{MAX}			±5	
Input Leakage Current (Channel Off)	I_{LKG}	V_{IN} = 0V	T_A = +25°C		±0.5	±50	nA
			T_A = T_{MIN} to T_{MAX}			±1	µA
Input Resistance (Channel On) (Note 1)	R_{IN}	-2V ≤ V_{CM} ≤ 2V	T_A = +25°C	0.5	2.0		MΩ
			T_A = T_{MIN} to T_{MAX}	0.2			
Input Capacitance	C_{IN}	Channel on or off			4		pF
DC Output Resistance	R_{OUT}	A_V = 0dB			25		mΩ
		A_V = 6dB			50		
Open-Loop Voltage Gain	A_{VOL}	R_L = 75Ω, -2V ≤ V_{OUT} ≤ +2V	T_A = +25°C	50	60		dB
			T_A = T_{MIN} to T_{MAX}	46			
Common-Mode Rejection Ratio	CMRR	-2V ≤ V_{IN} ≤ +2V	T_A = +25°C	46	50		dB
			T_A = T_{MIN} to T_{MAX}	46			
Power-Supply Rejection Ratio	PSRR	±4.75V to ±5.25V	T_A = +25°C	54	80		dB
			T_A = T_{MIN} to T_{MAX}	54			
Output Voltage Swing	V_{OUT}	R_L = 75Ω	T_A = +25°C	±2.5	±3.0		V
			T_A = T_{MIN} to T_{MAX}	±2.0			

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5V, V- = -5V, R_L = 150Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
-3dB Bandwidth	BW	A_V = 0dB, R_L = 100Ω			140		MHz
Slew Rate	SR1				250		V/µs
Differential Phase Error	DP				0.09		deg
Differential Gain Error	DG				0.07		%
Settling Time	t_S	To 0.1% of final value, A_V = 0dB, R_L = 150Ω, 2V step input			50		ns
Crosstalk	X_{TALK}	f = 10MHz, R_S = 75Ω, A_V = 0dB			76		dB
Input Noise-Voltage Density	e_n	f = 10kHz			12		nV/√Hz
POWER REQUIREMENTS							
Operating Supply-Voltage Range	V_S			±4.75		±5.25	V
Positve Supply Current	I_{CC}	V_{IN} = 0V	T_A = +25°C	25	30	35	mA
			MAX442C	22		38	
			MAX442E	19		41	
Negative Supply Current	I_{EE}	V_{IN} = 0V	T_A = +25°C	23	28	35	mA
			MAX442C	20		38	
			MAX442E	17		41	
SWITCHING CHARACTERISTICS							
Logic Low Threshold	V_{IL}					0.8	V
Logic High Threshold	V_{IH}			2.4			V
Address Propagation Delay	t_{APD}				24		ns
Channel Switching Time	t_{SW}				36		ns

Note 1: Incremental resistance for a common-mode voltage between ±2V.

Pin Description

PIN	NAME	FUNCTION
1	IN0	Analog Input, channel 0
2	GND	Ground
3	IN1	Analog Input, channel 1
4	V-	Negative Power Supply, -5V
5	IN-	Amplifier Inverting Input
6	V_{OUT}	Amplifier Output
7	V+	Positive Power Supply, +5V
8	A0	Channel Address Input: A0 = logic 0 selects channel 0, A0 = logic 1 selects channel 1

140MHz, 2-Channel, Video Multiplexer/Amplifier

Applications Information

The MAX442's bipolar construction results in a typical channel input capacitance of only 4pF, whether the channel is on or off. As with all ICs, the mux's input capacitance forms a single-pole RC lowpass filter with the signal-source's output impedance. This filter can limit the system's signal bandwidth if the RC product becomes too large. However, the MAX442's low channel input capacitance allows full AC performance of the amplifier, even with source impedances as great as 250Ω–a significant improvement over common mux or switch alternatives.

Feedback resistors should be limited to no more than 500Ω to ensure that the RC time constant formed by the resistors, the circuit board's capacitance, and the capacitance of the amplifier input pins does not limit the system's high-speed performance.

Power-Supply Bypassing and Board Layout

Realizing the full AC performance of high-speed amplifiers requires careful attention to power-supply bypassing and board layout. Use a low-impedance ground plane with the MAX442. With multilayer boards, the ground plane should be located on the PC board's component side to minimize impedance between the components and the ground plane. For single-layer boards, components should be mounted on the board's copper side and the ground plane should include the entire portion of the board that is not dedicated to a specific signal trace.

To prevent oscillation and unwanted signal coupling, minimize trace area at the circuit's critical high-impedance nodes, especially the amplifier summing junction (the amplifier's inverting input). Surround these critical nodes with a ground trace, and include ground traces between all signal traces to minimize parasitic coupling that can degrade crosstalk and/or amplifier stability. Keep signal paths as short as possible to minimize inductance, and all input channel traces should be of equal length to maintain the phase relationship between the input channels.

Bypass all power-supply pins directly to the ground plane with 0.1µF ceramic capacitors, placed as close to the supply pins as possible. For high-current loads, it may be necessary to include 1µF tantalum or aluminum electrolytic capacitors in parallel with the 0.1µF ceramic bypass capacitors. Keep capacitor lead lengths as short as possible to minimize series inductance; surface-mount (chip) capacitors are ideal for this application.

Differential Gain and Phase Errors

In color video applications, lowest differential gain and phase errors are critical for an IC, because they cause changes in contrast and color of the displayed picture. Typically the MAX442's multiplexer/amplifier combination has a differential gain and phase error of only 0.07% and 0.09° respectively. This low differential gain and phase error makes the MAX442 ideal for use in broadcast-quality color video systems.

Coaxial-Cable Drivers

High-speed performance and excellent output current capability make the MAX442 ideal for driving 50Ω or 75Ω coaxial cables. The MAX442 will drive 50Ω and 75Ω coaxial cables to ±3V

The typical operating circuit shows the MAX442 driving a back-terminated 75Ω video cable. The back-termination resistor (at the MAX442 output) is included to match the impedance of the cable's driven end to the characteristic impedance of the cable itself. This, plus the load-termination resistor, eliminates signal reflections from the cable's ends. The back-termination resistor forms a voltage divider with the load impedance, which attenuates the signal at the cable output by one-half. The amplifier is operated with a 2V/V closed-loop gain to provide unity gain at the cable's video output.

19-2858; Rev. 1; 4/91

MAXIM

8 x 8 Video Crosspoint Switch

General Description

The MAX456 is the first monolithic CMOS 8x8 video crosspoint switch that significantly reduces component count, board space, and cost. The crosspoint switch contains a digitally-controlled matrix of 64 T-switches that connect eight video input signals to any, or all, output channels. Each matrix output connects to eight internal, high-speed (250V/µs), unity gain stable buffers capable of driving 400Ω and 20pF to ±1.3V. For applications requiring increased drive capability, the outputs of the MAX456 can be connected directly to four MAX457 (dual) video amplifiers, which are capable of driving 75Ω loads.

Three-state output capability and internal, programmable active loads make it feasible to parallel multiple MAX456s and form larger switch matrices.

In the 40-pin DIP package, crosstalk (70dB at 5MHz) is minimized, and board area and complexity are simplified by using a straight-through pin out. The analog inputs and outputs are on opposite sides, and each channel is separated by a power-supply line or "quiet" digital logic line.

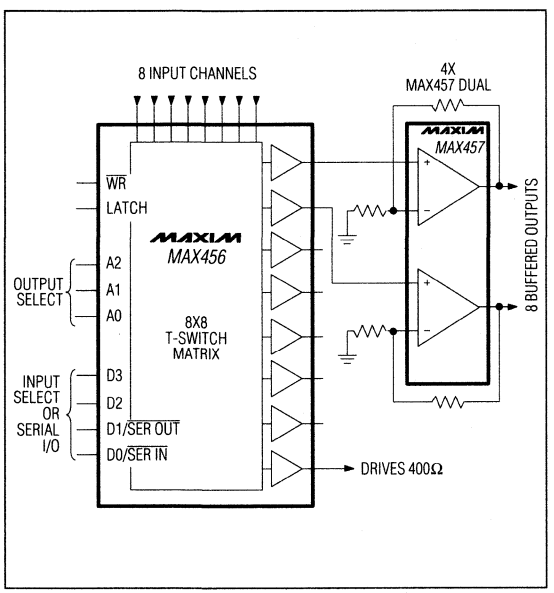
Applications

Video Test Equipment

Video Security Systems

Video Editing

Typical Application



Features

- ♦ **Routes Any Input Channel to Any Output Channel**
- ♦ **Switches Standard Video Signals**
- ♦ **Serial or Parallel Digital Interface**
- ♦ **Expandable for Larger Switch Matrices**
- ♦ **80dB All-Channel Off Isolation at 5MHz**
- ♦ **Eight Internal Buffers with: 250V/µs Slew Rate, Three-State Output Capability, Power-Saving Disable Feature, 35MHz Bandwidth**

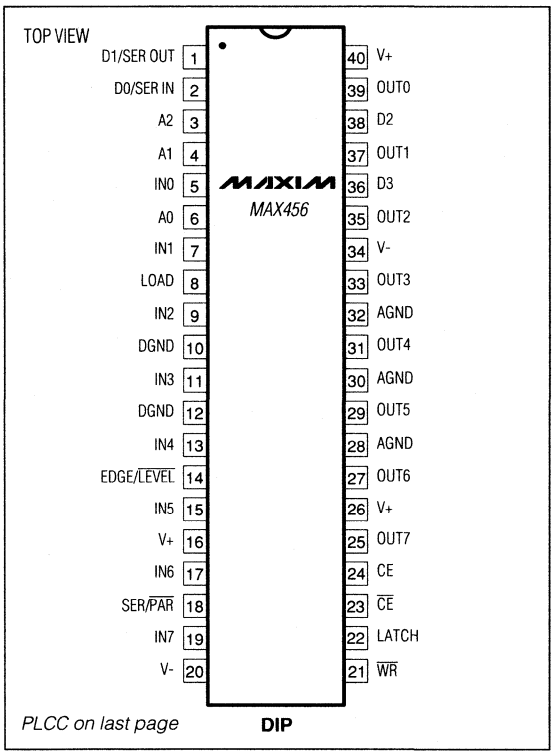
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX456CPL	0°C to +70°C	40 Plastic DIP
MAX456CQH	0°C to +70°C	44 PLCC
MAX456C/D	0°C to +70°C	Dice*

** Dice electrical characteristics are specified at T_A = 25°C only.*

Ordering Information continued on last page

Pin Configurations



PLCC on last page

8 x 8 Video Crosspoint Switch

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V+ to V-) 12V
Positive Supply Voltage V+ referred to AGND . . . . . +12V
Negative Supply Voltage V- referred to AGND . . . . . -12V
DGND Voltage . . . . . AGND ±0.3V
Buffer Short Circuit to Ground,
when not exceeding package power dissipation . . . Indefinite
Analog Input Voltage . . . . . (V+) +0.3V to (V-) -0.3V
Digital Input Voltage . . . . . (V+) +0.3V to (V-) -0.3V
Input Current, power on or off
Digital Inputs . . . . . ±20mA
Analog Inputs . . . . . ±50mA

Continuous Total Power Dissipation (T_A = +70°C)
40-Pin Plastic DIP (derate 11.3mW/°C above +70°C) . 889mW
40-Pin CERDIP (derate 20.0mW/°C above +70°C) . . 1600mW
44-Pin PLCC (derate 13.3mW/°C above +70°C 1066mW
Operating Temperature Ranges:
MAX456C__ __ . . . . . 0°C to +70°C
MAX456E__ __ . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -65°C to +160°C
Lead Temperature (soldering, 10 sec) . . . . . +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 5.0V, V- = -5.0V; -1.3V ≤ V_{IN} ≤ +1.3V; Load Pin = +5V; Internal Load Resistors On; AGND = DGND = 0V; T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range		-1.3		1.3	V
Voltage Gain	Internal Load Resistors On, No External Load, V_{IN} = 0V to +1V T_A = +25°C T_A = -40°C to +85°C	 0.99 0.98	 1.0 1.0	 1.01 1.02	V/V
Buffer Offset Voltage	T_A = +25°C T_A = -40°C to +85°C			±5 ±12	mV
Offset Voltage Drift	T_A = -40°C to +85°C		20		µV/°C
Operating Supply Voltage		±4.5		±5.5	V
Supply Current, All Buffers On (No External Load)	T_A = +25°C T_A = -40°C to +85°C		39	45 60	mA
Supply Current, All Buffers Off	T_A = +25°C T_A = -40°C to +85°C		1.5	3 4	mA
Power-Supply Rejection Ratio	±4.5V to ±5.5V, DC Measurement	50	64		dB
Analog Input Current	T_A = -40°C to +85°C		±0.1	±10	nA
Output Leakage Current	Internal Load Resistors Off, All Buffers Off T_A = -40°C to +85°C			±100nA	nA

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5.0V, V- = -5.0V; -1.3V ≤ V_{IN} ≤ +1.3V; Load Pin = +5V; Internal Load Resistors On; AGND = DGND = 0V; T_A = +25°C, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Internal-Amplifier Load Resistor (LOAD Pin = 5V)	T_A = +25°C T_A = -40°C to +85°C	250 200	400	600 765	Ω
Buffer-Output Voltage Swing	Internal Load Resistors On, No Ext. Load	±1.3			V
Digital Input Current	T_A = -40°C to +85°C			±1	µA
Output Impedance at DC			10		Ω
Input Logic Low Threshold Input Logic High Threshold		 2.4		0.8	V
SER OUT Output Logic Low (Pin 1) SER OUT Output Logic High	Serial Mode, SER/$\overline{PAR}$ = 5V I_{OL} = 1.6mA I_{OH} = -0.4mA	 4		0.4	V
Dynamic Specifications (Note 1)					
Output-Buffer Slew Rate	Internal Load Resistors On, 10pF Load		250		V/µs
Single-Channel Crosstalk	At 5MHz, V_{IN} = $2V_{P-P}$ (Note 2)	60	70		dB
All-Channel Crosstalk	5MHz, V_{IN} = $2V_{P-P}$ (Notes 2, 3)		57		dB
All-Channel Off Isolation	5MHz, V_{IN} = $2V_{P-P}$ (Note 2)		80		dB
-3dB Bandwidth	10pF Load, V_{IN} = $2V_{P-P}$ (Note 2)	25	35		MHz
Differential Phase Error	Note 4		1.0		deg
Differential Gain Error	Note 4		0.5		%
Input Noise	DC to 40MHz		0.3	1.0	mV_{rms}
Input Capacitance	All Buffer Inputs Grounded		6		pF
Buffer Input Capacitance	Additional Capacitance for Each Output Buffer Connected to Channel Input		2		pF
Output Capacitance	Output Buffer Off		7		pF

Note 1: Guaranteed by design.
Note 2: See *Dynamic Test Circuits* on page 11.
Note 3: 3dB typical crosstalk improvement when R_S = 0Ω.
Note 4: Input test signal: 3.58MHz sine wave of amplitude 40IRE superimposed on a linear ramp (0 to 100IRE). IRE is a unit of video-signal amplitude developed by the International Radio Engineers. 140IRE = 1.0V.

8 x 8 Video Crosspoint Switch

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 5.0V, V- = -5.0V; -1.3V ≤ V_{IN} ≤ +1.3V; Load Pin = +5V; Internal Load Resistors On; AGND = DGND = 0V)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Switching Characteristics (Note 1) (See Figure 4) $T_A = T_{MIN}$ to T_{MAX}						
Chip Enable to Write Setup	t_{CE}		0			ns
Write Pulse Width	t_{WR}		80			ns
Data Setup	t_{DS}	Parallel Mode 32-bit Serial Mode	240 160			ns
Data Hold	t_{DH}		0			ns
Latch Pulse Width	t_L		80			ns
Latch Delay	t_D		80			ns
Switch Break-Before-Make Delay	t_{ON}-t_{OFF}			15		ns
LATCH Edge to Switch (Off) (On)	 t_{OFF} t_{ON}	 LATCH On		 35 50		ns

Note 1: Guaranteed by design.

Detailed Description

Output Buffers

The MAX456 video crosspoint switch consists of 64 T-switches in an 8 x 8 grid (Figure 1). The 8 matrix outputs are followed by 8 wideband buffers optimized for driving 400Ω and 20pF loads. Each buffer has an internal active load on the output which can be readily shut off via the LOAD input (Off when LOAD = 0V). This is useful when two or more MAX456 circuits are connected in parallel to increase the number of input channels. In such applications, only one set of buffers is active at a time, and they can drive only one set of loads. The buffers **must** have a load when they are active. This load may be:

1. The internal load
2. The internal load of another buffer in another MAX456
3. An external load (390Ω to 470Ω resistor)

Each MAX456 output can be disabled under logic control. When a buffer is disabled, its output enters a high impedance state. In multichip-parallel applications, the disable function prevents inactive outputs from loading lines driven by other devices. Disabling the inactive buffers reduces power consumption.

The MAX456 outputs connect easily to MAX457 dual amplifiers when 75Ω loads must be driven.

Power-On RESET

The MAX456 has an internal power-on reset (POR) circuit which remains low for 5µs when power is applied. POR also remains low if the total supply voltage is less than 4V. In the serial-interface mode, the POR clears all address and data latches and **disables all buffer outputs at power-up.** In the parallel-interface mode, random data can override this initial preset, so initial conditions should be re-programmed soon after power-up.

Digital Interface

Refer to Table 3 and the *Timing Diagrams*, Figures 4-6. Switch programming data is loaded in one of two ways:

7-bit Parallel
32-bit Serial

All action associated with the $\overline{WR}$ line occurs on its rising edge. The same is true for the LATCH line if EDGE/$\overline{LEVEL}$ is high. Otherwise, the 2nd-rank registers update while LATCH is low (when EDGE/$\overline{LEVEL}$ is low). $\overline{WR}$ is logically ANDed with CE and $\overline{CE}$ to allow active-high or active-low chip enable.

7-Bit Parallel Mode

In the parallel mode, the 7 data bits A2-A0 and D3-D0 specify an output channel (A2-A0) and the input channel to which it connects (D3-D0). The data is loaded on the rising edge of $\overline{WR}$. The 8 input channels are selected by 0000 through 0111 (D3-D0). The remaining 8 codes (1000-1111) control other MAX456 functions as listed in Table 1.

Table 1. Parallel-Mode Functions

A2-A0	D3-D0	FUNCTION
Selects Output Buffer, OUT0 to OUT7	0000 to 0111	Connect the buffer selected by A2-A0 to the input channel selected by D3-D0.
	1000	Connect the buffer selected by A2-A0 to DGND. Note, if the buffer output is on, its output is its offset voltage.
	1011	Shut off buffer selected by A2-A0, and retain 2nd-rank contents.
	1100	Turn on buffer selected by A2-A0, or restore previously connected channel.
	1101	Turn off all buffers, and leave 2nd-rank registers unchanged.
	1110	Turn on all buffers, or restore previously connected channels.
	1111	Send a pulse to the 2nd-rank registers to load them with the contents of the 1st-rank registers. This is a "software-LOAD" command to the 2nd-rank registers.
	1001 and 1010	Do not use these codes in the parallel-interface mode. These codes are for the serial-interface mode only.

32-Bit Serial Mode

In the serial mode (SER/$\overline{PAR}$ = high) all 1st-rank registers are loaded with data, making it unnecessary to specify an output address (A2,A1,A0). The input data format is D3-D0, starting with OUT0 and ending with OUT7 for 32 total bits. Only codes 0000 through 1010 are valid. Code 1010 disables a buffer, while code 1001 enables it. After data is shifted into the 32-bit 1st-rank register, it is transferred to the 2nd rank by the LATCH line.

Table 2. Serial-Mode Functions

D3-D0	FUNCTION
0000 to 0111	Connect the selected buffer to the input channel selected by D3-D0.
1000	Connect the input of the selected buffer to GND. Note, if the buffer output remains on, its output is its offset voltage.
1001	Turn on the selected buffer and connect its input to GND. Use this code to turn on buffers after power is applied. The default power-up state is all buffers disabled.
1010	Shut off the selected buffer at the specified channel, and erase data stored in the 2nd rank of registers. The 2nd rank now holds the command word 1010.
1011 to 1111	Do not use these codes in the serial-interface mode. They inhibit the latching of the 2nd-rank registers, which prevents proper loading of data.

Pin Descriptions

MAX456 DIP PIN#	MAX456 PLCC PIN#	NAME	FUNCTION
—	1	N.C.	No Connect
1	2	D1/SER OUT	Parallel Data Bit D1 when SER/$\overline{PAR}$ = 0V. When SER/$\overline{PAR}$ = 5V, this pin is a Serial Output for cascading multiple parts.
2	3	D0/SER IN	Parallel Data Bit D0 when SER/$\overline{PAR}$ = 0V. A Serial Input when SER/$\overline{PAR}$ = 5V.
3	4	A2	Output-Buffer Address Line
4	5	A1	Output-Buffer Address Line
5	6	IN0	1-of-8 Video Input Lines
6	7	A0	Output-Buffer Address Line
7	8	IN1	1-of-8 Video Input Lines

Pin Descriptions continued on next page

8 x 8 Video Crosspoint Switch

Pin Descriptions (continued)

MAX456 DIP PIN#	MAX456 PLCC PIN#	NAME	FUNCTION
8	9	LOAD	LOAD is an asynchronous control line. When LOAD = 1, all the 400Ω internal active loads are on. When LOAD = 0, external 400Ω loads must be used. The buffers MUST have a resistive load to maintain stability.
9	10	IN2	1-of-8 Video Input Lines
10,12	11, 14	DGND	1-of-2 Digital Ground Pins. Both DGND pins must have the same potential and be bypassed to AGND. DGND should be within ±0.3V of AGND.
—	12	N.C.	No Connect
11	13	IN3	1-of-8 Video Input Lines
13	15	IN4	1-of-8 Video Input Lines
14	16	EDGE/$\overline{\text{LEVEL}}$	When this control line is high, the 2nd-rank registers are loaded with the rising edge of the LATCH line. If the line is low, the 2nd-rank registers are transparent, passing data directly from the 1st-rank registers to the decoders.
15	17	IN5	1-of-8 Video Input Lines
16,26,40	18,29,44	V+	All V+ pins must be tied to each other and bypassed to AGND separately (See Figure 2).
17	19	IN6	1-of-8 Video Input Lines
18	20	SER/$\overline{\text{PAR}}$	5V = Serial 32Bit 0V = 7-Bit Parallel
19	21	IN7	1-of-8 Video Input Lines
20, 34	22, 38	V-	Both V- pins must be tied to each other and bypassed to AGND separately (See Figure 2).
—	23	N.C.	No Connect
21	24	$\overline{\text{WR}}$	$\overline{\text{WRITE}}$. In the serial mode, $\overline{\text{WR}}$ shifts data in. In the parallel mode, $\overline{\text{WR}}$ loads data into the 1st-rank registers. Data is latched on the rising edge.
22	25	LATCH	If EDGE/$\overline{\text{LEVEL}}$ = 5V, data latches from the 1st-rank registers to the 2nd-rank registers on the rising edge. If EDGE/$\overline{\text{LEVEL}}$ = 0V, data is latched while the LATCH = 0V.
23	26	$\overline{\text{CE}}$	$\overline{\text{Chip Enable}}$. When $\overline{\text{CE}}$ = 0V and CE = 5V, the $\overline{\text{WR}}$ line is enabled.
24	27	CE	Chip Enable. When $\overline{\text{CE}}$ = 0V and CE = 5V, the $\overline{\text{WR}}$ line is enabled.
25	28	OUT7	Output Buffer 7 (Note 1)
27	30	OUT6	Output Buffer 6 (Note 1)
28,30,32	31,33,36	AGND	Analog Ground must be at 0.0V since the gain resistors of the buffers are tied to these 3 pins.
29	32	OUT5	Output Buffer 5 (Note 1)
—	34	N.C.	No Connect
31	35	OUT4	Output Buffer 4 (Note 1)
33	37	OUT3	Output Buffer 3 (Note 1)
35	39	OUT2	Output Buffer 2 (Note 1)
36	40	D3	Parallel Data Bit D3 when SER/$\overline{\text{PAR}}$ = 0V. When D3 = 0V, D0-D2 specifies the input channel to be connected to buffer. When D3 = 5V, then D0-D2 specify control codes. D3 is not used when SER/$\overline{\text{PAR}}$ = 5V.
37	41	OUT1	Output Buffer 1 (Note 1)
38	42	D2	Parallel Data Bit D2 when SER/$\overline{\text{PAR}}$ = 0V. Not used when the SER/$\overline{\text{PAR}}$ = 5V.
39	43	OUT0	Output Buffer 0 (Note 1)

Note 1: Buffer inputs are internally grounded with a 1000 or 1001 command from the D3-D0 lines. AGND must be at 0.0V since the gain-setting resistors of the buffers are internally tied to AGND.

Functional Diagram

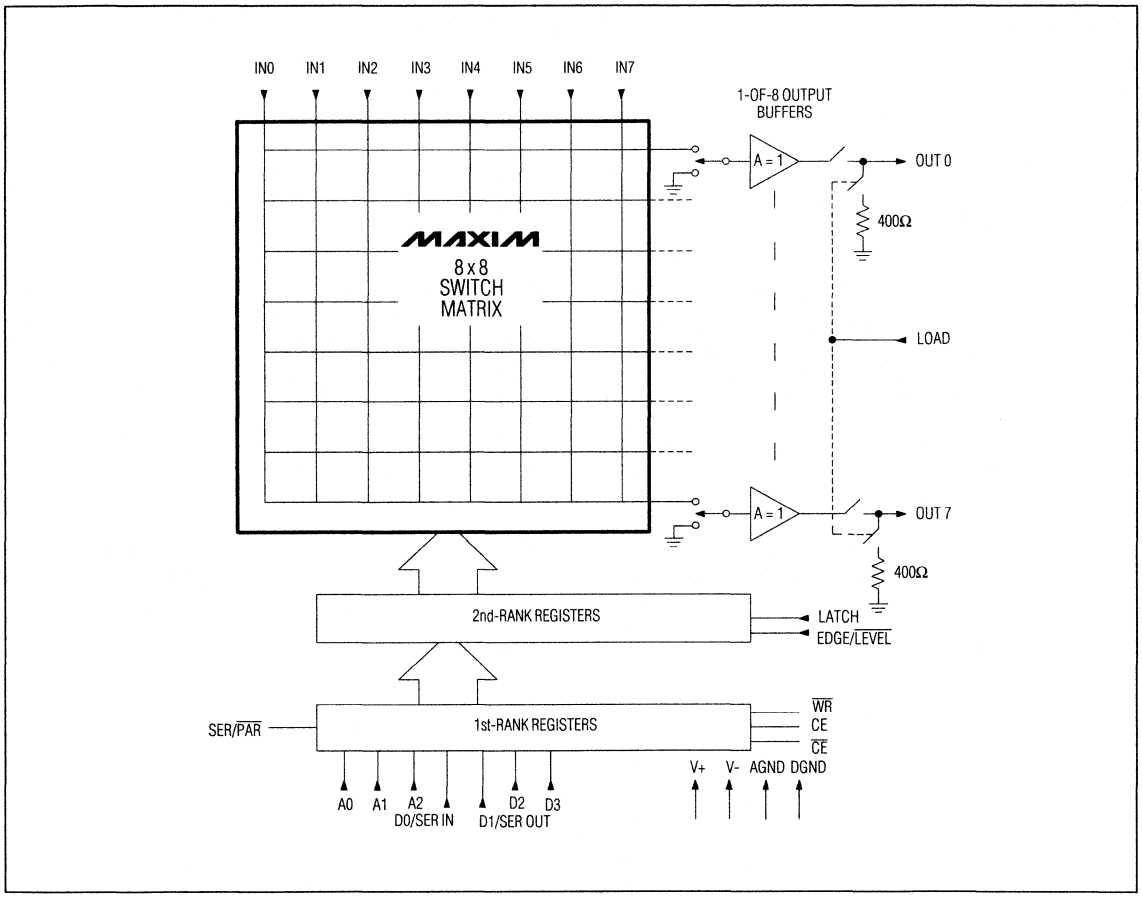


Figure 1. MAX456 Functional Diagram

8 x 8 Video Crosspoint Switch

Table 3. Input/Output Line Configurations

SERIAL/ PARALLEL	D3	D2	D1	D0	A2-A0	COMMENT
H	X	X	Serial Output	Serial Input	X	32-Bit Serial Mode
L	H	Parallel Input	Parallel Input	Parallel Input	Parallel Mode	D0-D2 = Control Code
L	L	Parallel Input	Parallel Input	Parallel Input	Parallel Mode	D0-D2 = Input Address

Note: X = Don't Care, H = 5V, L = 0V

Typical Application

Figure 2 shows a typical application of the MAX456 with MAX457 (dual) amplifiers at the outputs to drive 75Ω loads. This application shows the MAX456 digital-switch control interface set up in the 7-bit parallel mode. Each of the MAX456 output buffers drives a MAX457 with a gain of 2. The MAX456 uses 7 data lines and 2 control lines ($\overline{WR}$ and LATCH). Two additional lines may be needed to control CE and LOAD when using multiple MAX456s.

The input/output information is presented to the chip at A2-A0 and D3-D0 by a parallel printer port. The data is stored in the 1st-rank registers on the rising edge of $\overline{WR}$. When the LATCH line goes high, the switch configuration is loaded into the 2nd-rank registers, and all 8 outputs enter the new configuration at the same time. Each 7-bit data word updates only one output buffer at a time. If several buffers are to be updated, the data is individually loaded into the 1st-rank registers. Then, a single LATCH pulse is used to reconfigure all channels simultaneously.

The short Basic program in Figure 3 loads programming data into the MAX456 from any IBM PC or compatible. It uses the computer's "LPT1" output to interface to the circuit, then automatically finds the address for LPT1 and displays a table of valid input values to be used. The program does not keep track of previous commands, but it does display the last data sent to LPT1, which is written and latched with each transmission.

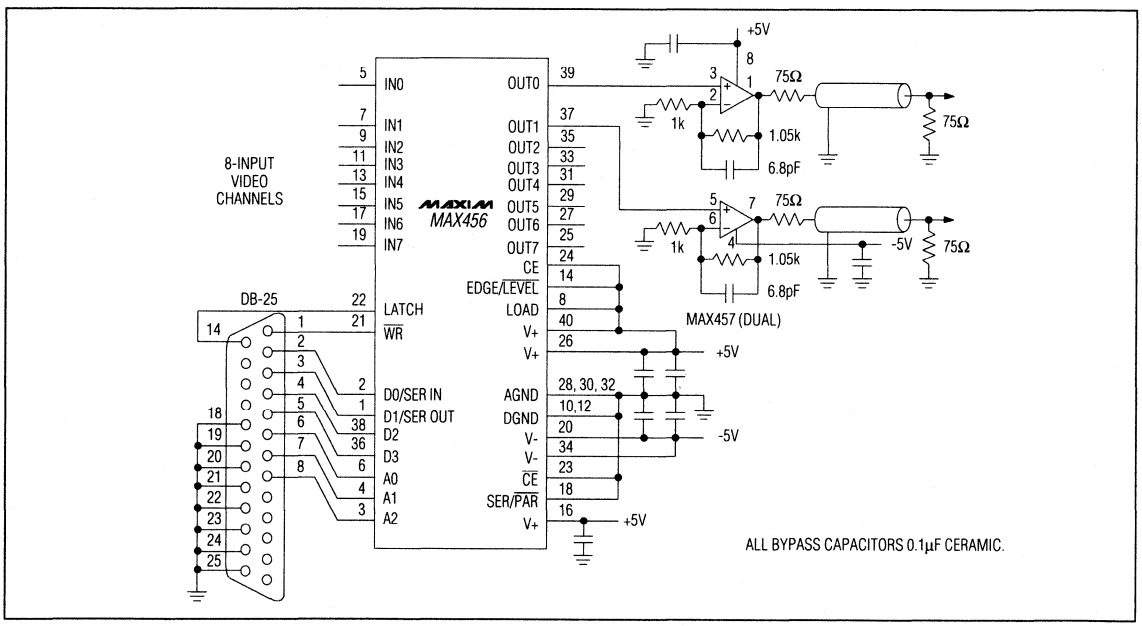


Figure 2. Typical Application

```
10  REM MAX456st rev. 4/26/90  : CLS
20  DIM VALU(5,5): COL=17 : RO=5
30  DEF SEG=&H0  : ADDRESS=(PEEK(&H409)*256)+(PEEK(&H408))
40  LOCATE RO-4,COL-2   : PRINT"MAX456  8 X 8  CROSSPOINT SWITCH "
50  LOCATE RO+8,COL-12  : PRINT " Input and control codes:"
60  LOCATE RO+10,COL-16 : PRINT "0 to 7 = Valid channel and buffer input values"
70  LOCATE RO+11,COL-12 : PRINT " 8 = Specify Buffer input to connect to ground"
80  LOCATE RO+12,COL-12 : PRINT "11 = Shut off specified Buffer output"
90  LOCATE RO+13,COL-12 : PRINT "12 = Turn  on specified Buffer output"
100 LOCATE RO+14,COL-12 : PRINT "13 = Shut off all Buffer outputs"
110 LOCATE RO+15,COL-12 : PRINT "14 = Turn  on all Buffer outputs"
120 LOCATE RO+16,COL-12 : PRINT " E = End Program"
130 LOCATE RO+0,COL+21  : PRINT "        "
140 LOCATE RO-1,COL+5   : PRINT "Input Channel or "
150 LOCATE RO+0,COL+5   : INPUT "Control Code ? ",CH$ : REM D0-D3
160 CH=VAL(RIGHT$(CH$,2)) : IF CH<0 OR CH>15 OR CH=9 OR CH=10 THEN 130
170 IF RIGHT$(CH$,1)="E" OR RIGHT$(CH$,1)="e" THEN END
180 LOCATE RO+1,COL+5   : INPUT "Buffer Output ? ",AM$ : REM A0-A2
190 LOCATE RO+1,COL+21  : PRINT "        "
200 AM=VAL(RIGHT$(AM$,1)) : IF AM<0 OR AM>7 THEN 180
210 LOCATE RO+3,COL+5   : PRINT "OUTPUT VALUES"
220 LOCATE RO+4,COL+5   : PRINT "DATA=";CH :LOCATE RO+4,COL+15 :PRINT" BUF=";AM
230 OUT ADDRESS,(AM*16)+CH: REM DATA OUT
240 OUT ADDRESS+2,1     : REM WRite low  DB25-1
250 OUT ADDRESS+2,2     : REM Latch low  DB25-14  and WR hi DB25-1
260 OUT ADDRESS+2,0     : REM take Latch hi
270 GOTO 130
```

Figure 3. Basic Program for Loading Data into the MAX456 from a PC Using the Circuit of Figure 2

Timing Diagrams

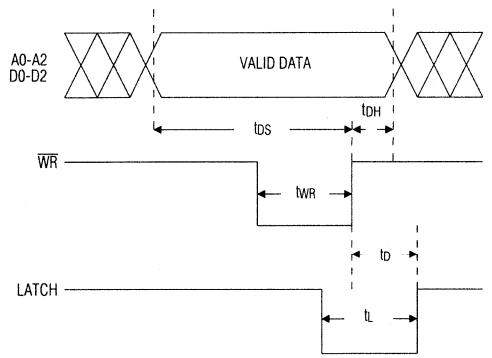


Figure 4. MAX456 Write Timing for Serial and Parallel Interface Modes

8 x 8 Video Crosspoint Switch

Timing Diagrams (continued)

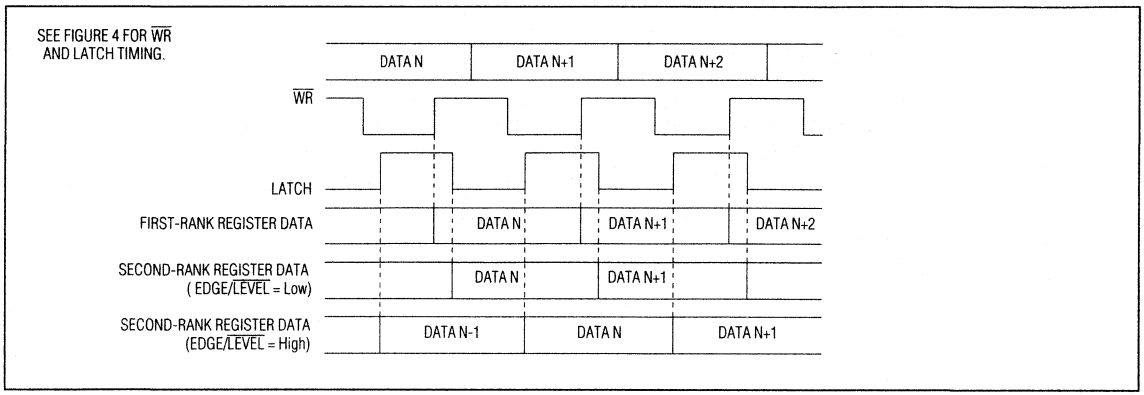


Figure 5. Parallel-Mode Interface Format (SER/PAR = Low)

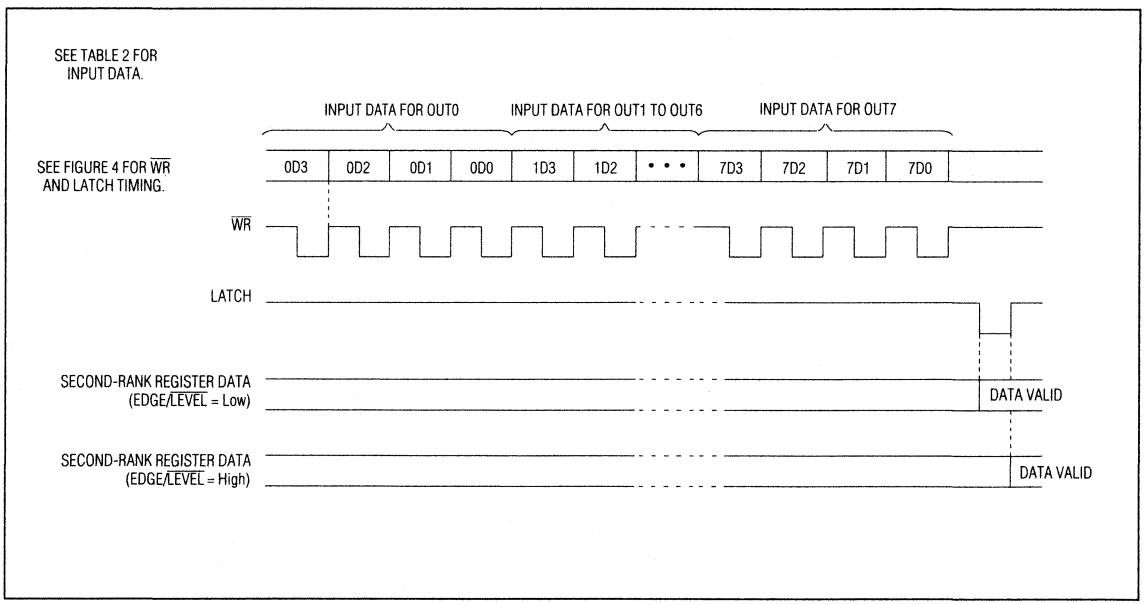
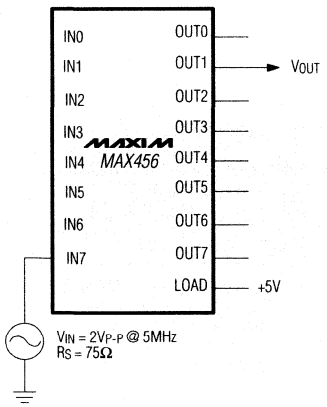
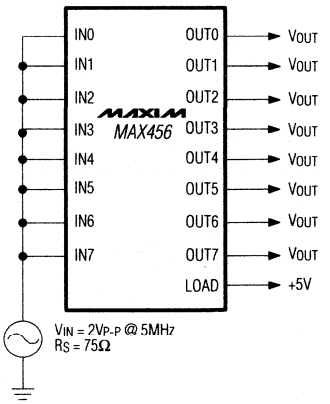


Figure 6. 32-Bit Serial-Mode Interface Format (SER/PAR = High)

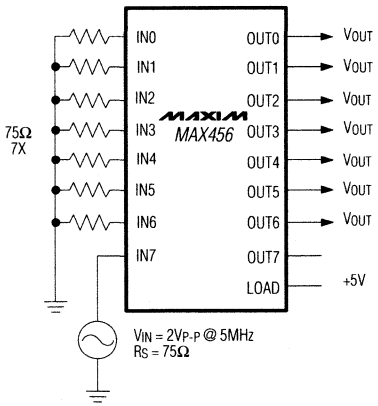
Dynamic Test Circuits



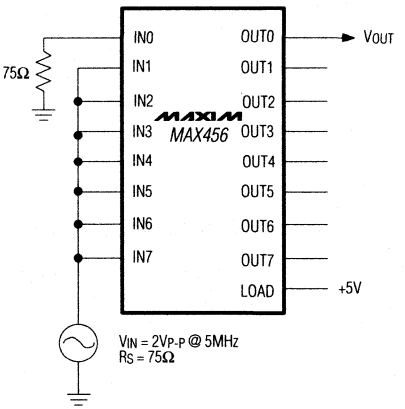
-3dB Bandwidth (Notes 1-4)



All-Channel Off Isolation (Notes 1, 5-8)



Single-Channel Crosstalk (Notes 1, 5, 9-11)

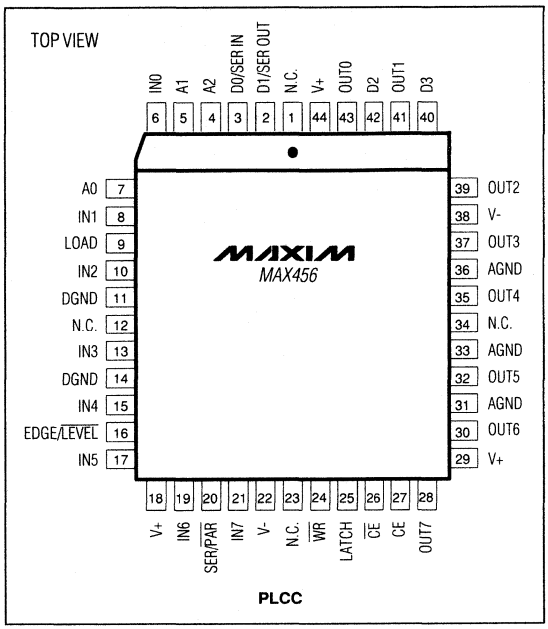


All-Channel Crosstalk (Notes 1, 5, 9, 11, 12)

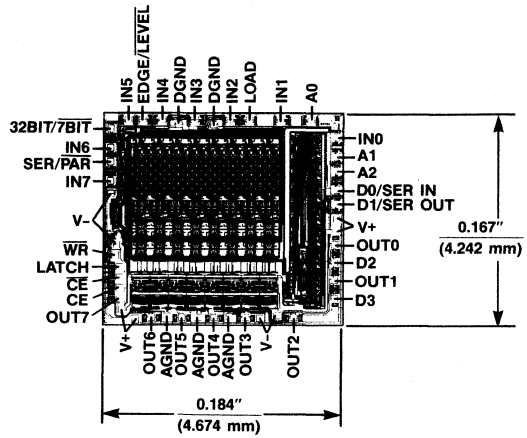
Note 1. Connect LOAD (pin 8) to +5V (internal 400Ω loads on at all outputs).
Note 2. Program any one input to connect to any one output (see Table 1 or 2 for programming codes).
Note 3. Turn on buffer at the selected output (see Table 1 or 2).
Note 4. Drive the selected input with V_{IN}, and measure V_{OUT} at the -3dB frequency at the selected output.
Note 5. Program each numbered input to connect to the same numbered output (IN0 to OUT0, IN1 to OUT1, etc. See Table 1 or 2 for programming codes).
Note 6. Turn off all output buffers (see Table 1 or 2).
Note 7. Drive all inputs with V_{IN} and measure V_{OUT} at any output.
Note 8. Isolation (in dB) = $20\log_{10}(V_{OUT}/V_{IN})$.
Note 9. Turn on all output buffers (see Table 1 or 2).
Note 10. Drive any one input with V_{IN} and measure V_{OUT} at any undriven output.
Note 11. Crosstalk (in dB) = $20\log_{10}(V_{OUT}/V_{IN})$.
Note 12. Drive all but one input with V_{IN} and measure V_{OUT} at the undriven output.

8 x 8 Video Crosspoint Switch

Pin Configurations (continued)



Chip Topography



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX456EPL	-40°C to +85°C	40 Plastic DIP
MAX456EJL	-40°C to +85°C	40 CERDIP
MAX456EQH	-40°C to +85°C	44 PLCC

D/A Converters

* Advance Information – first page of data sheet in preparation.

Part Number	Resolution (Bits)	Output Type[1]	DACs in Package	Reference[2]	Settling Time (µs)	Data-Bus Interface (Bits)	Supply Voltage[3] (V)	Features	Price† 1000-up ($)
MAX7624	8	I	1	MDAC	0.25	µP/8	+12/+15	Improved MX7524	2.26
MX7224	8	V	1	Ext	5.0	µP/8	+12/+15 & -5	Single or dual supplies	3.16
MX7523	8	I	1	MDAC	0.15	Logic	+15	Low-cost 8-bit DAC	2.60
MX7524	8	I	1	MDAC	0.4	µP/8	+5/+15	Low-cost 8-bit DAC	2.52
MX7520	10	I	1	MDAC	0.5	Logic	+15	Low-cost 10-bit DAC	2.80
MX7530	10	I	1	MDAC	0.5	Logic	+15	Low-cost 10-bit DAC	2.80
MX7533	10	I	1	MDAC	0.6	Logic	+15	Low-cost 10-bit DAC	2.84
MAX501	12	V	1	MDAC	5.0	µP/8+4	±12/±15	4-quadrant multiplying DAC	5.65
MAX502	12	V	1	MDAC	5.0	µP/12	±12/±15	4-quadrant multiplying DAC	5.65
MAX507	12	V	1	Int	10.0	µP/12	±15/±12	Complete 12-bit DAC with reference	7.65
MAX508	12	V	1	Int	10.0	µP/8+4	±15/±12	Complete 12-bit DAC with reference	7.65
MAX543	12	I	1	MDAC	1.0	Serial	+5/+12/+15	12-bit multiplying DAC in 8-pin DIP	6.80
MAX7645	12	I	1	MDAC	1.0	µP/12	+15	Improved MX7545	5.60
MX566A	12	I	1	Ext	0.35	Logic	-15	No built-in reference	††
MX565A	12	I	1	Int	0.25	Logic	+15 & -15	With +10V buried-zener reference	††
MX7245	12	V	1	Int	10.0	µP/12	±15, +12/+15	Single or dual supplies with reference	8.33
MX7248	12	V	1	Int	10.0	µP/8+4	±15, +12/+15	8-bit interface MX7245	8.33
MX7521	12	I	1	MDAC	0.5	Logic	+15	Low-cost 12-bit DAC	5.00
MX7531	12	I	1	MDAC	0.5	Logic	+15	Low-cost 12-bit DAC	5.08
MX7541	12	I	1	MDAC	1.0	Logic	+15	12-bit data bus	5.07
MX7541A	12	I	1	MDAC	0.6	Logic	+15	12-bit data bus	5.72
MX7542	12	I	1	MDAC	2.0	4-bit µP	+5	4-bit data bus with latches	7.52
MX7543	12	I	1	MDAC	2.0	Serial	+5	Serial interface	7.52
MX7545	12	I	1	MDAC	2.0	µP/12	+5/+15	12-bit data bus with latches	5.00
MX7545A	12	I	1	MDAC	1.0	µP/12	+5/+15	Improved MX7545	6.03
MX7548	12	I	1	MDAC	1.0	µP/8	+5/+12/+15	8-bit data bus with latches	6.06
MX7845	12	V	1	MDAC	5.0	µP/12	±15	4-range 4-quadrant multiplying DAC	6.26
MX7534	14	I	1	MDAC	1.5	µP/8	+12/+15	Double-buffered inputs	13.37
MX7535	14	I	1	MDAC	1.5	µP/8/14	+12/+15	Double-buffered inputs	15.00
MX7536	14	I	1	MDAC	1.5	µP/8/14	+12/+15	No external resistors needed	14.66
MX7538	14	I	1	MDAC	1.5	µP/14	+12/+15	Low-cost 14-bit DAC	8.88

[1] V = voltage, I = current
[2] MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference
[3] "/" indicates "to" and "," indicates "or"
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.

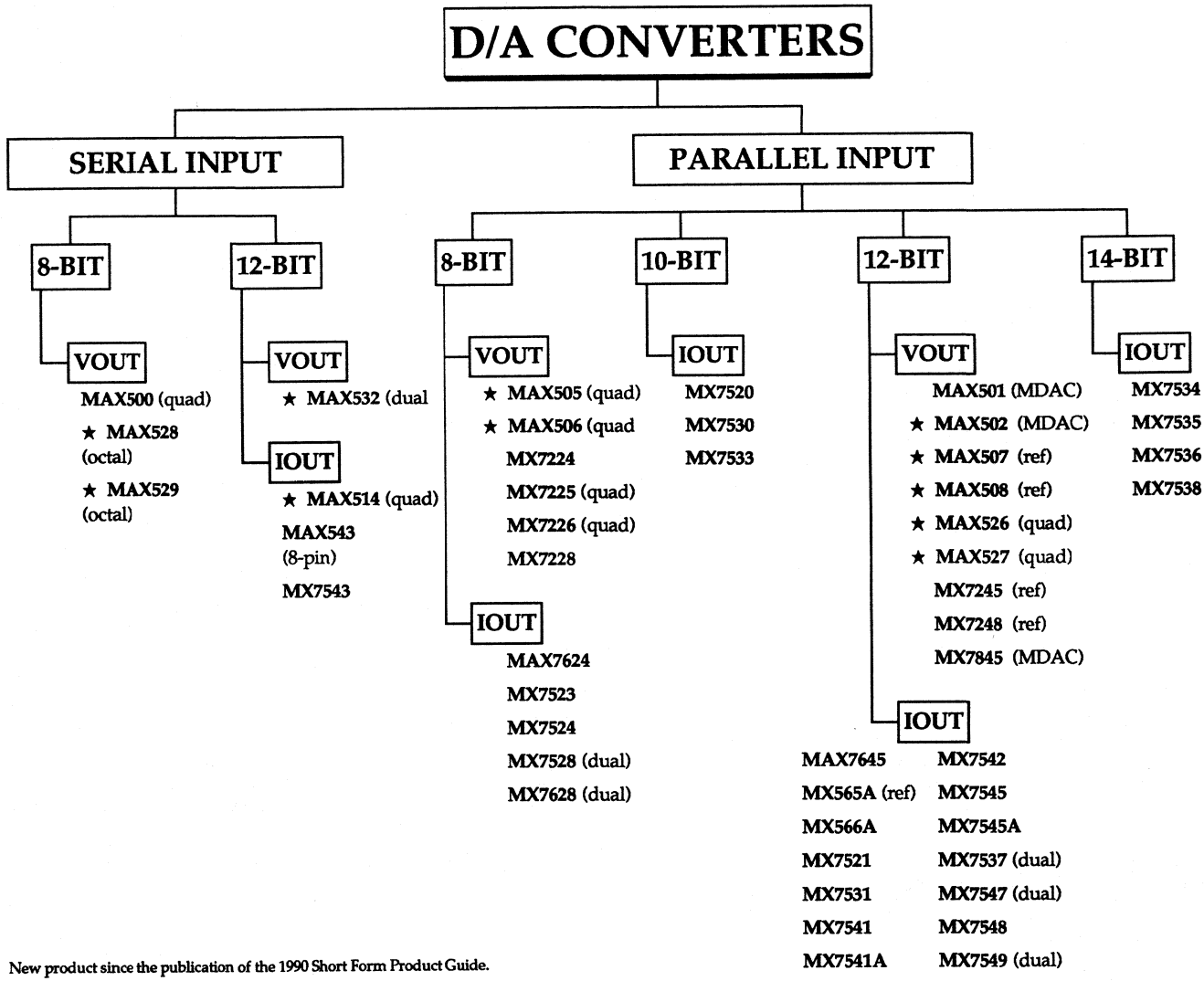
Part Number	Resolution (Bits)	Output Type[1]	DACs in Package	Reference2	Settling Time (µs)	Data-Bus Interface (Bits)	Supply Voltage[3] (V)	Features	Price† 1000-up ($)
DUAL									
MX7528	8	I	2	MDAC	0.18	µP/8	+5/+15	Data latches for both DACs	3.79
MX7628	8	I	2	MDAC	0.35	µP/8	+12/+15	Data latches for both DACs	3.80
MAX532	12	V	2	MDAC	4.0	Serial	±12/±15	16-pin DIP/SO	††
MX7537	12	I	2	MDAC	1.5	µP/8	+12/+15	Dual DAC with 8-bit data bus	11.23
MX7547	12	I	2	MDAC	1.5	µP/12	+12/+15	Dual DAC with 12-bit data bus	11.40
MX7549	12	I	2	MDAC	1.5	µP/4	+15	Dual DAC with 4-bit data bus	12.97
QUAD									
MAX500	8	V	4	Ext	4.0	Serial	+12/+15 & -5	Single or dual supplies	5.70
MAX505	8	V	4	MDAC	6.0	µP/8	+5/±5	Double-buffered logic, separate reference inputs	6.95
MAX506	8	V	4	MDAC	6.0	µP/8	+5/±5	Single-buffered logic, single reference input	6.10
MX7225	8	V	4	Ext	4.0	µP/8	+12/+15 & -5	Double buffered	14.14
MX7226	8	V	4	Ext	4.0	µP/8	+12/+15 & -5	Single buffered	11.80
MAX514	12	I	4	MDAC	1.0	Serial	+5/+15	Quad current-output DACs, available in DIP/SO	15.79
MAX526	12	V	4	Ext	3.0	µP/8+4	+12/+15 & -5	Quad voltage-output DACs, available in DIP/SO	21.60
MAX527	12	V	4	Ext	3.0	µP/8+4	±5	±5V version of MAX526	21.60
OCTAL									
MAX528	8	V	8	Ext	5.0	Serial	+5/+15, +15 & -5, +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	8	Ext	5.0	Serial	+5	Single +5V supply MAX528	5.65
MX7228	8	V	8	Ext	5.0	µP/8	+5/+15 & -5, +15	Single or dual supplies	24.57

1 V = voltage, I = current
2 MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference
3 "/" indicates "to" and "," indicates "or"
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.

Serial D/A Converters

Part Number	Resolution (Bits)	Output Current Voltage[1]	DACs in Package	Reference[2]	Settling Time (µs)	Data-Bus Interface (Bits)	Supply Voltage[3] (V)	Features	Price† 1000-up ($)
MAX500	8	V	4	Ext	4.0	Serial	+12/+15 & -5	Single or dual supplies	5.70
MAX528	8	V	8	Ext	5.0	Serial	+5/+15, +15 & -5, +5 & -15	µP-selected buffered and unbuffered output	6.90
MAX529	8	V	8	Ext	5.0	Serial	+5	Single +5V supply MAX528	5.65
MAX514	12	I	4	MDAC	1.0	Serial	+5	Quad current-output DACs, available in DIP/SO	15.79
MAX532	12	V	2	MDAC	4.0	Serial	±12/±15	16-pin DIP/SO	††
MAX543	12	I	1	MDAC	1.0	Serial	+5/+12/+15	8-pin AD7543 replacement	6.80
MX7543	12	I	1	MDAC	2.0	Serial	+5	Serial interface	7.52

[1] V = voltage, I = current
[2] MDAC = 4-quadrant multiplying capability, Int = internal reference, Ext = external reference
[3] "/" indicates "to" and "," indicates "or"
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.



★ New product since the publication of the 1990 Short Form Product Guide.

19-4011; Rev 0; 9/91

MAXIM

Voltage-Output, 12-Bit Multiplying DACs

General Description

The MAX501/MAX502 are 12-bit, 4-quadrant, voltage-output, multiplying digital-to-analog converters (DACs) with an output amplifier. Thin-film resistors, laser trimmed at the wafer level, maintain accuracy over the full operating temperature range.

The MAX501/MAX502 have buffered latches that are easily interfaced with microprocessors. Data is transferred into the input register in either a right-justified 8+4-bit format (MAX501) or with a 12-bit-wide data path (MAX502). In the MAX501, an $\overline{LDAC}$ signal transfers data from the input register to the DAC register. In the MAX502, the input registers are controlled by standard CHIP SELECT ($\overline{CS}$) and WRITE ($\overline{WR}$) signals. For stand-alone operation, the $\overline{CS}$ and $\overline{WR}$ inputs are grounded, making all latches transparent. All logic inputs are level triggered and compatible with TTL and +5V CMOS logic levels.

The internally compensated, low-input offset-voltage output amplifier provides an output voltage from +10V to -10V while sourcing and sinking up to 5mA.

Applications

Digital Attenuators
Programmable-Gain Amplifiers
Servo Controls
Digital to 4mA-to-20mA Converters
Automatic Test Equipment
Programmable Power Supplies

Features

- ♦ **12-Bit Voltage Output DAC**
- ♦ **±10V and 5mA Output Drive**
- ♦ **Monotonic Over Temperature**
- ♦ **Four Range-Scaling Resistors**
- ♦ **8+4 (MAX501) and 12-Bit (MAX502) Interface**
- ♦ **24-Pin DIP and Wide SO Packages**

Ordering Information

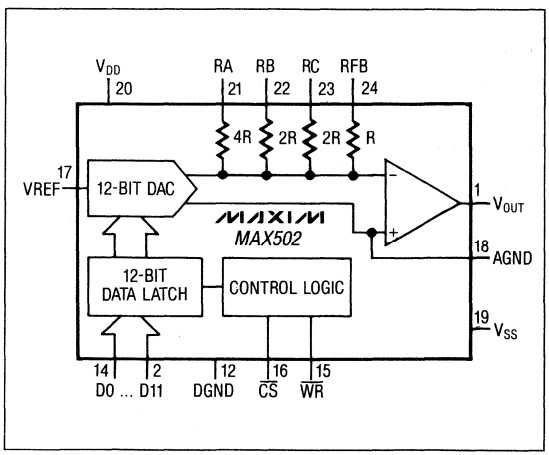
PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX501ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX501BCNG	0°C to +70°C	24 Narrow Plastic DIP	±3/4
MAX501ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX501BCWG	0°C to +70°C	24 Wide SO	±3/4
MAX501BC/D	0°C to +70°C	Dice*	±3/4
MAX501AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX501BENG	-40°C to +85°C	24 Narrow Plastic DIP	±3/4
MAX501AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX501BEWG	-40°C to +85°C	24 Wide SO	±3/4
MAX501AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1/2
MAX501BMRG	-55°C to +125°C	24 Narrow CERDIP**	±3/4

Ordering Information continued on last page.

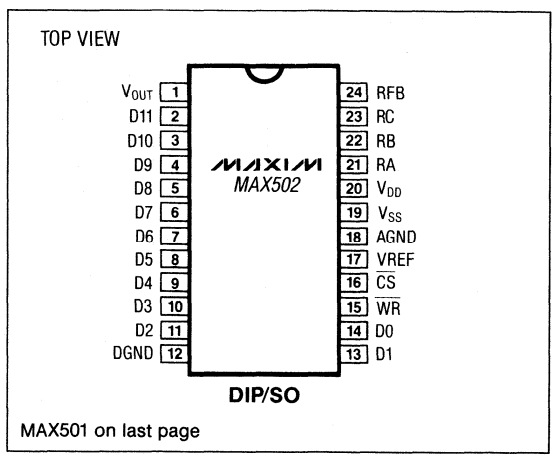
* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configurations



MAX501 on last page

Voltage-Output, 12-Bit Multiplying DACs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to DGND ..... +0.3V, -17V
VREF to AGND ..... ±25V
RFB to AGND ..... ±25V
RA to AGND ..... ±25V
RB to AGND ..... ±25V
RC to AGND ..... ±25V
V_{OUT} to AGND (Note 1) ..... V_{DD} +0.3V, V_{SS} -0.3V
V_{DD} to AGND ..... -0.3V, +17V
AGND to DGND ..... -0.3V, V_{DD}

Digital Input Voltage to DGND ..... -0.3V, V_{DD}
Continuous Power Dissipation (any package)
to +75°C 650mW
derate above +75°C ..... 10mW/°C
Operating Temperature Ranges:
MAX501_C_, MAX502_C_ ..... 0°C to +70°C
MAX501_E_, MAX502_E_ ..... -40°C to +85°C
MAX501_M_, MAX502_M_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: V_{OUT} may be shorted to AGND, V_{DD}, or V_{SS} if the power dissipation of the package is not exceeded.

Stresses beyond those under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Dual Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = -11.4V to -15.75V, VREF = +10V, AGND = DGND = 0V, R_L = 2kΩ, C_L = 100pF, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	T_A = +25°C	MAX501/502A			±1/2	LSB
			MAX501/502B			±3/4	
		T_A = T_{MIN} to T_{MAX}	MAX501/502A			±3/4	
			MAX501/502B			±1	
Differential Nonlinearity	DNL					±1	LSB
Zero-Code Offset Error		T_A = +25°C				±1	mV
		T_A = T_{MIN} to T_{MAX}	MAX501/502_C/E			±2	
			MAX501/502_M			±3	
Offset Temperature Coefficient	$\Delta V_{OS}/\Delta Temp$				±5		µV/°C
Gain Error		RFB, V_{OUT} connected				±3	LSB
		RC or RB connected to V_{OUT}, VREF = 5V				±4½	
		RA, V_{OUT} connected, VREF = 2.5V				±6	
Gain Temperature Coefficient	$\Delta Gain/\Delta Temp$				±1		ppm/°C
Reference Input Resistance		RFB		8	12	16	kΩ
Application Resistor Ratio Matching		RA to RB to RC match				0.5	%

ELECTRICAL CHARACTERISTICS (continued)

Dual Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = -11.4V to -15.75V, VREF = +10V, AGND = DGND = 0V, R_L = 2kΩ, C_L = 100pF, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
Input Current	I_{IN}	V_{IN} = 0V and V_{DD}	T_A = +25°C			±1	µA
			T_A = T_{MIN} to T_{MAX}			±10	
Input Low Voltage	V_{IL}					0.8	V
Input High Voltage	V_{IH}			2.4			V
Input Capacitance	C_{IN}				7		pF
POWER SUPPLIES							
Supply Voltage	V_{DD}			11.40		15.75	V
	V_{SS}			-11.40		-15.75	
Supply Current	I_{DD}	V_{OUT} unloaded				10	mA
	I_{SS}	V_{OUT} unloaded				4	
Power-Supply Rejection	PSR	ΔGain/ΔV_{DD}	VREF = -10V V_{DD} = 15V ± 5%			±0.02	%/%
			VREF = -8.9V V_{DD} = 12V ± 5%				
		ΔGain/ΔV_{SS}	VREF = 10V V_{SS} = -15V ± 5%			±0.02	
			VREF = 8.9V V_{SS} = -12V ± 5%				
DYNAMIC PERFORMANCE (Note 3)							
Output-Voltage Settling Time	t_S	To ±0.01% of full scale				5	µs
Slew Rate	SR				5		V/µs
DAC Glitch Impulse		Major carry transition			450		nV-s
Multiplying Feedthrough Error		VREF = ±10V at 10kHz, DAC = all 0s			5		mV_{P-P}
Unity-Gain Small-Signal Bandwidth					3		MHz
Full-Power Bandwidth					250		kHz
Total Harmonic Distortion	THD	VREF = $6V_{RMS}$ at 1kHz			-90		dB
OUTPUT CHARACTERISTICS							
Open-Loop Gain	A_{VO}	RFB not connected, V_{OUT} = ±10V, R_L = 2kΩ		90			dB
Output Resistance	R_O				0.2		Ω
Short-Circuit Current		T_A = +25°C			20		mA
Output Noise Voltage		0.1Hz to 10Hz, T_A = +25°C			2		μV_{RMS}
		f = 1kHz, T_A = +25°C			25		$nV/\sqrt{Hz}$

9

Voltage-Output, 12-Bit Multiplying DACs

TIMING CHARACTERISTICS (See Figures 1a, 1b)

Dual Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = -11.4V to -15.75V, VREF = +10V, AGND = DGND = 0V, R_L = 2kΩ, C_L = 100pF, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.) (Note 2)

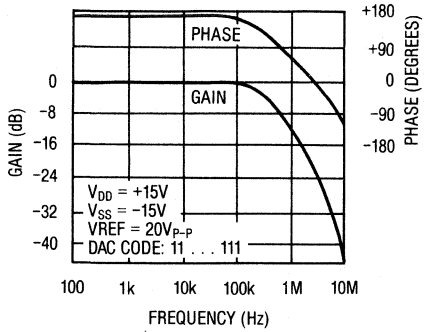
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MAX501							
Chip Select to Write-Setup Time	t_{CS}			0			ns
Write Pulse Width	t_{WR}	T_A = +25°C		55			ns
		T_A = T_{MIN} to T_{MAX}		70			
Data-Setup Time	t_{DS}	MAX501_C/E		50			ns
		MAX501_M		60			
Data-Hold Time	t_{DH}			10	0		ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}			70			ns
$\overline{CLR}$ Pulse Width	t_{CLR}			70			ns
$\overline{SET}$ Pulse Width	t_{SET}			200			ns
MAX502							
Chip Select to Write-Setup Time	t_{CS}			0			ns
Write Pulse Width	t_{WR}	T_A = +25°C		40			ns
		T_A = T_{MIN} to T_{MAX}	MAX502_C/E	50			
			MAX502_M	60			
Data-Setup Time	t_{DS}	MAX502_C/E		50			ns
		MAX502_M		60			
Data-Hold Time	t_{DH}			10	0		ns

Note 2: V_{OUT} must be less than V_{DD} - 2.5V and greater than V_{SS} + 2.5V to ensure correct operation. Performance at supplies other than V_{DD} = +15V and V_{SS} = -15V is guaranteed by PSRR tests.

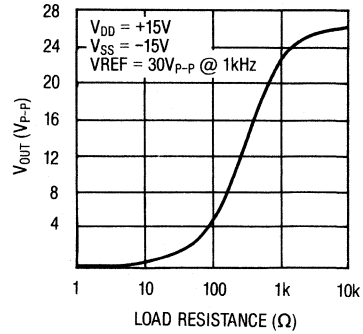
Note 3: Dynamic Performance and Output Characteristics are included for design guidance and are not subject to test.

Typical Operating Characteristics

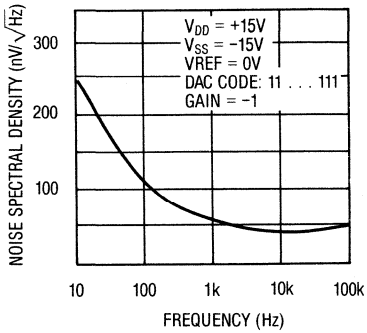
FREQUENCY RESPONSE, GAIN = –1



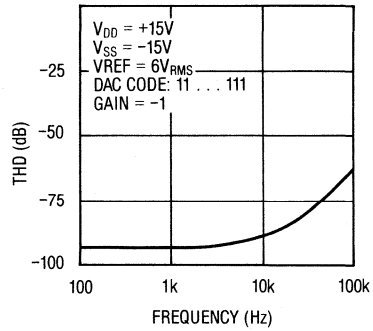
OUTPUT VOLTAGE SWING vs. RESISTIVE LOAD



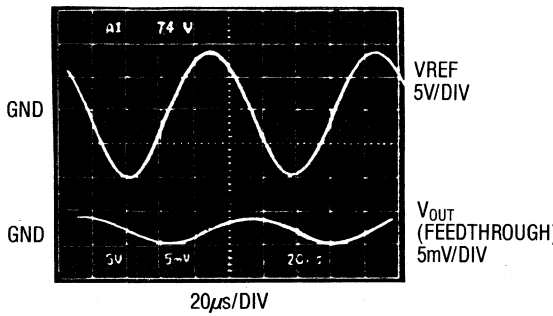
NOISE SPECTRAL DENSITY



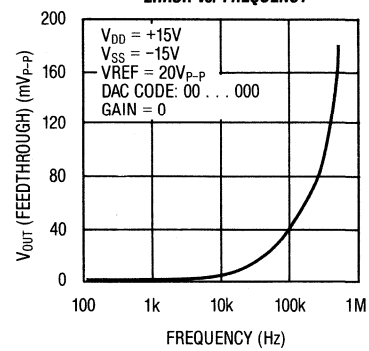
THD vs. FREQUENCY



MULTIPLYING FEEDTHROUGH ERROR



MULTIPLYING FEEDTHROUGH ERROR vs. FREQUENCY



9

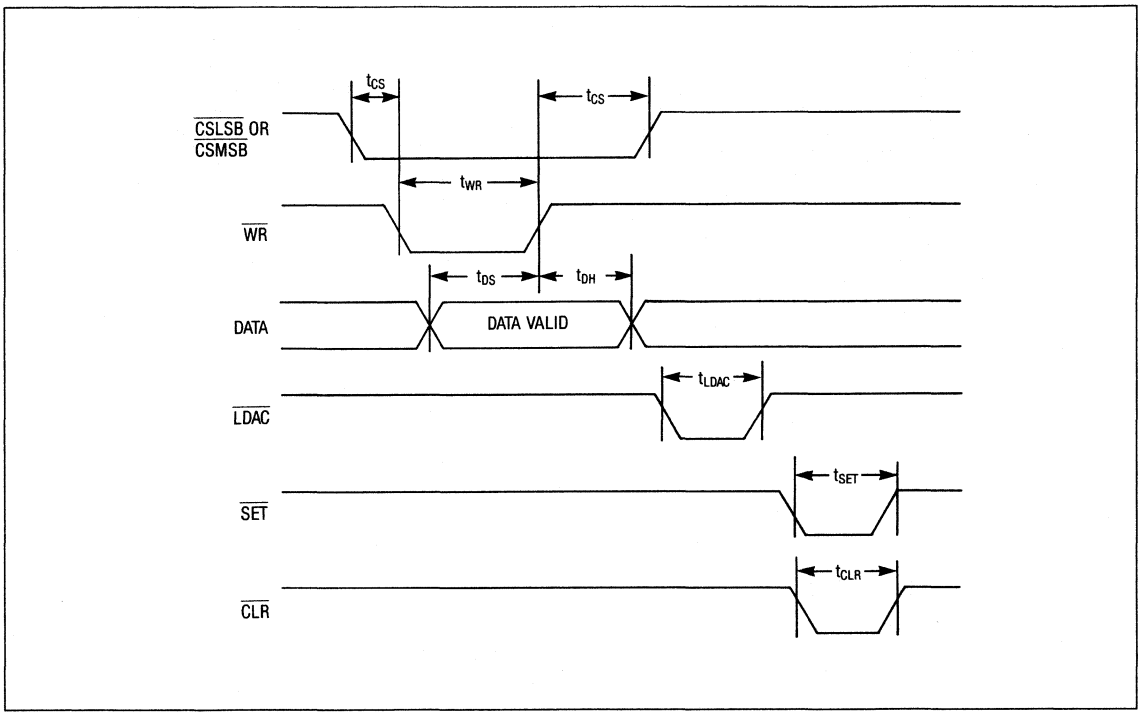


Figure 1a. MAX501 Timing Diagram

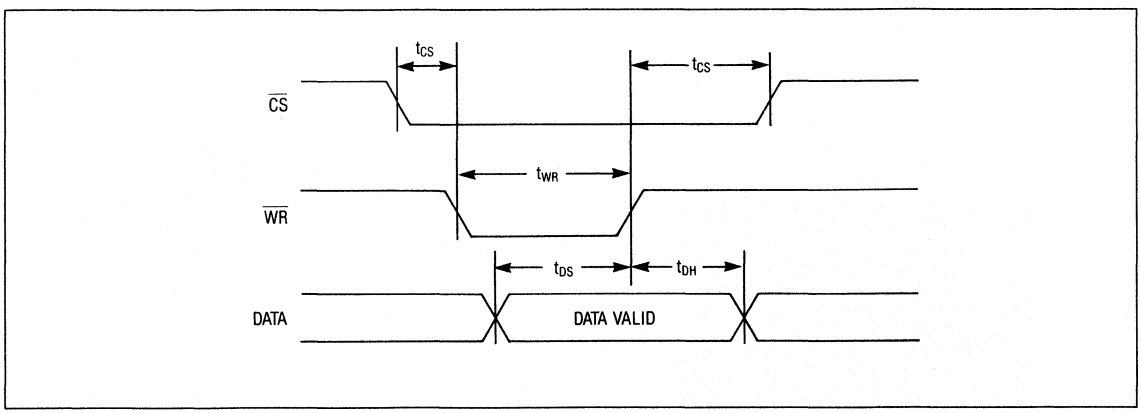


Figure 1b. MAX502 Timing Diagram

NOTES:

1. All input signal rise and fall times measured from 10% to 90% of +5V, $t_R = t_F = 20ns$.
2. Timing measurement reference level is $\frac{V_{IH} + V_{IL}}{2}$

Pin Descriptions

MAX501

PIN	NAME	FUNCTION
1	V_{OUT}	Voltage Output
2	$\overline{LDAC}$	Asynchronous Load DAC Input is active low
3	$\overline{SET}$	Sets DAC register to all 1s
4	$\overline{CLR}$	Sets DAC register to all 0s
5-8	D7-D4	Data Bits 7 to 4
9	D3/D11	Data Bit 3 or 11
10	D2/D10	Data Bit 2 or 10
11	D1/D9	Data Bit 1 or 9
12	DGND	Digital Ground
13	D0/D8	Data Bit 0 or 8 (LSB)
14	$\overline{CSLSB}$	LSB Chip-Select Input is active low
15	$\overline{WR}$	Write Input is active low
16	$\overline{CSMSB}$	MSB Chip-Select Input is active low
17	VREF	Reference Input to DAC
18	AGND	Analog Ground
19	V_{SS}	-12V to -15V Supply Voltage Input
20	V_{DD}	+12V to +15V Supply Voltage Input
21	RA	Scaling Resistor: RA = 4RFB
22	RB	Scaling Resistor: RB = 2RFB
23	RC	Scaling Resistor: RC = 2RFB
24	RFB	Feedback Resistor

MAX502

PIN	NAME	FUNCTION
1	V_{OUT}	Voltage Output
2-11	D11-D2	Data Bits 2 to 11 (MSB)
12	DGND	Digital Ground
13,14	D1, D0	Data Bits 0 to 1 (LSB)
15	$\overline{WR}$	Write Input is active low
16	$\overline{CS}$	Chip-Select Input is active low
17	VREF	Reference Input to DAC
18	AGND	Analog Ground
19	V_{SS}	-12V to -15V Supply Voltage Input
20	V_{DD}	+12V to +15V Supply Voltage Input
21	RA	Scaling Resistor: RA = 4RFB
22	RB	Scaling Resistor: RB = 2RFB
23	RC	Scaling Resistor: RC = 2RFB
24	RFB	Feedback Resistor

Voltage-Output, 12-Bit Multiplying DACs

Detailed Description

Digital Circuit

Figures 2a and 2b are simplified circuit diagrams of the MAX501 and MAX502 input control logic. For the MAX501, a low on $\overline{CSLSB}$ and $\overline{WR}$ with $\overline{CSMSB}$ high loads the least significant bit (LSB) byte into the input register. The LSB byte is then latched into the input register on the rising edge of either a $\overline{WR}$ or a $\overline{CSLSB}$. Similarly, a low on $\overline{CSMSB}$ and $\overline{WR}$ with $\overline{CSLSB}$ high loads the most significant bit (MSB) nibble into the input register. The MSB nibble is then latched into the input register on the rising edge of either a $\overline{WR}$ or a $\overline{CSMSB}$ pulse. With all 12 bits loaded, a low on $\overline{LDAC}$ transfers the data to the DAC register. For the MAX502, a low on $\overline{CS}$ and $\overline{WR}$ transfers the data on the input registers to the DAC latch. Both parts' digital inputs are TTL and CMOS compatible, providing easy microprocessor (μP) interfacing. Tables 1 and 2 are MAX501 and MAX502 truth tables.

Table 1. MAX501 Truth Table

$\overline{WR}$	$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{LDAC}$	$\overline{CLR}$	$\overline{SET}$	OPERATION
X	X	X	X	X	0	DAC Register overridden by 1's Input Register unaffected
X	X	X	X	0	1	DAC Register overridden by 0's Input Register unaffected
0	0	1	1	1	1	Load MSB nibble into Input Register
0	1	0	1	1	1	Load LSB byte into Input Register
X	X	X	0	1	1	Transfer Input Register to DAC Register
1	X	X	1	1	1	No Operation
0	1	1	1	1	1	No Operation
0	R	1	1	1	1	Latching MSB nibble into Input Register
R	0	1	1	1	1	Latching MSB nibble into Input Register
0	1	R	1	1	1	Latching LSB byte into Input Register
R	1	0	1	1	1	Latching LSB byte into Input Register

H = High State, L = Low State, R = Rising Edge, X = Don't Care

Table 2. MAX502 Truth Table

$\overline{WR}$	$\overline{CS}$	OPERATION
H	X	No Operation
X	H	No Operation
L	L	Input Register is Transparent
L	R	Input Register is Latched
R	L	Input Register is Latched

H = High State, L = Low State, R = Rising Edge, X = Don't Care

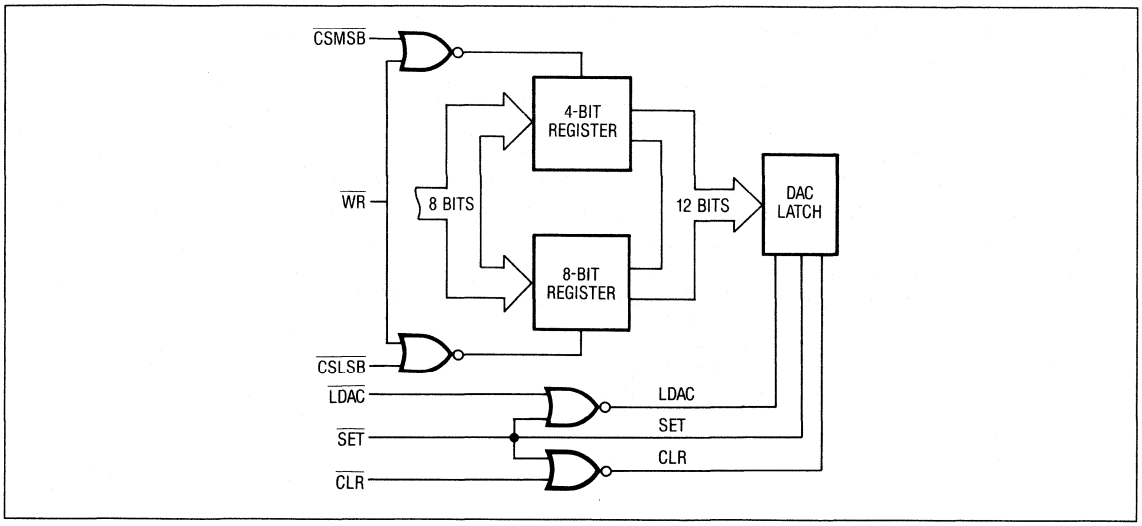


Figure 2a. MAX501 Input Control Logic

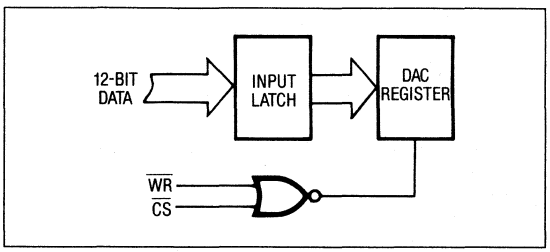


Figure 2b. MAX502 Input Control Logic

Digital-to-Analog Converter

The MAX501/MAX502 have a 12-bit, binary-weighted, current-output DAC with standard R-2R ladder (Figure 3). Binarily weighted currents are switched between AGND and the inverting input of the internal output amplifier. The output amplifier, typically connected to the feedback resistor RFB, converts the output current to a voltage. With RFB connected to V_{OUT},

$$V_{OUT} = -D \times VREF,$$

where D is the fractional expression of the digital input code divided by full scale. D can vary from 0 to 4095/4096 in unipolar mode.

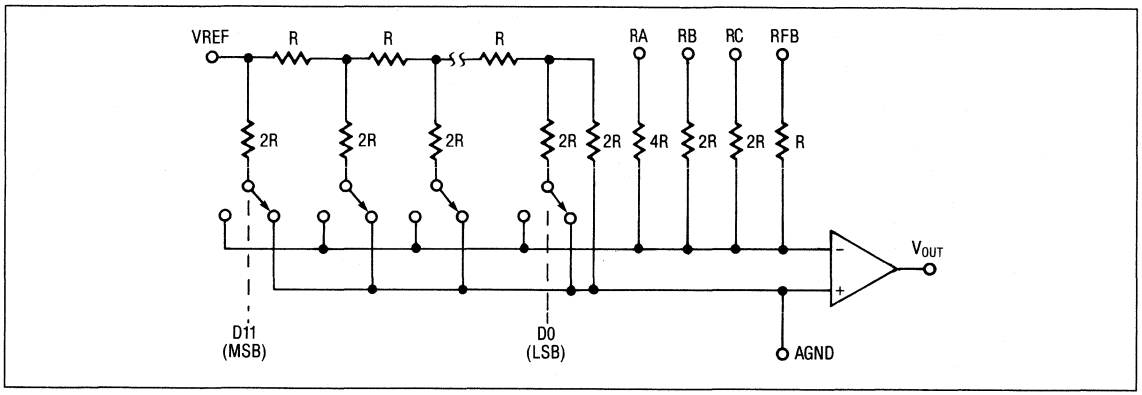


Figure 3. MAX501/MAX502 Simplified DAC and Amplifier Circuit

Voltage-Output, 12-Bit Multiplying DACs

Output-Buffer Amplifier

The output amplifier is an internally compensated, non-inverting, gain-scalable amplifier that can develop ±10V across a 2kΩ load. Maximum settling time is less than 5μs (to within 0.01% FSR). Input offset voltage is laser trimmed at the wafer level. Slew rate is typically 7V/μs. The gain-setting resistors (RA, RB, and RC) connect to the amplifier inverting terminal.

Unipolar Configuration

Figure 4, a typical configuration for the MAX501/502, provides for unipolar-bipolar operation or two-quadrant multiplication when V_{IN} is an AC signal. R1 adjusts gain and R3 adjusts zero offset. For fixed-reference applications, trim the reference voltage and omit R1 and R2. If R1 and R2 are included, you must take into account their gain-temperature coefficient. The typical gain-temperature coefficient of the MAX502 is 1ppm/°C, which corresponds to a gain shift of ½LSB over a +100°C temperature range. Table 3 is the code table for unipolar-binary operation.

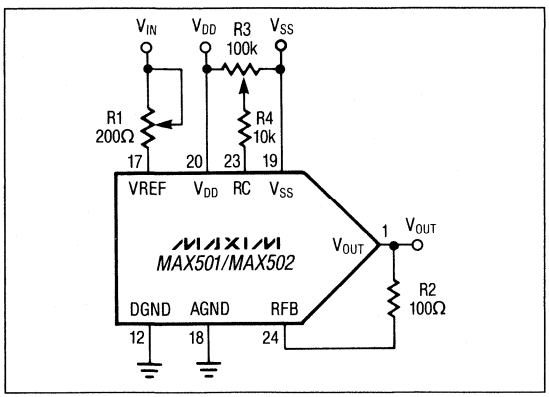


Figure 4. Unipolar-Binary Operation (2-Quadrant Multiplication)

Table 3. MAX501/MAX502 Unipolar-Binary Code Table

DIGITAL INPUT			ANALOG OUTPUT
1111	1111	1111	$(-V_{IN})\frac{4095}{4096}$
1000	0000	0000	$(-V_{IN})\frac{2048}{4096} = -\frac{1}{2}V_{IN}$
0000	0000	0001	$(-V_{IN})\frac{1}{4096}$
0000	0000	0000	0V

Bipolar Operation

Figure 5 shows a 4-quadrant, bipolar operation. Gain error may be adjusted by changing the R1 and R2 ratio. These resistors should be ratio-matched to 0.01% to stay within gain-error specifications and to eliminate trimming. The offset value is defined by matching the RB and RC internal resistors. Table 4 is the code table for bipolar-binary operation.

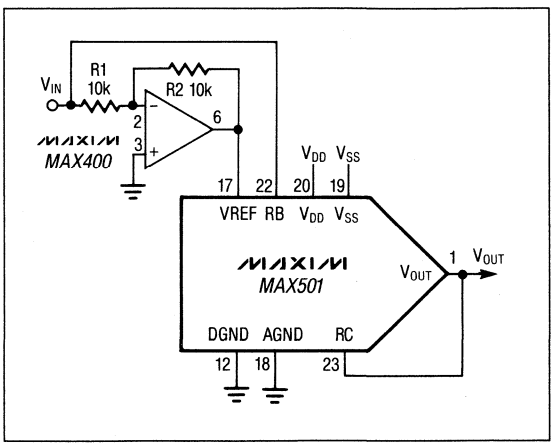


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

Table 4. MAX501/MAX502 Bipolar-Binary Code Table

DIGITAL INPUT			ANALOG OUTPUT
1111	1111	1111	$(+V_{IN})\frac{2047}{2048}$
1000	0000	0001	$(+V_{IN})\frac{1}{2048}$
1000	0000	0000	0V
0111	1111	1111	$(-V_{IN})\frac{1}{2048}$
0000	0000	0000	$(-V_{IN})\frac{2048}{2048} = V_{IN-}$

Applications Information

Noise

AC or transient voltages between AGND and DGND can cause noise injection into the analog output. Tie the MAX502 AGND to DGND to ensure both pins are at the same potential. If these ground pins connect to separate backplanes, use two back-to-back diodes to tie the pins together. Also, decouple V_{DD} and V_{SS} to AGND, as µP-based systems generally have noisy grounds that couple into the power supplies.

Digital Glitches

Any digital word written into the DAC causes a glitch impulse. This impulse couples across the stray capacitance of the DAC switches to the output bus. A glitch impulse on this bus is converted to a voltage by RFB and the output amplifier. The output voltage glitch energy is the product of its duration and its average magnitude (the net area under the curve), and is expressed in (nV)(s). The energy is measured with VREF connected to analog ground and the DAC register alternately loaded with all 0s and all 1s.

Digital Feedthrough

Most of the MAX501/MAX502's digital inputs are directly connected to the µP bus. These inputs are constantly changing, even when the DAC is not selected. High-frequency logic activity on the data bus can feed through the DAC package capacitance as noise on the DAC output. Figure 6 shows an interface that minimizes digital feedthrough. All data inputs are latched from the busy by $\overline{CS}$. Alternatively, using peripheral interface devices reduces digital feedthrough.

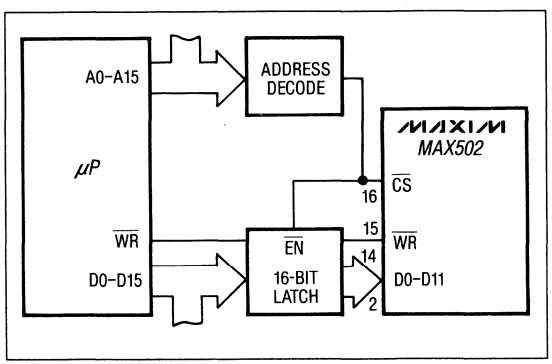


Figure 6. MAX502 Interface Circuit — Latches Minimize Digital Feedthrough

MAX502 Microprocessor Interfacing

16-Bit Microprocessor Systems

Figures 7-9 show the MAX502 interfaced with the MC68000, the 8086, and the TMS32010. The MAX502 appears as a memory-mapped peripheral to the processors. In each case, a write instruction loads the MAX502 with the appropriate data. The particular instructions used are as follows:

MC68000: MOVE
8086: MOV
TMS32010: OUT

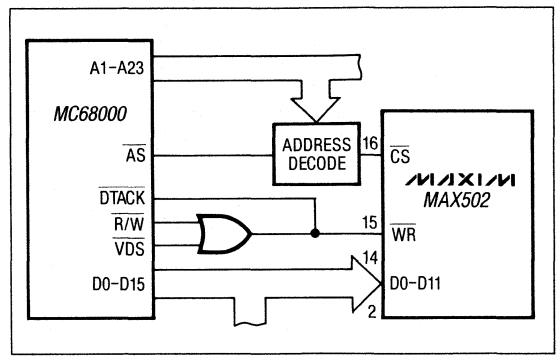


Figure 7. MAX502 to MC6800 Interface

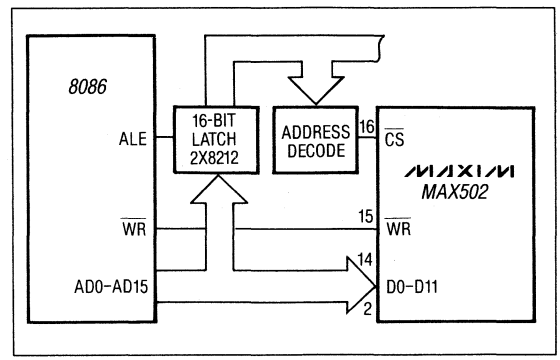


Figure 8. MAX502 to 8086 Interface

Voltage-Output, 12-Bit Multiplying DACs

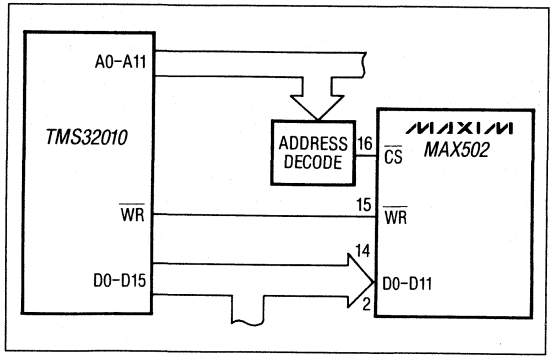


Figure 9. MAX502 to TMS32010 Interface

MAX501 Microprocessor Interfacing

8-Bit Microprocessor Systems

Figure 10 shows an interface circuit for the MAX501 to the 8085A 8-bit μP. The software routine to load data to the device is given in Table 3. Note that transferring 12 data bits requires two write operations. The first of these loads the 4 MSBs into the 7475 latch. The second write operation loads the 8 LSBs plus the 4 MSBs (which are held by the latch) into the DAC.

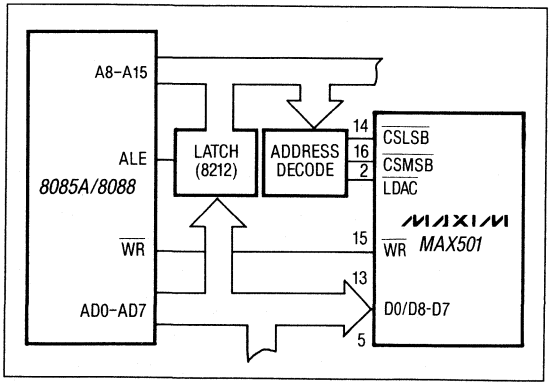
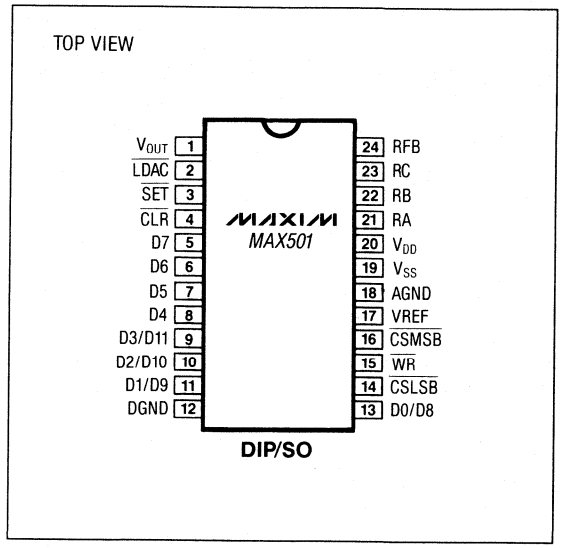


Figure 10. MAX501 to 8085A/8088 Interface

Pin Configurations (continued)



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX502ACNG	0°C to +70°C	24 Narrow Plastic DIP	1/2
MAX502BCNG	0°C to +70°C	24 Narrow Plastic DIP	3/4
MAX502ACWG	0°C to +70°C	24 Wide SO	1/2
MAX502BCWG	0°C to +70°C	24 Wide SO	3/4
MAX502BC/D	0°C to +70°C	Dice*	3/4
MAX502AENG	-40°C to +85°C	24 Narrow Plastic DIP	1/2
MAX502BENG	-40°C to +85°C	24 Narrow Plastic DIP	3/4
MAX502AEWG	-40°C to +85°C	24 Wide SO	1/2
MAX502BEWG	-40°C to +85°C	24 Wide SO	3/4
MAX502AMRG	-55°C to +125°C	24 Narrow CERDIP**	1/2
MAX502BMRG	-55°C to +125°C	24 Narrow CERDIP**	3/4

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

19-0021; Rev 0; 6/92

MAXIM

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

General Description

The MAX505 and MAX506 are CMOS, quad, 8-bit voltage-output digital-to-analog converters (DACs). The parts operate with a single +5V supply or dual ±5V supplies. Internal, precision output buffers swing rail-to-rail. The reference input range includes both supply rails.

Offset, gain, and linearity are factory calibrated to provide 1LSB total unadjusted error (TUE) over the full operating temperature range.

The MAX505 contains double-buffered logic inputs, which allow all analog outputs to be simultaneously updated using the asynchronous load DAC ($\overline{LDAC}$) control signal. The MAX505 also has four separate reference inputs, allowing each DAC's full-scale range to be independently set.

The MAX506 has separate input registers for each of its four DACs. Data is transferred to the input registers from a common 8-bit input port. The DACs are individually selected through address inputs A0 and A1, and updated by bringing $\overline{WR}$ low. All MAX506 DACs share a common reference input.

All logic inputs are TTL and +5V CMOS compatible.

Applications

Minimum Component Count Analog Systems
Digital Offset/Gain Adjustment
Arbitrary Function Generators
Industrial Process Control
Automatic Test Equipment
Programmable Attenuators

Features

- ♦ **Operate from Single +5V Supply or Dual ±5V Supplies**
- ♦ **Output Buffer Amplifiers Swing Rail-to-Rail**
- ♦ **Reference Input Range Includes Both Supply Rails**
- ♦ **Factory-Calibrated for 1LSB TUE**
- ♦ **Double-Buffered Digital Inputs (MAX505)**
- ♦ **Microprocessor and TTL/CMOS Compatible**
- ♦ **Require No External Adjustments**
- ♦ **Pin-Compatible Upgrades to MX7225/MX7226**

Ordering Information

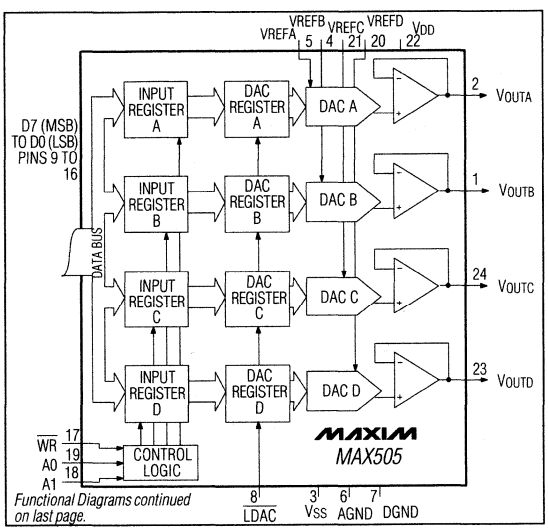
PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSBs)
MAX505ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX505BCNG	0°C to +70°C	24 Narrow Plastic DIP	±11/2
MAX505ACWG	0°C to +70°C	24 Wide SO	±1
MAX505BCWG	0°C to +70°C	24 Wide SO	±11/2
MAX505BC/D	0°C to +70°C	Dice*	±11/2

Ordering Information continued on last page.

** Contact factory for dice specifications.*

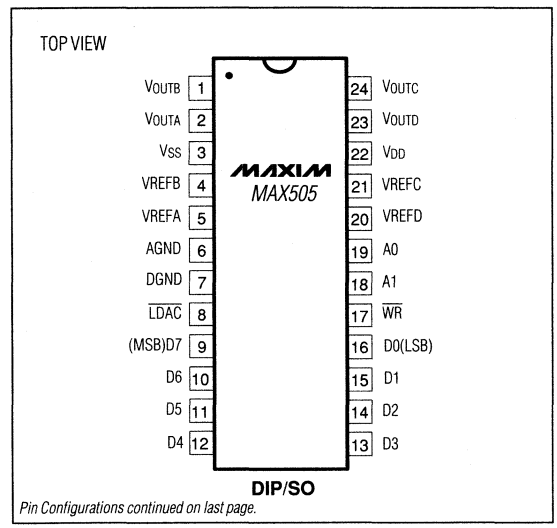
***Contact factory for availability and processing to MIL-STD-883.*

Functional Diagrams



Functional Diagrams continued on last page.

Pin Configurations



Pin Configurations continued on last page.

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +8V
V_{DD} to DGND ..... -0.3V, +6V
V_{SS} to AGND ..... -7V, 0.3V
V_{SS} to DGND ..... -7V, 0.3V
V_{DD} to V_{SS} ..... -0.3V, +12V
Digital Input Voltage to DGND ..... -0.3V, (V_{DD} + 0.3V)
VREF ..... (V_{SS} - 0.3V), (V_{DD} + 0.3V)
V_{OUT} (Note 1) ..... V_{SS}, V_{DD}
Continuous Power Dissipation (T_A = +70°C)
MAX505
Plastic DIP (derate 13.33mW/°C above +70°C) 1067mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
CERDIP (derate 12.50mW/°C above +70°C) 1000mW
MAX506
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 10.00mW/°C above +70°C) 800mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX50__C__ ..... 0°C to +70°C
MAX50__E__ ..... -40°C to +85°C
MAX50__M__ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The outputs may be shorted to V_{DD}, V_{SS}, or AGND if the package power dissipation is not exceeded. Typical short-circuit current to AGND is 50mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, AGND = DGND = 0V, VREF = 4V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC ACCURACY							
Resolution				8			Bits
Total Unadjusted Error	TUE	VREF = +4V, V_{SS} = 0V or -5V ±10%	MAX50_A			±1	LSB
			MAX50_B			±11/2	
		VREF = -4V, V_{SS} = -5V ±10%	MAX50_A			±1	
			MAX50_B			±11/2	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Zero-Code Error	ZCE	Code = 00 hex, V_{SS} = 0V	MAX50_C			14	mV
			MAX50_E			16	
			MAX50_M			20	
		Code = 00 hex, V_{SS} = -5V ±10%	MAX50_C			±14	
			MAX50_E			±16	
			MAX50_M			±20	
Zero-Code Error Supply Rejection		Code = 00 hex, V_{DD} = 5V ±10%, V_{SS} = 0V or -5V ±10%			1	2	mV
Zero-Code Temperature Coefficient		Code = 00 hex			±10		µV/°C
Full-Scale Error		Code = FF hex				±14	mV
Full-Scale Error Supply Rejection		Code = 00 hex, V_{DD} = +5V ±10%, V_{SS} = 0V or -5V ±10%	MAX50_C		1	2	mV
			MAX50_E		1	2	
			MAX50_M			10	
Full-Scale-Error Temperature Coefficient		Code = FF hex			±10		µV/°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, AGND = DGND = 0V, VREF = 4V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUTS							
Input Voltage Range				V_{SS}		V_{DD}	V
Input Resistance (Note 2)		Code = 55 hex	MAX505	16	24		kΩ
			MAX506	4	6		
Input Capacitance (Note 3)		Code = 00 hex	MAX505		15		pF
			MAX506		40		
Channel-to-Channel Isolation		MAX505 (Note 4)			-60		dB
AC Feedthrough		MAX505 (Note 5)			-70		dB
DAC OUTPUTS							
Full-Scale Output Voltage				V_{SS}		VDD	V
Resistive Load		VREF = 4V, load regulation ≤ 1/4LSB		2			kΩ
		VREF = -4V, V_{SS} = -5V ±10%, load regulation ≤ 1/4LSB		2			
		VREF = V_{DD} MAX50__C/E load regulation ≤ 1LSB		10			
		VREF = V_{DD} MAX50_M load regulation ≤ 2LSB		10			
DIGITAL INPUTS							
Logic High	V_{IH}			2.4			V
Logic Low	V_{IL}					0.8	V
Input Current		Measured at V_{IH} and V_{IL}				±1	µA
Input Capacitance					8		pF
Input Coding				Binary			
DYNAMIC PERFORMANCE							
Voltage-Output Slew Rate		Positive and negative	MAX50_C	1.0			V/µs
			MAX50_E	0.7			
			MAX50_M	0.5			
Output Settling Time		To ±1/2LSB, 10kΩ I I 100pF load (Note 6)			6		µs
Digital Feedthrough		Code = 00 hex, $\overline{WR}$ = V_{DD}, all digital inputs from 0V to V_{DD}			5		nV-s
Signal to (Noise + Distortion) Ratio		VREF = 4Vp-p at 1kHz, V_{DD} = 5V, V_{SS} = -5V, code = FF hex		-87			dB
		VREF = 4Vp-p at 20kHz, V_{SS} = -5V ±10%			-74		dB
Multiplying Bandwidth		VREF = 0.5Vp-p, 3dB bandwidth			1		MHz
Wideband Amplifier Noise					60		µV RMS

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

ELECTRICAL CHARACTERISTICS (continued)

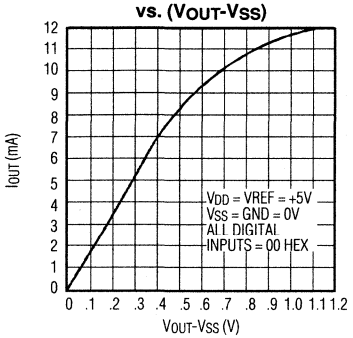
(V_{DD} = +5V ±10%, V_{SS} = 0V to -5.5V, AGND = DGND = 0V, VREF = 4V, R_L = 10kΩ, C_L = 100pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Positive Supply Voltage	V_{DD}	For specified performance		4.5		5.5	V
Negative Supply Voltage	V_{SS}	For specified performance		-5.50		0	V
Positive Supply Current	I_{DD}	Outputs unloaded, all digital inputs = 0V or VDD	MAX50__C/E		5	10	mA
			MAX50_M		5	12	
Negative Supply Current	I_{SS}	VSS = -5V ±10%, outputs unloaded, all digital inputs = 0V or V_{DD}	MAX50__C/E		5	10	mA
			MAX50_M		5	12	
SWITCHING CHARACTERISTICS							
Address to $\overline{WR}$ Setup	t_{AS}			5	-8		ns
Address to $\overline{WR}$ Hold	t_{AH}			5	-4		ns
Data to $\overline{WR}$ Setup	t_{DS}			45	35		ns
Data to $\overline{WR}$ Hold	t_{DH}			0	-13		ns
$\overline{WR}$ Pulse Width	t_{WR}			40	20		ns
$\overline{LDAC}$ Pulse Width	t_{LC}			40	20		ns

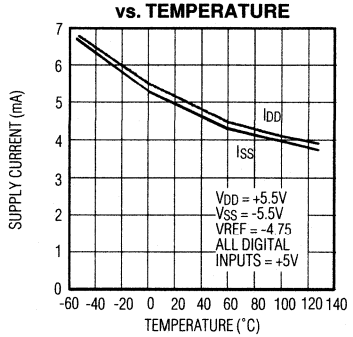
Note 2: Input resistance is code dependent. The lowest input resistance occurs at code = 55 hex.
Note 3: Input capacitance is code dependent. The highest input capacitance occurs at code = 00 hex.
Note 4: VREF = 10kHz, 4Vp-p. Channel-to-channel isolation is measured by setting the code of one DAC to FF hex and setting the code of all other DACs to 00 hex.
Note 5: VREF = 10kHz, 4Vp-p. DAC code = 00 hex.
Note 6: Output settling time is measured by taking the code from 00 hex to FF hex, and from FF hex to 00 hex.

Typical Operating Characteristics

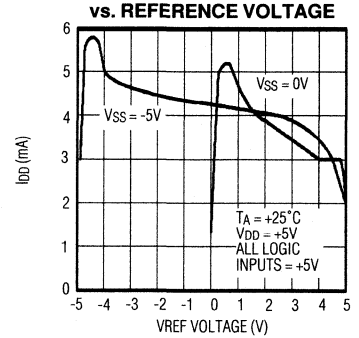
OUTPUT SINK CURRENT vs. (V_{OUT}-V_{SS})



SUPPLY CURRENT vs. TEMPERATURE

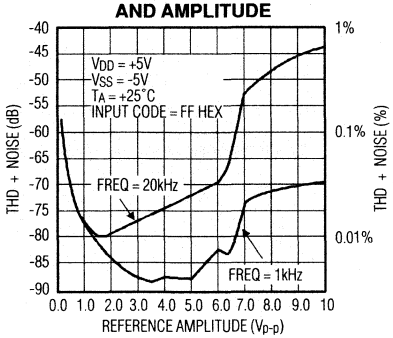


SUPPLY CURRENT vs. REFERENCE VOLTAGE

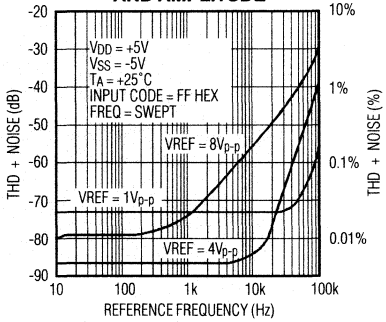


Typical Operating Characteristics (continued)

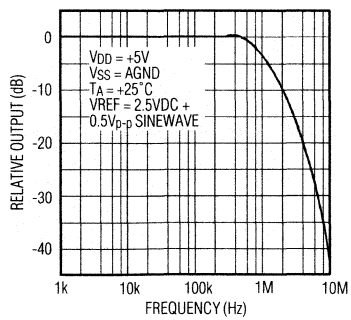
THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY AND AMPLITUDE



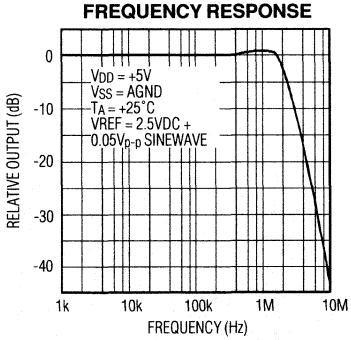
THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY AND AMPLITUDE



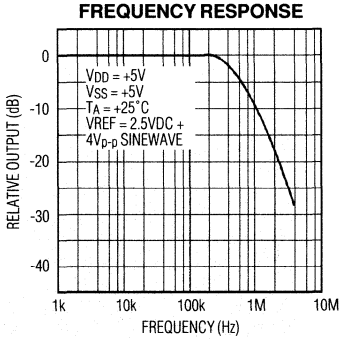
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



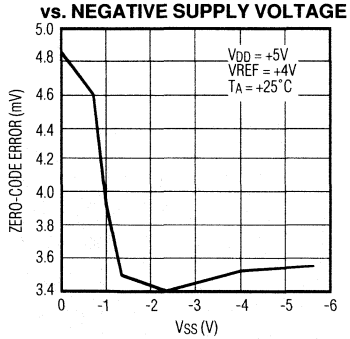
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



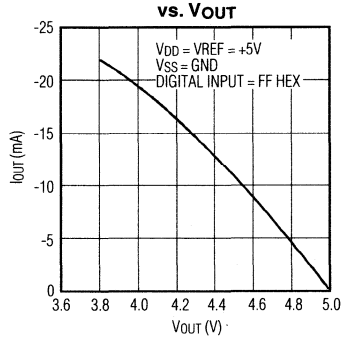
REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



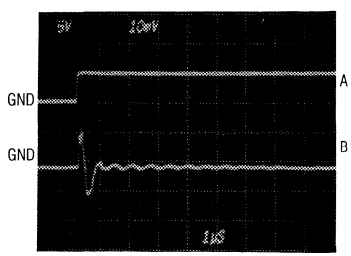
ZERO-CODE ERROR vs. NEGATIVE SUPPLY VOLTAGE



OUTPUT SOURCE CURRENT vs. VOUT



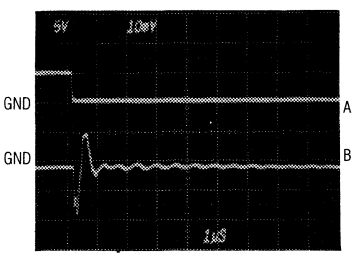
DIGITAL FEEDTHROUGH – GLITCH IMPULSE (0 TO 1 DIGITAL TRANSITION)



A = DIGITAL INPUTS, 5V/div
B = VOUTA, 10mV/div
TIMEBASE = 1µs

0 TO 1 DIGITAL TRANSITION ON ALL DATA BITS (WITH $\overline{WR}$ HIGH)
VREFA = AGND

DIGITAL FEEDTHROUGH – GLITCH IMPULSE (1 TO 0 DIGITAL TRANSITION)



A = DIGITAL INPUTS, 5V/div
B = VOUTA, 10mV/div
TIMEBASE = 1µs

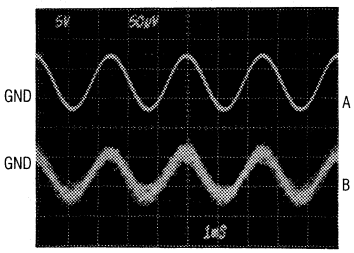
1 TO 0 DIGITAL TRANSITION ON ALL DATA BITS (WITH $\overline{WR}$ HIGH)
VREFA = AGND

9

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

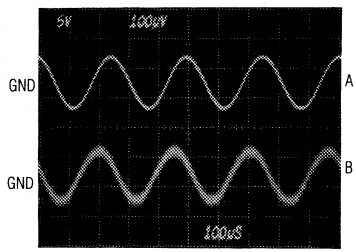
Typical Operating Characteristics (continued)

REFERENCE FEEDTHROUGH AT 400Hz



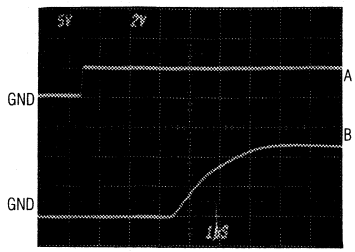
A = VREFA, 10V_{P-P}
B = V_{OUTA}, 50µV/div, UNLOADED
TIMEBASE = 1ms/div
V_{DD} = +5V
V_{SS} = -5V
CODE = ALL 0s
LOAD = ∞

REFERENCE FEEDTHROUGH AT 4000Hz



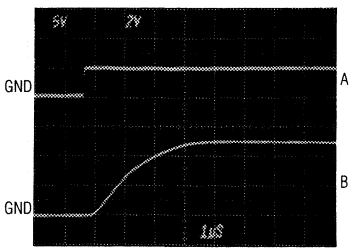
A = VREFA, 10V_{P-P}
B = V_{OUTA}, 100µV/div, UNLOADED
TIMEBASE = 100µs/div
V_{DD} = +5V
V_{SS} = -5V
CODE = ALL 0s
LOAD = ∞

POSITIVE SETTLING TIME (V_{SS} = AGND)



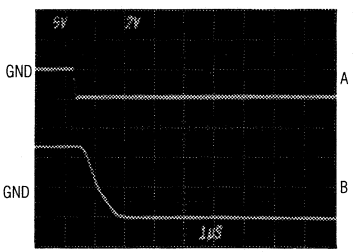
A = DIGITAL INPUT, 5V/div
B = V_{OUTA}, 2V/div
TIMEBASE = 1µs
V_{DD} = +5V
VREFA = +5V
ALL BITS OFF TO ALL BITS ON
R_L = 10kΩ, C_L = 100pF

POSITIVE SETTLING TIME (V_{SS} = -5V)



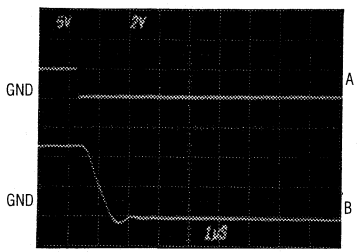
A = DIGITAL INPUT, 5V/div
B = V_{OUTA}, 2V/div
TIMEBASE = 1µs
V_{DD} = +5V
VREFA = +5V
ALL BITS OFF TO ALL BITS ON
R_L = 10kΩ, C_L = 100pF

NEGATIVE SETTLING TIME (V_{SS} = AGND)



A = DIGITAL INPUT, 5V/div
B = V_{OUTA}, 2V/div
TIMEBASE = 1µs
V_{DD} = +5V
VREFA = +5V
ALL BITS ON TO ALL BITS OFF
R_L = 10kΩ, C_L = 100pF

NEGATIVE SETTLING TIME (V_{SS} = -5V)



A = DIGITAL INPUT, 5V/div
B = V_{OUTA}, 2V/div
TIMEBASE = 1µs
V_{DD} = +5V
VREFA = +5V
ALL BITS ON TO ALL BITS OFF
R_L = 10kΩ, C_L = 100pF

Pin Description

PIN		NAME	FUNCTION
MAX505	MAX506		
1	1	V_{OUTB}	DAC B Output Voltage
2	2	V_{OUTA}	DAC A Output Voltage
3	3	V_{SS}	Negative Power Supply
4		VREFB	Reference Voltage Input for DAC B
	4	VREF	Reference Voltage Input for DAC A to DAC D
5		VREFA	Reference Voltage Input for DAC A
6	5	AGND	Analog Ground
7	6	DGND	Digital Ground
8		$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low transfers the contents of each input register to its respective DAC register.
9	7	D7	Data Bit 7 (MSB)
10	8	D6	Data Bit 6
11	9	D5	Data Bit 5
12	10	D4	Data Bit 4
13	11	D3	Data Bit 3
14	12	D2	Data Bit 2
15	13	D1	Data Bit 1
16	14	D0	Data Bit 0 (LSB)
17	15	$\overline{WR}$	Write Input (active low). Used to load data into the DAC input register selected by A0 and A1.
18	16	A1	DAC Address select bit (MSB)
19	17	A0	DAC Address select bit (LSB)
20		VREFD	Reference Voltage Input for DAC D
21		VREFC	Reference Voltage Input for DAC C
22	18	V_{DD}	Positive Supply Voltage
23	19	V_{OUTD}	DAC D Output Voltage
24	20	V_{OUTC}	DAC C Output Voltage

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

Detailed Description

Digital-to-Analog Section

The MAX505/MAX506 contain four matched voltage-output DACs. The DACs are inverted R-2R ladder networks that convert 8-bit digital words into equivalent analog output voltages in proportion to the applied reference voltage(s). Each DAC in the MAX505 has a separate reference input, while all four DACs in the MAX506 share a common reference input. Figure 1 shows a simplified functional diagram of one of the DACs.

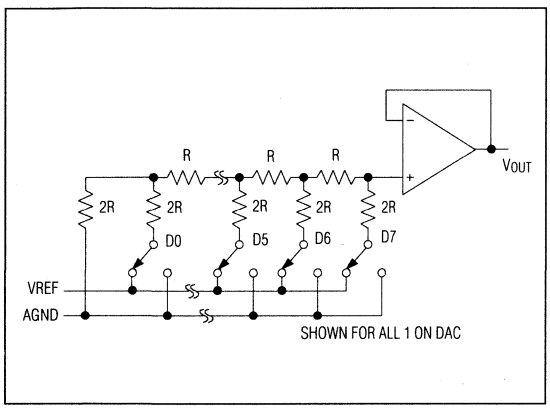


Figure 1. DAC Simplified Circuit Diagram

Power Supplies and Reference Input

The MAX505/MAX506 can be used for multiplying applications. The reference accepts both DC and AC signals. The voltage at each VREF input sets the full-scale output voltage for its respective DAC. The VREF input impedance is code dependent, with the lowest value (16kΩ for the MAX505 and 4kΩ for the MAX506) occuring when the input code is 55 hex. The maximum value, essentially infinity, occurs when the input code is 00 hex. Since the VREF input impedance is code dependent, the DACs' reference sources must have a low output impedance (no more than 32Ω for the MAX505 and 8Ω for the MAX506) to maintain output linearity. The VREF input capacitance is also code dependent: 15pF maximum for the MAX505 and 40pF maximum for the MAX506.

The output voltage for any DAC can be represented by a digitally programmable voltage source as:

$$V_{OUT} = (N_B \times VREF) / 256$$

where N_B is the numeric value of the DAC's binary input code.

Output Buffer Amplifiers

All MAX505/MAX506 voltage outputs are internally buffered by precision unity-gain followers that slew at 1V/µs. With a 0V to +4V (or +4V to 0V) output transition, the amplifier outputs will settle to 1/2LSB in typically 6µs when loaded with 10kΩ in parallel with 100pF.

The buffer amplifiers are stable with any combination of resistive loads ≥ 2kΩ and capacitive loads ≤ 300pF.

Digital Inputs and Interface Logic

The digital inputs are compatible with both TTL and 5V CMOS logic. However, the power-supply current (I_{DD}) depends on the input logic levels. Supply current is specified for CMOS input levels (best case). Supply current increases by about 2mA when driven with TTL logic levels.

Address lines A0 and A1 select which DAC receives data from the data bus as shown in Table 1. When $\overline{WR}$ is low, the addressed DAC's input register is transparent. Data is latched into the input register on $\overline{WR}$'s rising edge. Figure 2 shows the MAX505/MAX506 input control logic.

The MAX506 DAC outputs represent the data held in the four 8-bit input registers. The MAX505 has double-buffered inputs; in addition to the input registers, there are individual DAC registers (see *Functional Diagrams*).

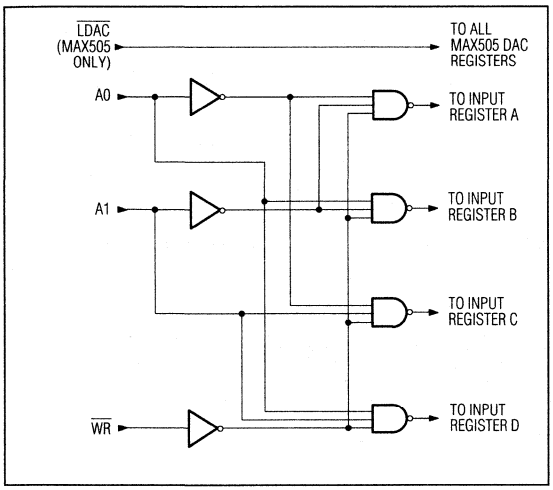


Figure 2. MAX505/MAX506 Input Control Logic

In the MAX505, data is transferred from the input registers to the DAC registers by pulling the $\overline{LDAC}$ control input low. This operation also initiates a conversion in each of the four DACs and simultaneously updates all four outputs. Since $\overline{LDAC}$ is asynchronous with respect to $\overline{WR}$, be sure that incorrect data is not latched to the output. Data is latched into all four DAC registers on $\overline{LDAC}$'s rising edge. Table 1a is the write-cycle truth table for the MAX505. Table 1b is the write-cycle truth table for the MAX506. Figure 3 shows the MAX505/MAX506 write-cycle timing. If simultaneous updating is not required, tie $\overline{LDAC}$ low to keep the second latch transparent.

On power-up, all MAX505/MAX506 registers are internally preset with all 0s.

Table 1a. MAX505 DAC Addressing (partial list)

$\overline{LDAC}$	$\overline{WR}$	A1	A0	OPERATION
H	H	X	X	No operation
H	L	L	L	DAC A input register transparent
H	R	L	L	DAC A input register latched
L	H	X	X	All 4 DAC's DAC registers transparent
L	L	L	L	DAC A input registers transparent and all 4 DAC's DAC registers transparent
R	H	X	X	All 4 DAC's DAC registers latched
H	L	L	H	DAC B input register transparent
H	L	H	L	DAC C input register transparent
H	L	H	H	DAC D input register transparent

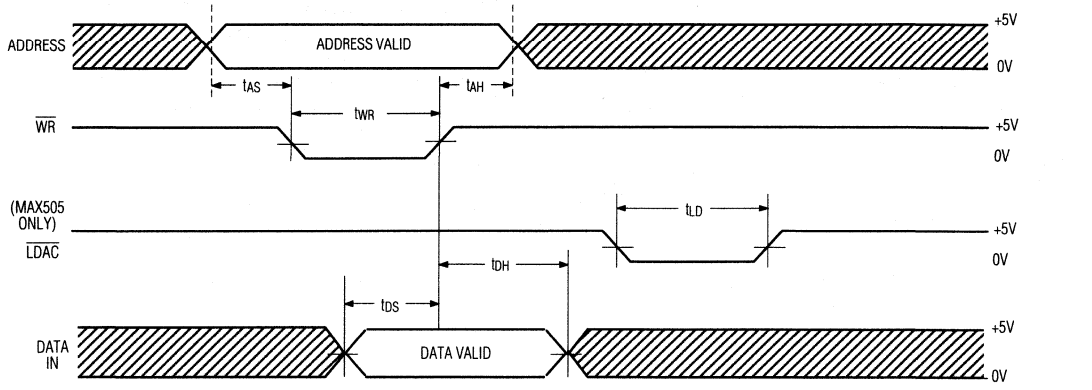
H = High State, L = Low State, X = Don't Care, R = Rising Edge

Table 1b. MAX506 DAC Addressing (partial list)

$\overline{WR}$	A1	A0	OPERATION
H	X	X	No operation
L	L	L	DAC A input register transparent
R	L	L	DAC A input register latched
L	L	H	DAC B input register transparent
L	H	L	DAC C input register transparent
L	H	H	DAC D input register transparent

H = High State, L = Low State, X = Don't Care, R = Rising Edge

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs



NOTES:
ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V, $t_r = t_f = 5ns$ OVER V_{DD} RANGE.
TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{INH} + V_{INL}}{2}$
IF $\overline{LDAC}$ (MAX505 ONLY) IS ACTIVATED PRIOR TO $\overline{WR}$'S RISING EDGE, IT MUST STAY LOW FOR t_{LD} (OR LONGER) AFTER $\overline{WR}$ GOES HIGH.

Figure 3. MAX505/MAX506 Write-Cycle Timing Diagram

Applications Information

Power Supply and Reference Operating Ranges

The MAX505/MAX506 are fully specified to operate with V_{DD} = 5V ±5% and V_{SS} = 0V to -5.5V. 8-bit performance is guaranteed for both single- and dual-supply operation. The zero-code output error is guaranteed to be less than 14mV when operating from a single +5V supply.

The DACs work well with reference voltages from V_{SS} to V_{DD}.

V_{SS} should never be more positive than either AGND or DGND. No input should be more positive than V_{DD}.

Power-Supply Bypassing and Ground Management

In single-supply operation (AGND = DGND = V_{SS} = 0V), AGND, DGND, and V_{SS} should be connected together in a "star" ground at the chip. This ground should then return to the highest quality ground available. Bypass V_{DD} with a 0.1µF capacitor, located as close to V_{DD} and AGND as possible.

In dual-supply operation, where DGND = AGND, V_{DD} and V_{SS} should be bypassed with 0.1µF capacitors to AGND. These capacitors should be placed as close to the supply pins as possible. To minimize digital noise on AGND, DGND and AGND should have separate return paths to the highest quality ground available.

Careful PCB layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Figures 4 and 5 show suggested circuit board layouts to minimize crosstalk.

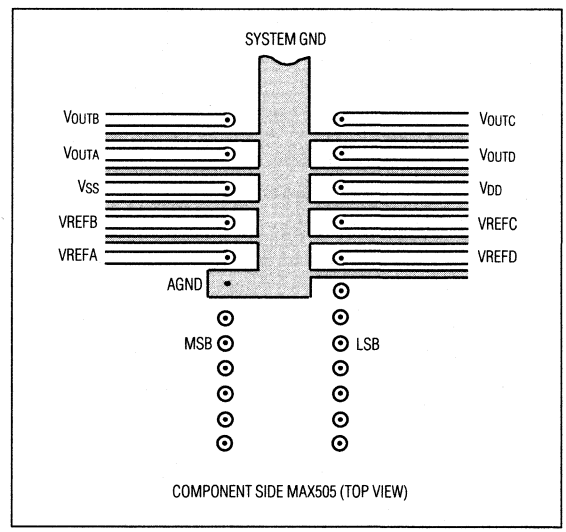


Figure 4. Suggested MAX505 PCB Layout for Minimizing Crosstalk

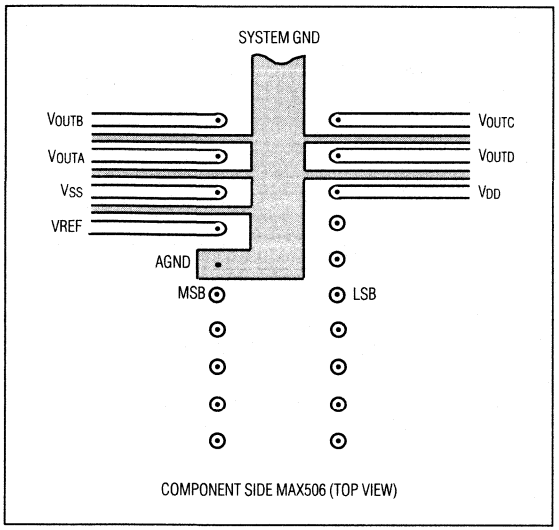


Figure 5. Suggested MAX506 PCB Layout for Minimizing Crosstalk

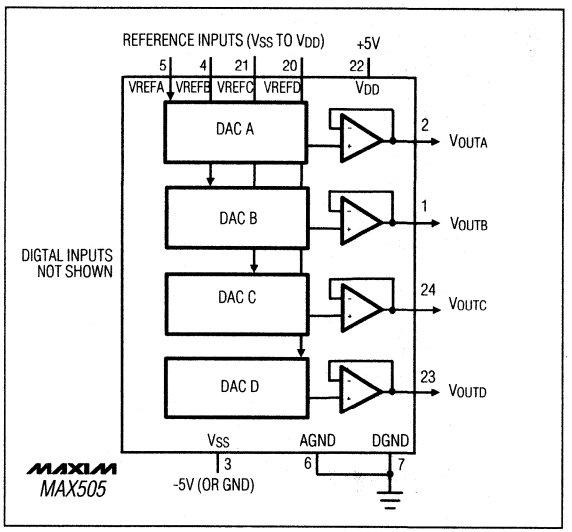


Figure 6. MAX505 Unipolar Output Circuit

Unipolar Output, 2-Quadrant Multiplication

In unipolar operation, the output voltages and the reference input(s) are the same polarity. Figures 6 and 7 show the MAX505/MAX506 unipolar configurations. If the reference inputs are positive, both devices can be operated from a single supply. If dual supplies are used, the reference input can vary from V_{SS} to V_{DD}. Table 2 is the unipolar code table.

Bipolar Output, 2-Quadrant Multiplication

Bipolar output 2-quadrant multiplication is achieved by offsetting AGND positively or negatively.

Offsetting AGND Positively - Single or Dual Supplies

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a 0 input code, as shown in Figure 8. The output voltage at V_{OUTA} is:

$$V_{OUTA} = VBIAS + (N_B/256)(V_{IN}),$$

where N_B represents the digital input word. Since AGND is common to all four DACs, all outputs will be offset by VBIAS in the same manner. AGND should not be biased more than +1V above DGND.

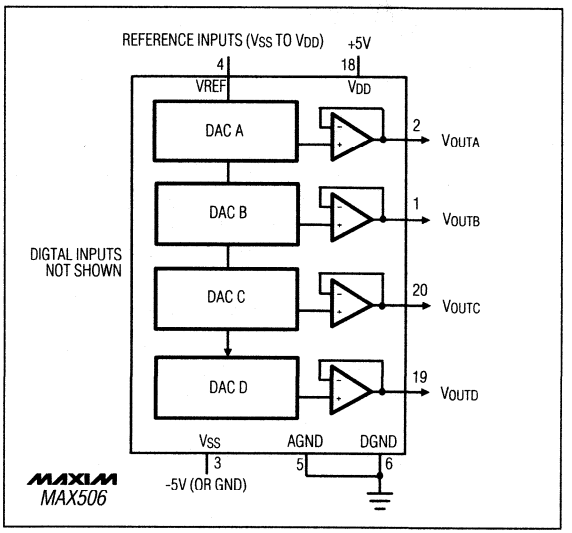


Figure 7. MAX506 Unipolar Output Circuit

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

Table 2. Unipolar Code Table

DAC CONTENTS MSB	DAC CONTENTS LSB	ANALOG OUTPUT
1111	1111	$+VREF\left(\frac{255}{256}\right)$
1000	0001	$+VREF\left(\frac{129}{256}\right)$
1000	0000	$+VREF\left(\frac{128}{256}\right) = +\frac{VREF}{2}$
0111	1111	$+VREF\left(\frac{127}{256}\right)$
0000	0001	$+VREF\left(\frac{1}{256}\right)$
0000	0000	0V

Note: $1LSB = (VREF)(2^{-8}) = +VREF\left(\frac{1}{256}\right)$

Table 3. Bipolar Code Table

DAC CONTENTS MSB	DAC CONTENTS LSB	ANALOG OUTPUT
1111	1111	$VREF\left(\frac{127}{128}\right)$
1000	0001	$VREF\left(\frac{1}{128}\right)$
1000	0000	0V
0111	1111	$-VREF\left(\frac{1}{128}\right)$
0000	0001	$-VREF\left(\frac{127}{128}\right)$
0000	0000	$-VREF\left(\frac{128}{128}\right) = -VREF$

Offsetting AGND Negatively - Dual Supplies

An alternate method of generating bipolar outputs uses Figure 9's circuits. In these circuits, AGND is biased negatively (up to -2.5V with respect to DGND) to provide an arbitrary negative output voltage for a 0 input code. The output voltage at V_{OUTA} is:

$$V_{OUTA} = -(R2/R1)(2.5V) + (N_B/256)(2.5V)(R2/R1 + 1)$$

where N_B represents the digital input word. Since AGND is common to all four DACs, all outputs will be offset by VBIAS in the same manner. Table 3, with VREF = 2.5V, shows the digital code vs. output voltage for Figure 9's circuits with R1 = R2.

4-Quadrant Multiplication

Each DAC output may be configured for 4-quadrant multiplication using Figure 10's circuit. One op amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = VREF\,[(2)(N_B/256) - 1],$$

where N_B represents the digital word in DAC register A.

Recommended values for resistors R1 and R2 are 330k (±0.1%). Table 3 shows the digital code vs. output voltage for Figure 10's circuit.

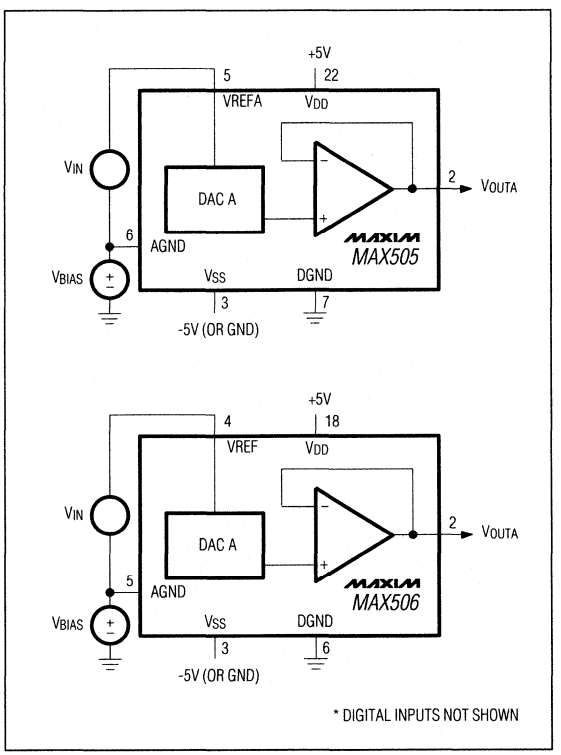


Figure 8. AGND Bias Circuits (Positive Offset)

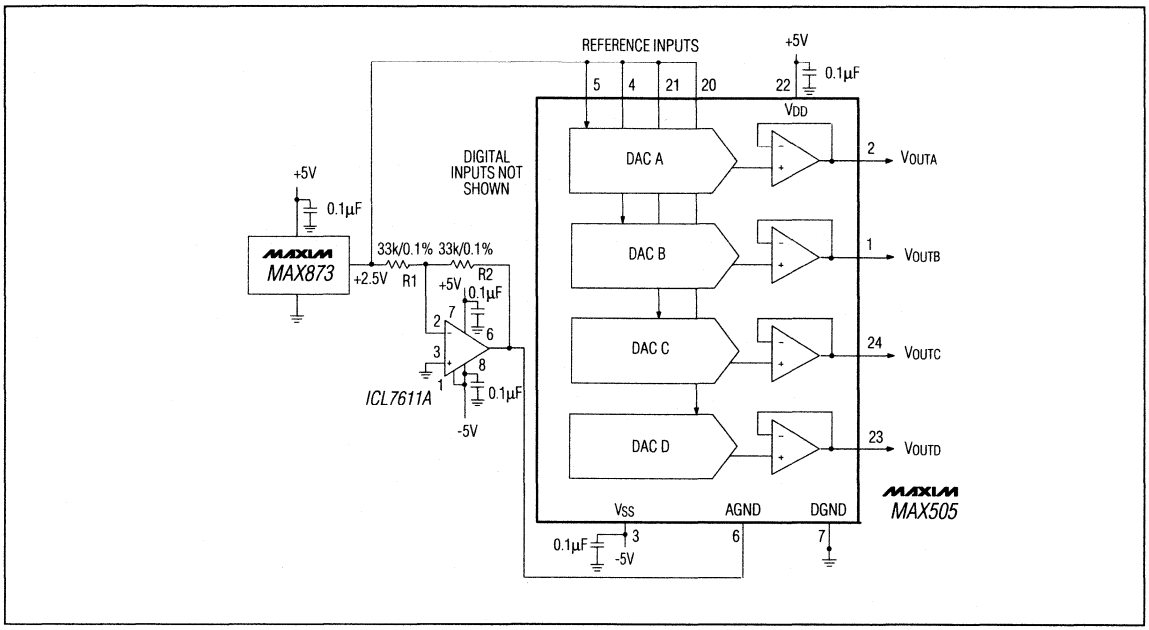


Figure 9a. MAX505 AGND Bias Circuit (Negative Offset)

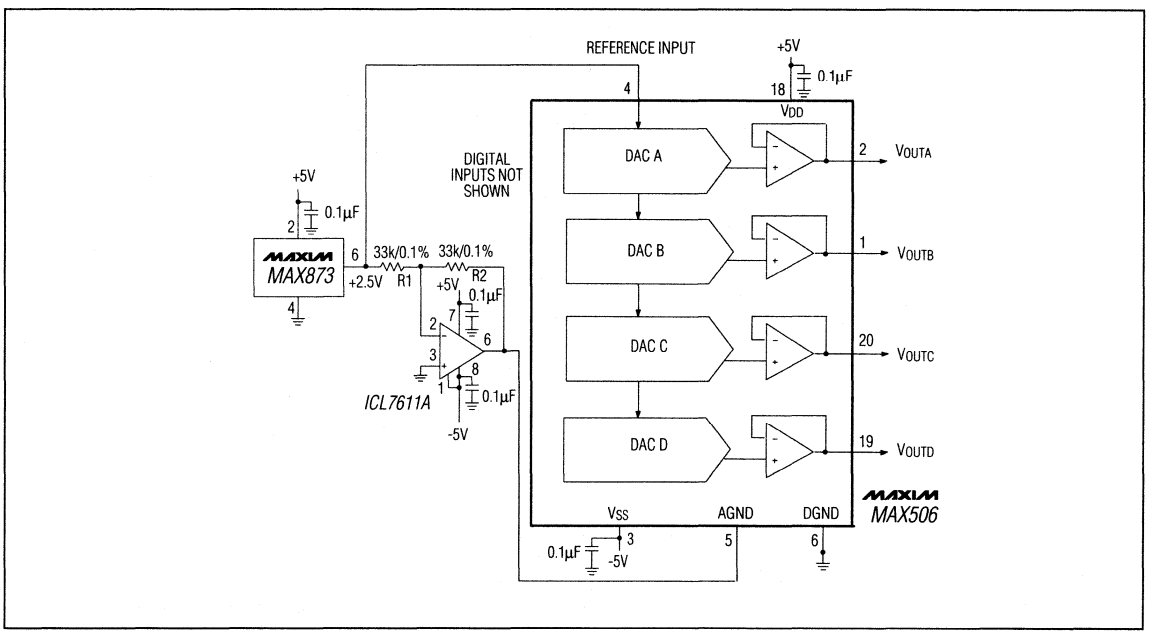


Figure 9b. MAX506 AGND Bias Circuit (Negative Offset)

9

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

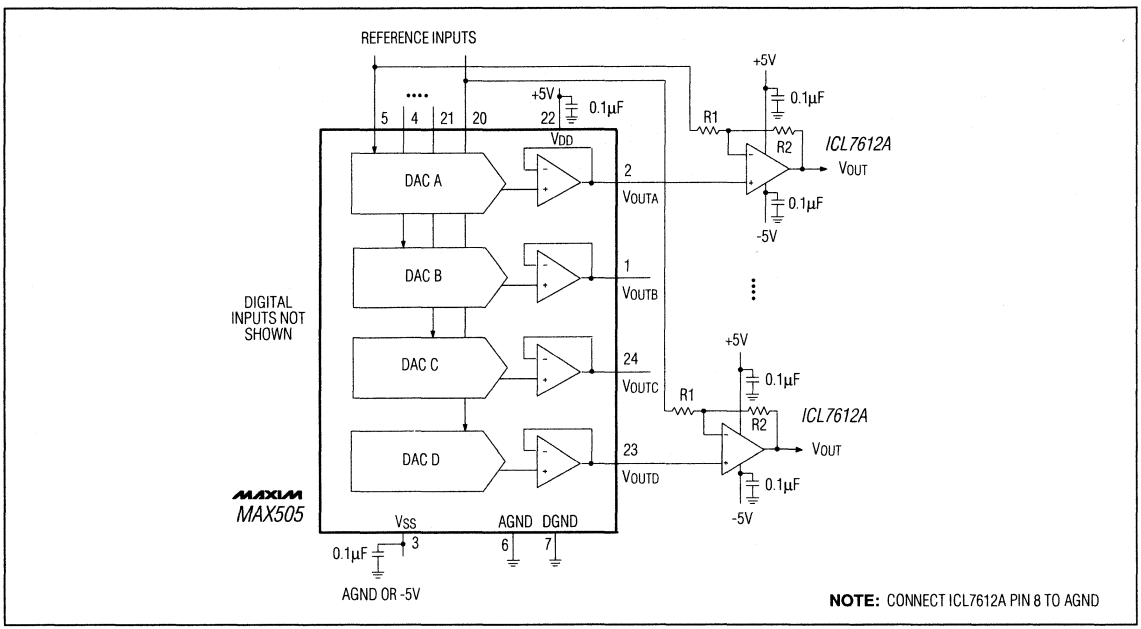


Figure 10a. MAX505 Bipolar Output Circuit

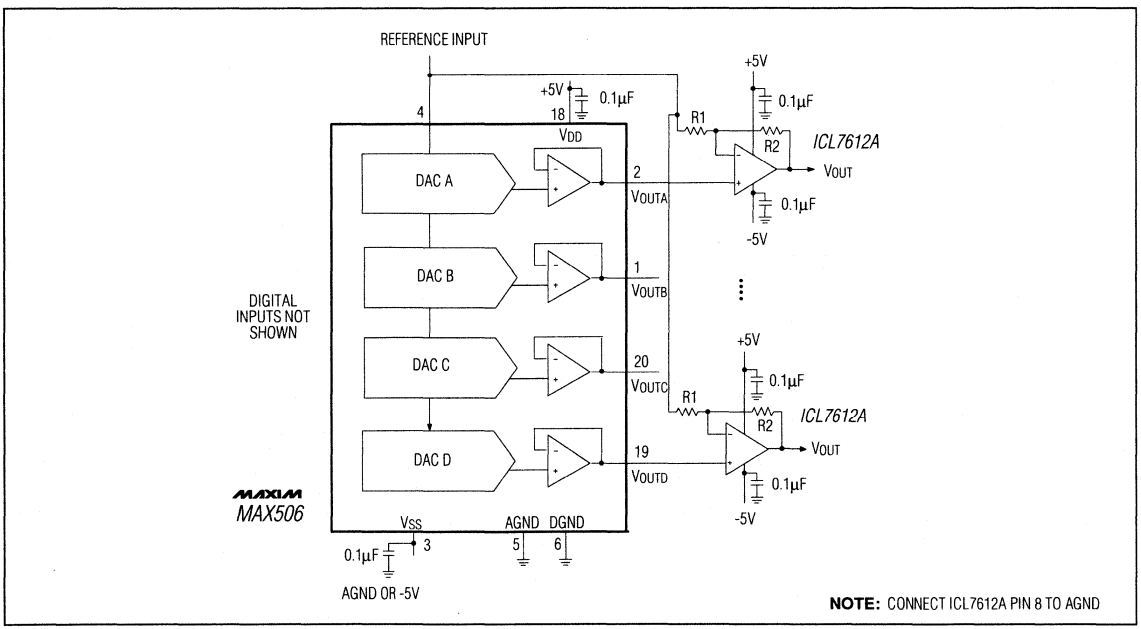
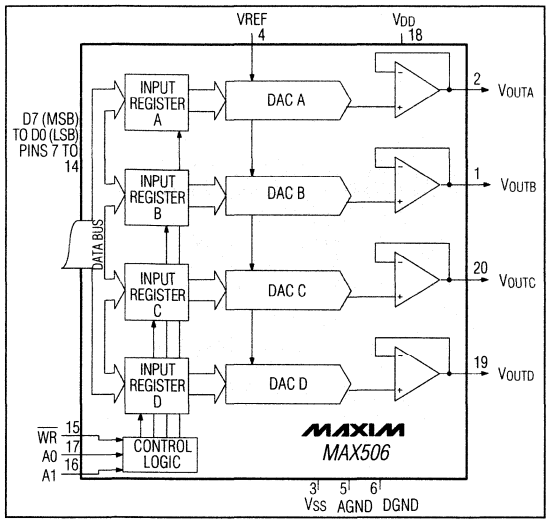


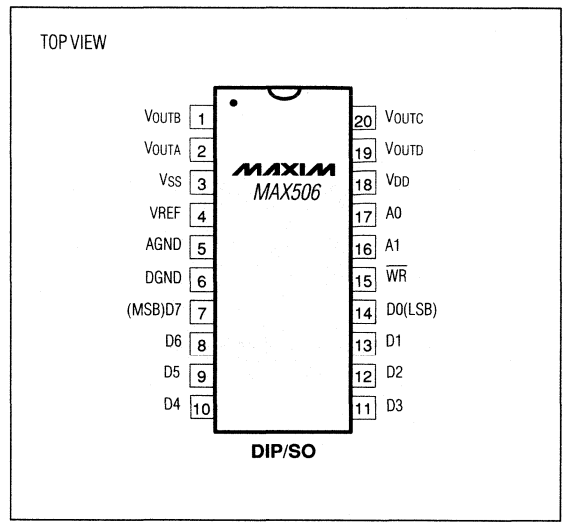
Figure 10b. MAX506 Bipolar Output Circuit

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

Functional Diagrams (continued)



Pin Configurations (continued)



Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	TUE (LSBs)
MAX505AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX505BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1 1/2
MAX505AEWG	-40°C to +85°C	24 Wide SO	±1
MAX505BEWG	-40°C to +85°C	24 Wide SO	±1 1/2
MAX505AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1
MAX505BMRG	-55°C to +125°C	24 Narrow CERDIP**	±1 1/2
MAX506ACPP	0°C to +70°C	20 Plastic DIP	±1
MAX506BCPP	0°C to +70°C	20 Plastic DIP	±1 1/2
MAX506ACWP	0°C to +70°C	20 Wide SO	±1
MAX506BCWP	0°C to +70°C	20 Wide SO	±1 1/2
MAX506BC/D	0°C to +70°C	Dice*	±1 1/2
MAX506AEPP	-40°C to +85°C	20 Plastic DIP	±1
MAX506BEPP	-40°C to +85°C	20 Plastic DIP	±1 1/2
MAX506AEWP	-40°C to +85°C	20 Wide SO	±1
MAX506BEWP	-40°C to +85°C	20 Wide SO	±1 1/2
MAX506AMJP	-55°C to +125°C	20 CERDIP**	±1
MAX506BMJP	-55°C to +125°C	20 CERDIP**	±1 1/2

** Contact factory for dice specifications.*

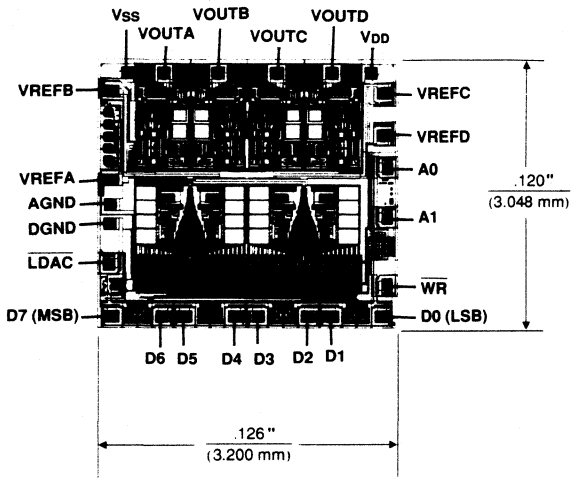
***Contact factory for availability and processing to MIL-STD-883.*

9

Quad 8-Bit DACs with Rail-to-Rail Voltage Outputs

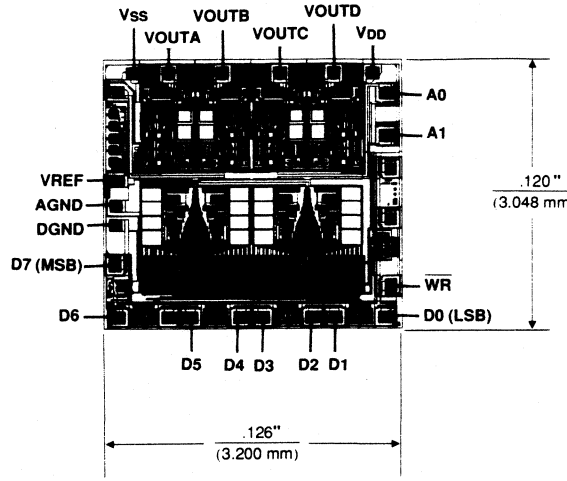
Chip Topographies

MAX505



MAX505 TRANSISTOR COUNT 1717;
SUBSTRATE CONNECTED TO V_{DD}.

MAX506



MAX506 TRANSISTOR COUNT 1717;
SUBSTRATE CONNECTED TO V_{DD}.

19-4338; Rev A; 9/91

MAXIM

Voltage-Output, 12-Bit DACs with Internal Reference

General Description

The MAX507/MAX508 are complete 12-bit, voltage-output digital-to-analog converters (DACs). The DAC output voltage and the reference have the same polarity, allowing single-supply operation. Both DACs include an internal buried-zener reference. Integrating a DAC, voltage-output amplifier, and reference on one monolithic device greatly enhances reliability over multi-chip circuits.

Double-buffered logic inputs interface easily to microprocessors (μPs). Data is transferred into the input register either from a 12-bit-wide data bus (MAX507) for 16-bit μPs, or in a right-justified (8+4)-bit format (MAX508) for 8- or 16-bit μPs. All logic signals are level triggered and are TTL and CMOS compatible. Interface timing specifications insure compatibility with all common μPs.

The DACs are specified and tested for both dual- and single-supply operation. Usable supplies range from single +12V to dual ±15V.

On-board gain-setting resistors allow three output-voltage ranges: 0V to +5V and 0V to +10V can be generated when using either single or dual supplies. With dual supplies, ±5V is also available. The output amplifier can drive a 2kΩ load to +10V.

Applications

Digital Offset and Gain Adjustment
Industrial Controls
Arbitrary Function Waveform Generators
Automatic Test Equipment
Automated Calibration
Machine and Motion Control

Features

- ♦ 12-Bit Voltage Output
- ♦ Internal Voltage Reference
- ♦ Fast μP Interface
- ♦ 12 (MAX507) and 8+4 (MAX508) Data-Bus Widths
- ♦ Single +12V to Dual ±15V Supply Operation
- ♦ 20- and 24-Pin DIP and Wide SO Packages

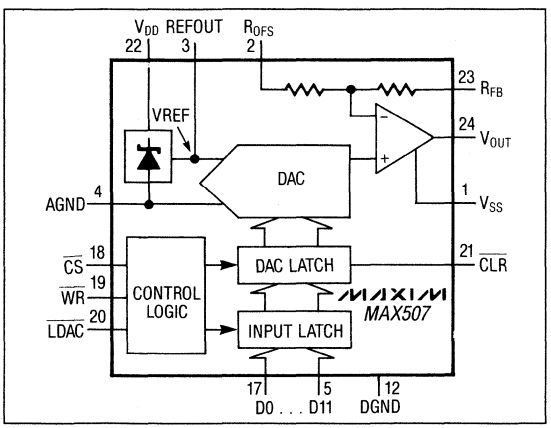
Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX507ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX507BCNG	0°C to +70°C	24 Narrow Plastic DIP	±3/4
MAX507ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX507BCWG	0°C to +70°C	24 Wide SO	±3/4
MAX507BC/D	0°C to +70°C	Dice*	±3/4
MAX507AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX507BENG	-40°C to +85°C	24 Narrow Plastic DIP	±3/4
MAX507AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX507BEWG	-40°C to +85°C	24 Wide SO	±3/4
MAX507AMRG	-55°C to +125°C	24 Narrow CERDIP**	±1/2
MAX507BMRG	-55°C to +125°C	24 Narrow CERDIP**	±3/4

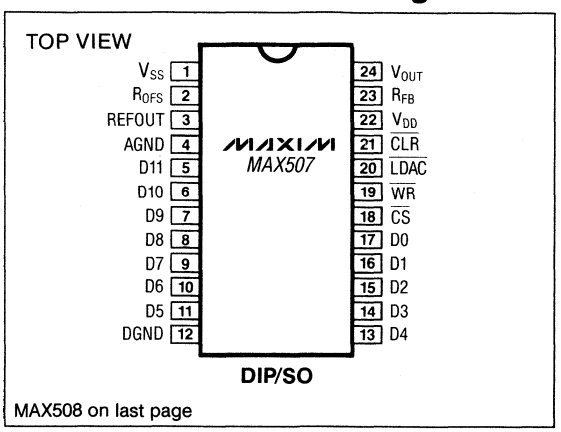
Ordering Information continued on page 12.

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



Pin Configurations



MAX508 on last page

Voltage-Output, 12-Bit DACs with Internal Reference

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
V_{DD} to V_{SS} ..... -0.3V, +34V
AGND to DGND ..... -0.3V, V_{DD}
Digital Input Voltage to GND ..... -0.3V, V_{DD} +0.3V
V_{OUT} to AGND (Note 1) ..... V_{SS}, V_{DD}
V_{OUT} to V_{SS} (Note 1) ..... 0V, +34V
V_{OUT} to V_{DD} (Note 1) ..... -34V, 0V
REFOUT to AGND (Note 1) ..... -0.3V, V_{DD} +0.3V

Continuous Power Dissipation (any package)
to +75°C 450mW
derate above +75°C ..... 6mW/°C
Operating Temperature Ranges:
MAX507_C_, MAX508_C_ ..... 0°C to +70°C
MAX507_E_, MAX508_E_ ..... -40°C to +85°C
MAX507_M_, MAX508_M_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Note 1: The output can be shorted to either supply rail if the package power dissipation is not exceeded. Typical short-circuit current to AGND is 25mA.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Single Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = AGND = DGND = 0V, R_L = 2kΩ, C_L = 100pF, REFOUT unloaded, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	T_A = +25°C	MAX507/508A			±1/2	LSB
			MAX507/508B			±3/4	
		T_A = T_{MIN} to T_{MAX}	MAX507/508A			±3/4	
			MAX507/508B			±1	
Differential Nonlinearity	DNL					±1	LSB
Unipolar Offset Error		T_A = +25°C				±3	LSB
		T_A = T_{MIN} to T_{MAX}				±5	
DAC Gain Error						±2	LSB
Full-Scale Output Voltage Error		V_{DD} = +12V or +15V	T_A = +25°C			±0.2	%FSR
			T_A = T_{MIN} to T_{MAX}			±0.6	
Full-Scale Output Voltage Change		V_{DD} over full range	T_A = +25°C			±0.12	%FSR/V
			T_A = T_{MIN} to T_{MAX}			±0.2	
Full-Scale Tempco		MAX507/508_C/E				±30	ppm FSR/°C
		MAX507/508_M				±40	
Unipolar Offset Error Change		V_{DD} = +12V ± 5% or +15V ± 5%				±1	mV

ELECTRICAL CHARACTERISTICS (continued)

Single Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = AGND = DGND = 0V, R_L = 2kΩ, C_L = 100pF, REFOUT unloaded, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE							
Reference Output		V_{DD} = +12V or +15V	T_A = +25°C	4.99		5.01	V
Reference Voltage Change		V_{DD} = +12V ± 5% or +15V ± 5%	T_A = +25°C			2	mV/V
			T_A = T_{MIN} to T_{MAX}			6	
Reference Temperature Coefficient		MAX507/508_C/E			±30		ppm/°C
		MAX507/508_M			±40		
Reference Load Sensitivity		I_{LOAD} = 0μA to 100μA				±1	mV
ANALOG OUTPUT							
Ranges (Note 2)						0 to 5	V
						0 to 10	
Output Range Resistors				15		30	kΩ
DC Output Impedance					0.5		Ω
Short-Circuit Current					40		mA
DYNAMIC PERFORMANCE (Note 3)							
Voltage-Output Slew Rate				2			V/μs
V_{OUT} Settling Time		To ±1/2 LSB for full-scale change				5	μs
Digital Feedthrough					10		nV-s
Digtal-to-Analog Glitch Impulse		Major carry transition			30		nV-s
Output Load Resistance (Note 2)		V_{OUT} = 0V to +10V		2			kΩ
POWER SUPPLIES							
V_{DD} Range		For specified performance		11.4		15.75	V
I_{DD}		Outputs unloaded	T_A = +25°C			9	mA
			T_A = T_{MIN} to T_{MAX}			12	

9

Voltage-Output, 12-Bit DACs with Internal Reference

ELECTRICAL CHARACTERISTICS

Dual Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = -11.4V to -15.75V, DGND = AGND = 0V, R_L = 2kΩ, C_L = 100pF, REFOUT unloaded, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE							
Resolution	N			12			Bits
Relative Accuracy	INL	T_A = +25°C	MAX507/508A			±1/2	LSB
			MAX507/508B			±3/4	
		T_A = T_{MIN} to T_{MAX}	MAX507/508A			±3/4	
			MAX507/508B			±1	
Differential Nonlinearity	DNL					±1	LSB
Bipolar Zero Offset Error	BZOE	MAX507/508A	T_A = +25°C			±2	LSB
			T_A = T_{MIN} to T_{MAX}			±4	
		MAX507/508B	T_A = +25°C			±3	
			T_A = T_{MIN} to T_{MAX}			±5	
DAC Gain Error						±2	LSB
Full-Scale Output Voltage Error		V_{DD} = +15V, V_{SS} = -15V	T_A = +25°C			±0.2	%FSR
			T_A = T_{MIN} to T_{MAX}			±0.6	
		V_{DD} = +12V, V_{SS} = -12V	T_A = +25°C			±0.2	
			T_A = T_{MIN} to T_{MAX}			±0.6	
Full-Scale Output Change with V_{DD}		V_{DD} = +12V ± 5% or +15V ± 5%, V_{SS} = -12V or -15V	T_A = +25°C			±0.12	%FSR/V
			T_A = T_{MIN} to T_{MAX}			±0.2	
Full-Scale Output Change with V_{SS}	V_{SS}	V_{SS} = -12V ± 5% or -15V ± 5%, V_{DD} = +12V or +5V				0.01	%FSR/V
Full-Scale Tempco		MAX507/508_C/E				±30	ppm FSR/°C
		MAX507/508_M				±40	
Bipolar Zero Offset Change		V_{DD} = +12V ± 5% or +15V ± 5%, V_{SS} = -12V or -15V				±1	mV
		V_{SS} = -12V ± 5% or -15V ± 5%, V_{DD} = +12V or +15V				±1	
REFERENCE							
Reference Output		V_{DD} = +12V or +15V	T_A = +25°C	4.99		5.01	V
Reference Output Change		V_{DD} over full range	T_A = +25°C			2	mV/V
			T_A = T_{MIN} to T_{MAX}			6	
Reference Temperature Coefficient		MAX507/508_C/E			±30		ppm/°C
		MAX507/508_M			±40		
Reference Load Sensitivity		I_{LOAD} = 0μA to 100μA				±1	mV

ELECTRICAL CHARACTERISTICS (continued)

Dual Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = -11.4V to -15.75V, DGND = AGND = 0V, R_L = 2kΩ, C_L = 100pF, REFOUT unloaded, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG OUTPUT							
Ranges (Notes 2, 4)					0 to +5 or +10, -5 to +5		V
Output Range Resistors				15		30	kΩ
DC Output Impedance					0.5		Ω
Short-Circuit Current					40		mA
DYNAMIC PERFORMANCE (Note 3)							
Voltage-Output Slew Rate				2			V/μs
V_{OUT} Settling Time		to ±1/2 LSB				5	μs
Digital Feedthrough					10		nV-s
Digtal-to-Analog Glitch Impulse		Major carry transition			30		nV-s
Output Load Resistance		V_{OUT} = -5V to +10V		2			kΩ
POWER SUPPLIES							
V_{DD} Range		For specified performance		11.4		15.75	V
V_{SS} Range		For specified performance		-11.4		-15.75	V
I_{DD}		Outputs unloaded	T_A = +25°C			9	mA
			T_A = T_{MIN} to T_{MAX}			12	
I_{SS}		Outputs unloaded	T_A = +25°C			3	mA
			T_A = T_{MIN} to T_{MAX}			5	

Voltage-Output, 12-Bit DACs with Internal Reference

ELECTRICAL CHARACTERISTICS

Single or Dual Supply (V_{DD} = +11.4V to +15.75V, V_{SS} = 0V to -15.75V, DGND = AGND = 0V, REFOUT unloaded, R_L = 2kΩ, C_L = 100pF, all grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS							
V_{INH}				2.4			V
V_{INL}						0.8	V
Input Current	I_{IN}	D0–D11	T_A = +25°C			±1	µA
			T_A = T_{MIN} to T_{MAX}			±10	
I_{INH}		$\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$, $\overline{CLR}$	T_A = +25°C			±1	µA
			T_A = T_{MIN} to T_{MAX}			±10	
I_{INL}		$\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$, $\overline{CLR}$	T_A = +25°C			±150	µA
			T_A = T_{MIN} to T_{MAX}			±200	
Digital Input Capacitance					8		pF

TIMING CHARACTERISTICS

(All grades, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width (Note 5)	t_1	T_A = +25°C	80			ns
		T_A = T_{MIN} to T_{MAX}	100			
$\overline{WR}$ Pulse Width	t_2	T_A = +25°C	80			ns
		T_A = T_{MIN} to T_{MAX}	100			
$\overline{CS}$ to $\overline{WR}$ Setup Time (Note 5)	t_3		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time (Note 5)	t_4		0			ns
Data to $\overline{WR}$ Setup Time	t_5	T_A = +25°C	100			ns
		T_A = T_{MIN} to T_{MAX}	110			
Data to $\overline{WR}$ Hold Time	t_6		10			ns
$\overline{LDAC}$ Pulse Width	t_7	T_A = +25°C	80			ns
		T_A = T_{MIN} to T_{MAX}	100			
$\overline{CLR}$ Pulse Width (MAX507)	t_8	T_A = +25°C	80			ns
		T_A = T_{MIN} to T_{MAX}	100			

Note 2: V_{OUT} must be less than (V_{DD} - 2.5V).
Note 3: Dynamic performance is included for design guidance, not subject to test.
Note 4: The 0V to +5V or +10V ranges can be used with V_{SS} = -5V with no degradation.
Note 5: CS = CSLSB and $\overline{CS}$MSB for MAX508.

Voltage-Output, 12-Bit DACs with Internal Reference

Detailed Description

Digital-to-Analog Converters

The MAX507/MAX508 are 12-bit, voltage-output DACs. The DAC output voltage has the same polarity as the reference, allowing single-supply operation.

The basic DAC circuit consists of a laser-trimmed, thin-film, R-2R resistor array with NMOS voltage switches (Figure 1).

Output-Buffer Amplifier

The output amplifier is noninverting and configurable for a gain of 1 or 2. Three output voltage ranges can be configured for: 0V to +5V, 0V to +10V, and -5V to +5V. The output amplifier can drive 2kΩ in parallel with 100pF connected to GND.

The MAX507/MAX508 can operate from a single supply with a 0V to +5V or a 0V to +10V output range by tying V_{SS} to 0V. However, the speed and current-sinking capability of the amplifier decreases as the output falls within 0.5V of V_{SS}. Speed and current-sinking capability can be maintained by including a negative supply. Table 1 lists the allowable single and dual supplies for each range.

The output amplifier's small-signal bandwidth is typically 2MHz. Output noise is approximately $25nV/\sqrt{Hz}$ at 1kHz, and output broadband noise is approximately $25\mu V_{RMS}$.

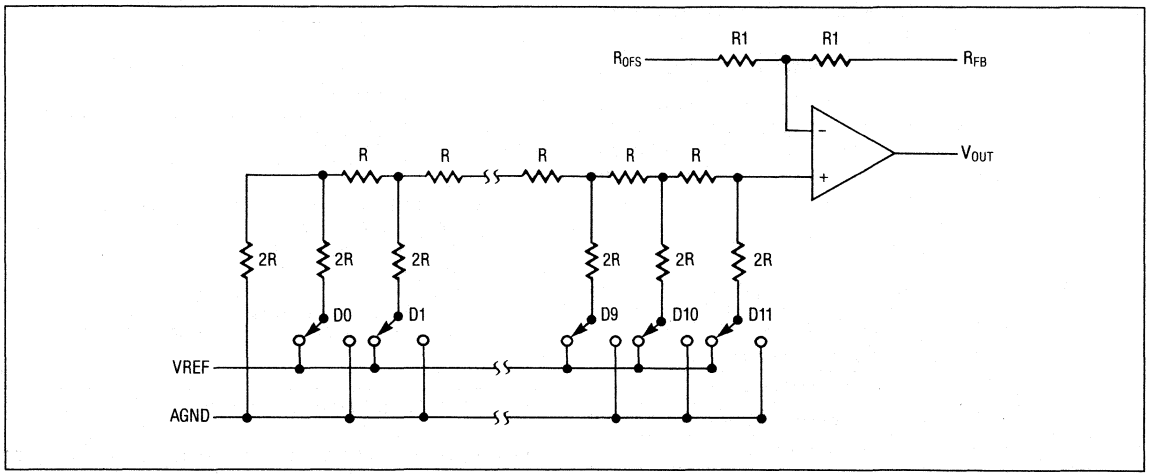


Figure 1. Simplified MAX507 DAC Circuit

Table 1. Output Voltage Range vs. Supply Voltage

Range	Single Supply V_{DD}	Dual Supply V_{DD}	Dual Supply V_{SS}
0V to +5V	+11.4V to +15.75V	+11.4V to +15.75V	-4.5V to -15.75V
0V to +10V	+14.25V to +15.75V	+14.25V to +15.75V	-4.5V to -15.75V
-5V to +5V		+11.4V to +15.75V	-11.4V to -15.75V

Voltage-Output, 12-Bit DACs with Internal Reference

Voltage Reference

The voltage at REFOUT is 5V ± 10mV at +25°C. The reference is internally connected to the DAC and is buffered to accommodate the DAC's variable impedance. This buffer is capable of driving the DAC, the R_{OFS} resistor, and up to 500μA of external current. MAX507/MAX508 specifications are determined with the internal reference. The reference should be decoupled at REFOUT with 10Ω in series with the recommended decoupling capacitors, 10μF in parallel with 0.1μF.

Digital Inputs and Interface Logic

All logic inputs are compatible with both TTL and 5V CMOS logic. Supply current is specified for TTL input levels, but is reduced by about 450μA when the data inputs are driven near DGND or V_{DD}. The control inputs (CLR, LDAC, WR, CS, CSMSB, and CSLSB) each draw 100μA from I_{DD} when low.

MAX507 Interface

Table 2 is the MAX507 truth table. The MAX507 accepts a 12-bit input word that can be latched or transferred directly to the DAC. CS and WR control the input latch, and LDAC transfers information from the input latch to the DAC latch.

Table 2. MAX507 Truth Table

CLR	LDAC	WR	CS	Function
1	0	0	0	Both latches transparent
1	1	1	X	Both latches latched
1	1	X	1	Both latches latched
1	1	0	0	Input latch transparent
1	1	↑	0	Input latch latched
1	0	1	1	DAC latch transparent
1	↑	1	1	DAC latch latched
0	X	X	X	DAC latch all 0s
↑	1	1	1	DAC latch latched with 0s; output at 0V or -5V
↑	0	0	0	Both latches transparent; output follows input data

1 = High State
0 = Low State
X = Don't Care
↑ = Rising Edge

The input latch is transparent when CS and WR are low; the DAC latch is transparent when LDAC is low. Data is latched within the input latch on the rising edge of WR when CS is low. The rising edge of LDAC latches data into the DAC when CS and WR are low. After CS and WR are high, LDAC must be held low for t_7 or longer (Figure 2).

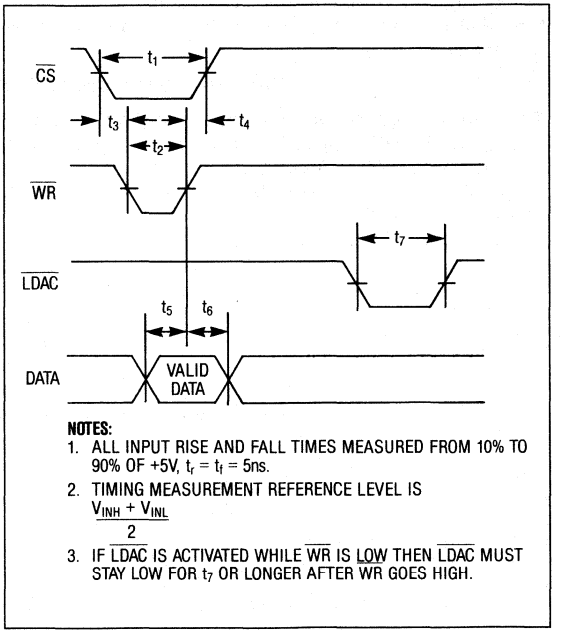


Figure 2. MAX507 Timing Diagram

The DAC latch is reset to zeros with CLR low. CLR acts as a zero override when the input latch and DAC latch are transparent. Then, a low-to-high CLR transition loads all zeros into the DAC latch, and the output remains low (0V to -5V).

MAX508 Interface

The MAX508's 8-bit-wide data bus interfaces with 8-bit μPs. The MAX508 contains an input latch and a DAC latch. The data held in the DAC latch determines the output of the DAC. Table 3 is the MAX508 truth table, Figure 3 shows the input control logic, and Figure 4 shows the write-cycle timing.

Table 3. MAX508 Truth Table

$\overline{CSLSB}$	$\overline{CSMSB}$	$\overline{WR}$	$\overline{LDAC}$	Function
0	1	0	1	Loads LSBs to input latches
0	1	↑	1	Locks LSBs in input latches
↑	1	0	1	Locks LSBs in input latches
1	0	0	1	Loads MSBs to input latches
1	0	↑	1	Locks MSBs in input latches
1	↑	0	1	Locks MSBs in input latches
1	1	1	0	Loads input into DAC latch
1	1	1	↑	Locks input into DAC latch
1	0	0	0	Loads MSBs to input latches and loads input into DAC latch
1	1	1	1	No data transfer

1 = High State 0 = Low State ↑ = Rising Edge

Right-justified data is loaded into the MAX508 using $\overline{CSMSB}$, $\overline{CSLSB}$, and $\overline{WR}$. Data can be latched into the input latch on the rising edge of $\overline{WR}$ for the most significant bit (MSB) and least significant bit (LSB), or on the rising edge of $\overline{CSMSB}$ for the MSB and $\overline{CSLSB}$ for the LSB. Either the MSB or the LSB can be loaded first.

The complete, 12-bit word loads into the DAC register when $\overline{LDAC}$ is low, and latches on $\overline{LDAC}$'s rising edge. $\overline{LDAC}$ is asynchronous and independent of $\overline{WR}$, so it is ideal for simultaneously updating multiple MAX508 outputs. Because $\overline{LDAC}$ can occur during a write cycle, it must stay low for t_7 (or longer) after $\overline{WR}$ goes high to ensure correct data is latched to the output.

The MAX508 output can be updated in two write cycles by tying $\overline{CSMSB}$ and $\overline{LDAC}$. In this automatic transfer mode, $\overline{CSLSB}$ and $\overline{WR}$ latch the lower 8 bits into the input latch; then $\overline{CSMSB}$, $\overline{WR}$, and $\overline{LDAC}$ load the upper 4 bits into the input latch and transfer the 12-bit word into the DAC latch. Alternatively, the MAX507 can be updated in two writes by tying $\overline{CSLSB}$ to $\overline{LDAC}$ if the upper 4 bits are input first, followed by the lower 8 bits.

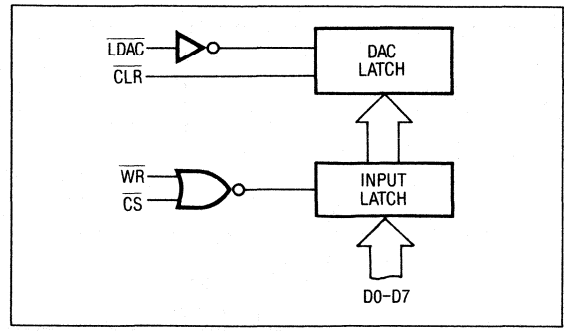


Figure 3a. MAX507 Input Control Logic

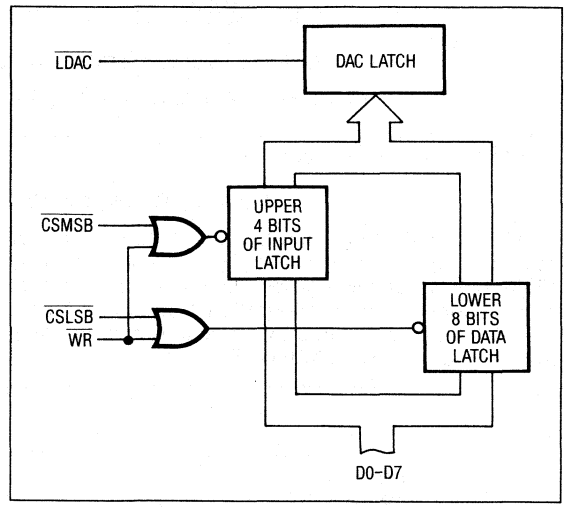


Figure 3b. MAX508 Input Control Logic

9

Voltage-Output, 12-Bit DACs with Internal Reference

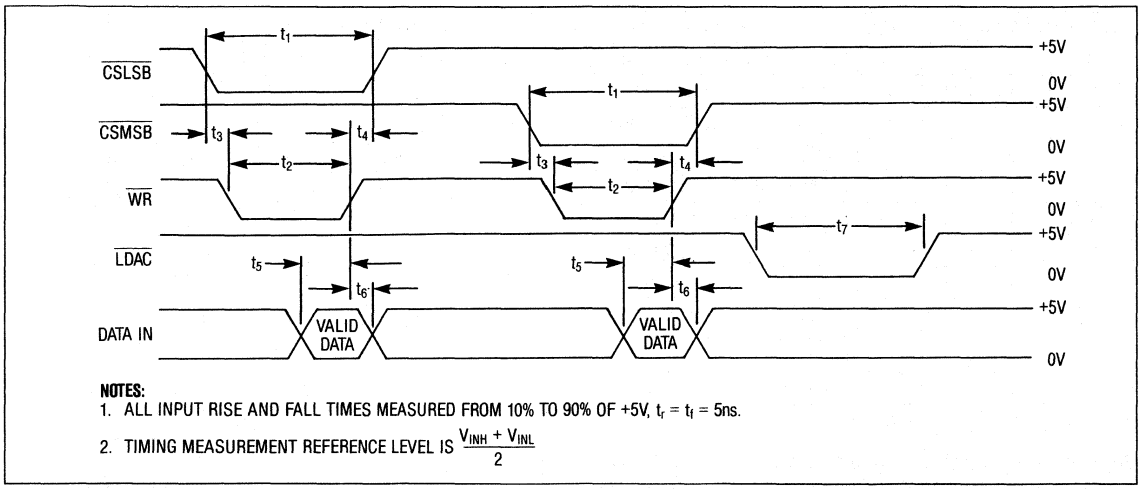


Figure 4. MAX508 Timing Diagram

Unipolar Configuration

The MAX507/MAX508 are set up for a 0V to +5V unipolar output range by connecting ROFS, RFB, and VOUT (Figure 5). The converters operate from either a single or a dual supply in this configuration. See Table 4 for the DAC-latch contents (input) vs. analog output (output). In this range, 1LSB = VREF (2^{-12}).

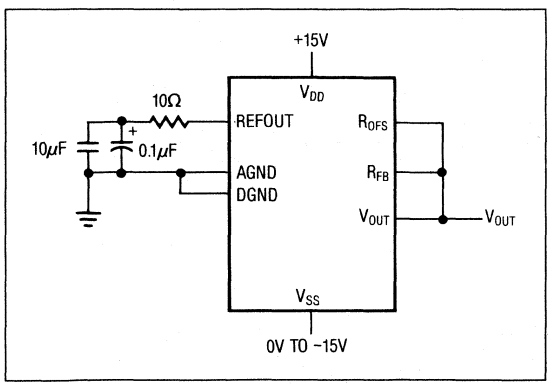


Figure 5. Unipolar Configuration (0V to +5V Output)

Table 4. Unipolar-Code Table (0V to +5V Output)

INPUT			OUTPUT
1111	1111	1111	(VREF) 4095/4096
1000	0000	0001	(VREF) 2049/4096
1000	0000	0000	(VREF) 2048/4096 =+VREF/2
0111	1111	1111	(VREF) 2047/4096
0000	0000	0001	(VREF) 1/4096
0000	0000	0000	0V

A 0V to +10V unipolar output range is set up by connecting ROFS to AGND and RFB to VOUT (Figure 6). See Table 5 for the DAC-latch contents (input) vs. analog output (output). The MAX507/MAX508 operate from either a single or a dual supply in this configuration. In this range, 1LSB = VREF (2^{-11}).

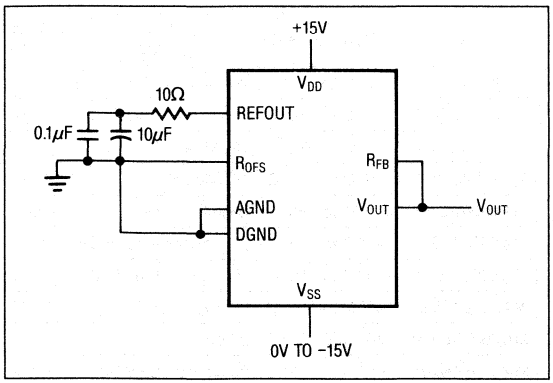


Figure 6. Unipolar Configuration (0V to +10V Output)

Table 5. Unipolar-Code Table (0V to +10V Output)

INPUT			OUTPUT
1111	1111	1111	$+2\ (VREF)\frac{4095}{4096}$
1000	0000	0001	$+2\ (VREF)\frac{2049}{4096}$
1000	0000	0000	$+2\ (VREF)\frac{2048}{4096}=+VREF$
0111	1111	1111	$+2\ (VREF)\frac{2047}{4096}$
0000	0000	0001	$+2\ (VREF)\frac{1}{4096}$
0000	0000	0000	0V

Bipolar Configuration

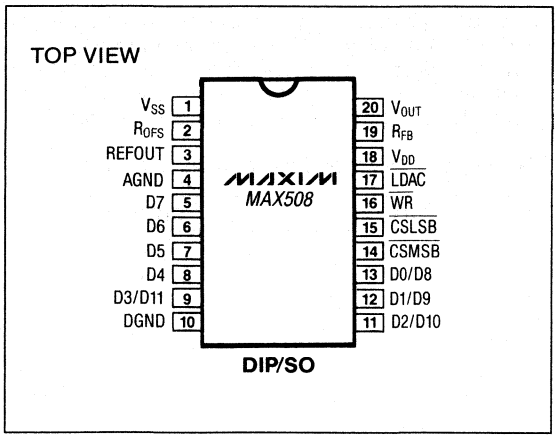
A -5V to +5V bipolar range is set up by connecting R_{OFS} to REFOUT and R_{FB} to V_{OUT}, and operating from dual power supplies (Table 1). See Table 6 for the DAC-latch contents (input) vs. analog output (output). In this range, 1LSB = (2) VREF (2^{-11}) = (VREF) 1/2048.

Table 6. Bipolar-Code Table (-5V to +5V Output)

INPUT			OUTPUT
1111	1111	1111	$(+VREF)\frac{2047}{2048}$
1000	0000	0001	$(+VREF)\frac{1}{2048}$
1000	0000	0000	0V
0111	1111	1111	$(-VREF)\frac{1}{2048}$
0000	0000	0001	$(-VREF)\frac{2047}{2048}$
0000	0000	0000	$(-VREF)\frac{2048}{2048}=-VREF$

Voltage-Output, 12-Bit DACs with Internal Reference

Pin Configurations (continued)



Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	ERROR (LSBs)
MAX508ACPP	0°C to +70°C	20 Narrow Plastic DIP	±1/2
MAX508BCPP	0°C to +70°C	20 Narrow Plastic DIP	±3/4
MAX508ACWP	0°C to +70°C	20 Wide SO	±1/2
MAX508BCWP	0°C to +70°C	20 Wide SO	±3/4
MAX508BC/D	0°C to +70°C	Dice*	±3/4
MAX508AEPP	-40°C to +85°C	20 Narrow Plastic DIP	±1/2
MAX508BEPP	-40°C to +85°C	20 Narrow Plastic DIP	±3/4
MAX508AEWP	-40°C to +85°C	20 Wide SO	±1/2
MAX508BEWP	-40°C to +85°C	20 Wide SO	±3/4
MAX508AMJP	-55°C to +125°C	20 Narrow CERDIP**	±1/2
MAX508BMJP	-55°C to +125°C	20 Narrow CERDIP**	±3/4

* *Contact factory for dice specifications.*
** *Contact factory for availability and processing to MIL-STD-883.*

19-4516; Rev. 0; 12/91

MAXIM

CMOS Quad, 12-Bit, Serial-Input Multiplying DAC

General Description

The MAX514 contains four 12-bit R-2R multiplying digital-to-analog converters (DACs), each with a serial-in parallel-out shift register, a DAC register, and control logic. The MAX514's 3-wire serial interface design minimizes the number of package pins and internal level translators, so it uses less board space and dissipates less power (10mW max) than parallel-interface devices.

When used with microprocessors (µPs) with a serial port, the MAX514 minimizes digital-noise feedthrough from its logic input pins to its analog output. To further reduce noise, the µP serial port can be used as a dedicated analog bus and kept inactive while the MAX514 is in use. Serial interfacing also simplifies opto-coupler or transformer-isolated applications.

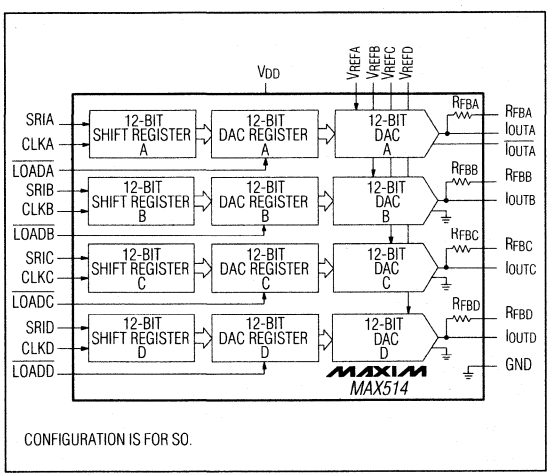
This device uses low-tempco thin-film resistors, laser trimmed to ±1LSB linearity, with gain accuracy better than ±1½LSB.

The MAX514 is specified with a +5V power supply. All logic inputs are TTL and CMOS compatible. It comes in space-saving 24-pin DIP and 28-pin SO packages.

Applications

Digital Offset/Gain Adjustment
Arbitrary Waveform Generators
Industrial Process Controls
Automatic Test Equipment
Motion Control Systems
Programmable Amplifiers/Attenuators
µP-Controlled Systems

Functional Diagram



CONFIGURATION IS FOR SO.

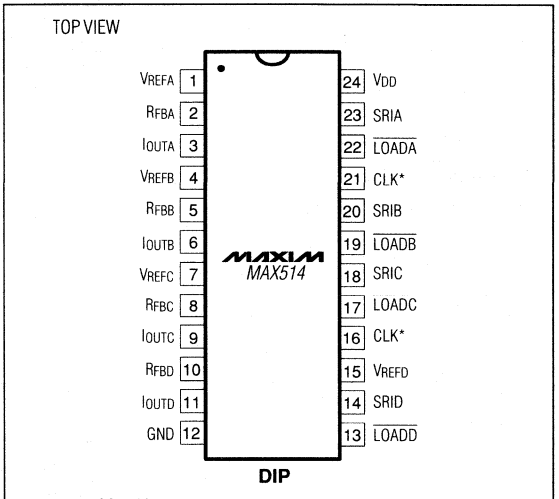
Features

- ♦ **Four 12-Bit Accurate DACs**
- ♦ **Fast 3-Wire Serial Interface**
- ♦ **Low Differential Nonlinearity: ±½LSB Max**
- ♦ **Low Integral Nonlinearity: ±1LSB Max**
- ♦ **Gain Accuracy to ±1½LSB Max**
- ♦ **Low Gain Tempco: 5ppm/°C Max**
- ♦ **Operates from a Single +5V Power Supply**
- ♦ **TTL/CMOS Compatible**
- ♦ **Available in 24-Pin DIP and 28-Pin SO Packages**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	DNL (LSBs)
MAX514ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX514BCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX514ACWI	0°C to +70°C	28 Wide SO	±1/2
MAX514BCWI	0°C to +70°C	28 Wide SO	±1
MAX514AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX514BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX514AEWI	-40°C to +85°C	28 Wide SO	±1/2
MAX514BEWI	-40°C to +85°C	28 Wide SO	±1

Pin Configurations



*INTERNALLY CONNECTED

Pin Configurations continued on last page

CMOS Quad, 12-Bit, Serial-Input Multiplying DAC

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
V_{RFB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD} + 0.3V
I_{OUTA} to GND ..... -0.3V, V_{DD} + 0.3V
Continuous Power Dissipation (T_A = +70°C)
24-Pin Narrow Plastic DIP
(derate 8.7mW/°C above +70°C) 696mW
28-Pin Wide SO
(derate 12.5mW/°C above +70°C) ..... 1000mW/°C
Maximum Current into Any Pin 50mA
Operating Temperature Ranges:
MAX514_C__ ..... 0°C to +70°C
MAX514_E__ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering , 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V, V_{REF} = +10V, I_{OUT} = $I_{\overline{OUTA}}$ = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
STATIC PERFORMANCE								
Resolution	N				12			Bits
Integral Nonlinearity	INL						±1	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic		MAX514A			±1/2	LSB
				MAX514B			±1	
Full-Scale Error (Gain Error)	FSE	Using internal R_{FB}	T_A = +25°C	MAX514A			±1.5	LSB
				MAX514B			±2.5	
			T_A = T_{MIN} to T_{MAX}	ALL			±2.5	
Full-Scale Temperature Coefficient (Note 1)	TCFS	Using internal R_{FB}				±1	±5	ppm/°C
DC Power-Supply Rejection	PSR	V_{DD} = 4.75V to 5.25V					±0.001	%/%
DYNAMIC PERFORMANCE (Note 1)								
Current Settling Time	t_s	T_A = +25°C, to 1/2LSB, I_{OUT} load is 100Ω | 113pF, DAC register alternately loaded with all 1s and all 0s				0.25	1	µs
Digital Feedthrough	Q	V_{REF} = 0V, I_{OUT} load is 100Ω | 113pF, DAC register alternately loaded with all 1s and all 0s				2	20	nV-s
AC Feedthrough at I_{OUT}	FTE	V_{REF} = ±10V_{p-p} at 10kHz, DAC register loaded with all 0s				0.4	1	mV_{p-p}
Total Harmonic Distortion	THD	V_{REF} = 6V_{RMS} at 1kHz, DAC register loaded with all 1s				-85		dB
Output Noise Voltage Density	e_n	T_A = +25°C, 10Hz to 100kHz, measured between R_{FB} and I_{OUT}				13	15	nV/√Hz
REFERENCE INPUT								
Reference Input Resistance	R_{REF}	V_{REF} pin to I_{OUT}			7	11	25	kΩ
Input Resistance Tempco	TCR					-200		ppm/°C
ANALOG OUTPUTS								
I_{OUT} Leakage Current	I_{LKG}	DAC register loaded with all 0s		T_A = +25°C		±0.5	±5	nA
				T_A = T_{MIN} to T_{MAX}			±25	
$I_{\overline{OUTA}}$ Leakage Current (DAC A, SO package only)	I_{LKG}	DAC register loaded with all 1s		T_A = +25°C		±0.5	±5	nA
				T_A = T_{MIN} to T_{MAX}			±25	
I_{OUT} Capacitance (Note 1)	C_{OUT1}	DAC register loaded with all 0s				55	80	pF
		DAC register loaded with all 1s				85	110	
$I_{\overline{OUTA}}$ Capacitance (DAC A, SO package only) (Note 1)	C_{OUT2}	DAC register loaded with all 0s				85	110	pF
		DAC register loaded with all 1s				55	80	

ELECTRICAL CHARACTERISTICS (continued)

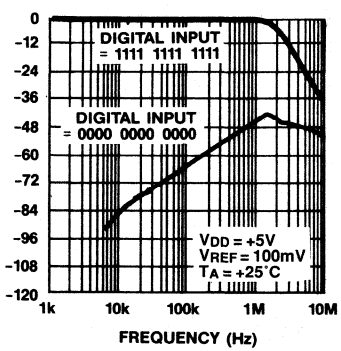
(V_{DD} = +5V, V_{REF} = +10V, I_{OUT} = $\overline{I_{OUTA}}$ = GND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS						
Digital Input High Voltage	V_{IH}		2.4			V
Digital Input Low Voltage	V_{IL}				0.8	V
Digital Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}			±1	µA
CLK Input Leakage Current (DIP only, pins 16, 21)	I_{IN}	V_{IN} = 0V or V_{DD}			±4	µA
Digital Input Capacitance (Note 1)	C_{IN}	V_{IN} = 0V or V_{DD}			8	pF
CLK Input Capacitance (DIP only, pins 16, 21) (Note 1)	C_{IN}	V_{IN} = 0V or V_{DD}			32	pF
SWITCHING CHARACTERISTICS						
CLK Pulse Width High	t_{CH}		90			ns
CLK Pulse Width Low	t_{CL}		120			ns
SRI Data to CLK Setup	t_{DS}		40			ns
SRI Data to CLK Hold	t_{DH}		80			ns
$\overline{LOAD}$ Pulse Width	t_{LD}		120			ns
LSB CLK to $\overline{LOAD}$	t_{SL}		0			ns
$\overline{LOAD}$ High to CLK	t_{LC}		0			ns
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	For specified performance	4.75		5.25	V
Positive Supply Current	I_{DD}	All digital inputs at V_{IL} or V_{IH}			2000	µA
		All digital inputs at 0V or V_{DD}		20	400	

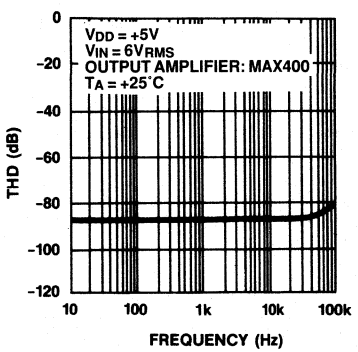
Note 1: Guaranteed by design, not subject to test.

Typical Operating Characteristics

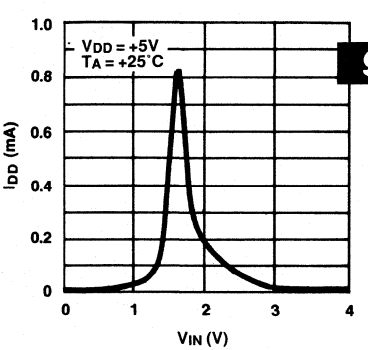
GAIN vs. FREQUENCY (OUTPUT AMPLIFIER: MAX400)



TOTAL HARMONIC DISTORTION vs. FREQUENCY (MULTIPLYING MODE)



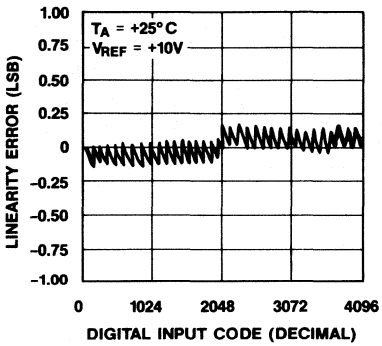
SUPPLY CURRENT vs. LOGIC INPUT VOLTAGE



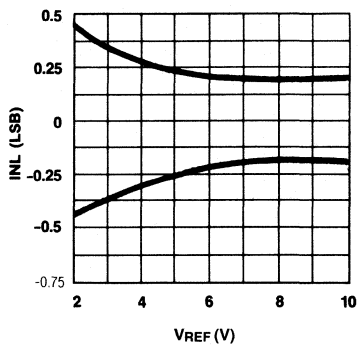
CMOS Quad, 12-Bit, Serial-Input Multiplying DAC

Typical Operating Characteristics (continued)

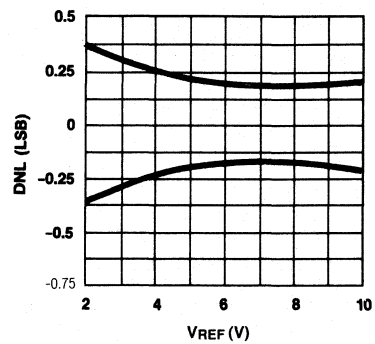
LINEARITY ERROR vs. DIGITAL CODE



INL ERROR vs. REFERENCE VOLTAGE



DNL ERROR vs. REFERENCE VOLTAGE



Pin Description

24-PIN DIP	28-PIN SO	NAME	FUNCTION
1	1	V_{REFA}	Reference Voltage Input for DACA
2	2	R_{FBA}	Internal Feedback Resistor for DACA
3	3	I_{OUTA}	DACA Output Current
–	4	$\overline{I_{OUTA}}$	DACA Inverted Current Output
4	5	V_{REFB}	Reference Voltage Input for DACB
5	6	R_{FBB}	Internal Feedback Resistor for DACB
6	7	I_{OUTB}	DACB Output Current
7	8	V_{REFC}	Reference Voltage Input for DACC
8	9	R_{FBC}	Internal Feedback Resistor for DACC
9	10	I_{OUTC}	DACC Output Current
15	11	V_{REFD}	Reference Voltage Input for DACD
10	12	R_{FBD}	Internal Feedback Resistor for DACD
11	13	I_{OUTD}	DACD Output Current
12	14	GND	Power-Supply Ground
13	15	$\overline{LOADD}$	Load DACD Input (active low). Driving this input low transfers the contents of shift register D to DAC register D and updates analog output D.
14	16	SRID	Serial Data Input for DACD
–	17	CLKD	Serial Clock Input for DACD
16, 21	–	CLK	Serial Clock Input for all four DACs. CLK pins are internally connected on DIP packaged parts.
17	18	$\overline{LOADC}$	Load DACC Input (active low). Driving this input low transfers the contents of shift register C to DAC register C and updates analog output C.
18	19	SRIC	Serial Data Input for DACC
–	20	CLKC	Serial Clock Input for DACC
19	21	$\overline{LOADB}$	Load DACB Input (active low). Driving this input low transfers the contents of shift register B to DAC register B and updates analog output B.
20	22	SRIB	Serial Data Input for DACB
–	23	CLKB	Serial Clock Input for DACB
–	24	N.C.	No Connect
22	25	$\overline{LOADA}$	Load DACA Input (active low). Driving this input low transfers the contents of shift register A to DAC register A and updates analog output A.
23	26	SRIA	Serial Data Input for DACA
–	27	CLKA	Serial Clock Input for DACA
24	28	V_{DD}	Positive Supply Voltage

Detailed Description

DAC Section

The MAX514 contains four current-output digital-to-analog converters (DACs). Each DAC consists of a laser-trimmed R-2R resistor array with NMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either I_{OUT} or GND (I_{OUTA} for DAC A), depending upon the status of each input data bit.

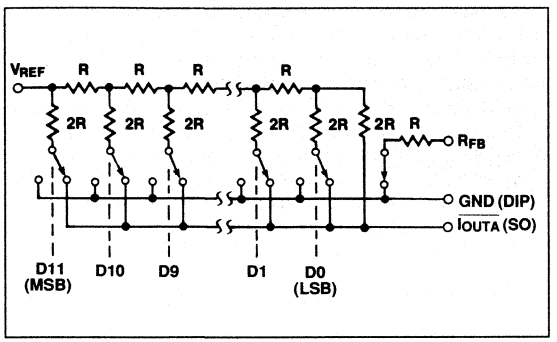


Figure 1. Simplified D/A Circuit for 1/4 of MAX514

Each of the current outputs (I_{OUT}) can be converted to a voltage by adding an external output amplifier as shown in Figure 3. V_{REF} inputs accept a wide range of signals, including fixed and time-varying voltage or current inputs. If a current source is used for the reference input, a low tempco external resistor should be used for R_{FB} to minimize gain variation with temperature.

Each internal feedback resistor (R_{FB}) is compensated with an NMOS switch that matches the NMOS switches used in the R-2R array. This results in excellent power-supply rejection and gain-temperature coefficient.

Digital Inputs and Interface Logic

Figure 2 shows the write-cycle timing diagram for the MAX514. The most significant bit (MSB) is always loaded first on the rising edge of the clock (CLK). Once all data is shifted into the MAX514, each DAC register is loaded by taking the corresponding $\overline{LOAD}$ signal low. The DAC registers are transparent when their $\overline{LOAD}$ input is low, and latched when their $\overline{LOAD}$ input is high. If $\overline{LOAD}$ is taken low before the least significant bit (LSB) is shifted into the shift register, the DAC output can produce a "glitch." If this is undesirable, avoid it by delaying the $\overline{LOAD}$ signal 30ns after the rising edge of the LSB CLK edge.

The digital interface of the dual-in-line package (DIP) and small outline (SO) devices differs slightly. Each DAC in the SO has its own CLK input, while DACs in the DIP share a common CLK input. The common CLK input of the DIPs is located on pins 16 and 21, which are internally connected. DACs can be individually loaded by separately controlling the four $\overline{LOAD}$ inputs. Data is shifted into each DAC through its SRI pin using the common CLK input. The output voltage of each DAC is updated after its $\overline{LOAD}$ input has been exercised, while the remaining DAC outputs are unchanged.

If simultaneous updating of all four DAC outputs is desired, the $\overline{LOAD}$ inputs on DIP devices should be bussed together and driven from a common source. Simultaneous updating of the four DAC outputs on SO devices can be accomplished by bussing the four CLK inputs together and the four $\overline{LOAD}$ inputs together.

The MAX514's input buffers act as level shifters, converting TTL levels into DAC switch-drive levels. Input buffers are compatible with both TTL and 5V CMOS logic, however the power supply current (I_{DD}) is dependent upon the input logic levels. Supply current is significantly

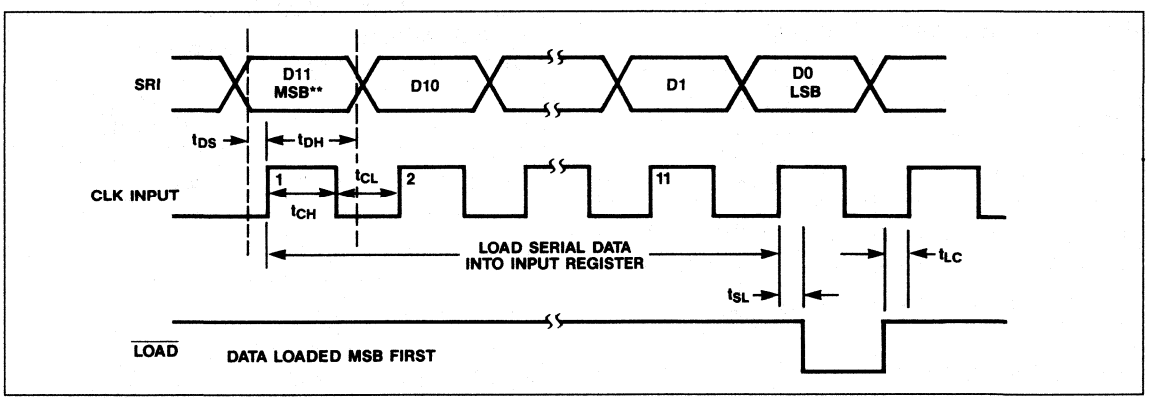


Figure 2. Write-Cycle Timing Diagram

CMOS Quad, 12-Bit, Serial-Input Multiplying DAC

reduced when logic inputs are driven as close to DGND as possible, and above 4V. This phenomenon is shown in the *Supply Current vs. Logic Input Voltage* graph in the *Typical Operating Characteristics*.

Circuit Configurations

Unipolar Operation

Figure 3 shows the basic application circuit for one-fourth of the MAX514. This circuit is used for unipolar operation or 2-quadrant multiplication. The unipolar output-code table is given in Table 1. Note that the polarity of the output voltage is the inverse of the reference voltage input (V_{REF}).

In many applications, gain adjustment will not be necessary: The gain accuracy of the part may be sufficient, or gain may be trimmed at the reference source. In these cases, resistors R1 and R2 in Figure 3 can be omitted. When the DAC is trimmed and operated over a wide temperature range, use low tempco (<300ppm/°C) resistors for R1 and R2.

The capacitor, C1, provides phase compensation and reduces overshoot and ringing when fast amplifiers are used at the DAC outputs.

Bipolar Operation

Figure 4 shows the MAX514 operating in the bipolar, or 4-quadrant multiplying mode. A second amplifier and three matched resistors (R3, R4, and R5) are required for each DAC output. These resistors must be of the same material (preferably metal film or wire-wound) for good temperature tracking characteristics (<15ppm/°C), and should match to 0.01% for 12-bit performance. The output code is offset binary and is listed in Table 2. In multiplying applications, the MSB determines output polarity while the other 11 bits control the amplitude. The MSB can be inverted in software using an exclusive-OR

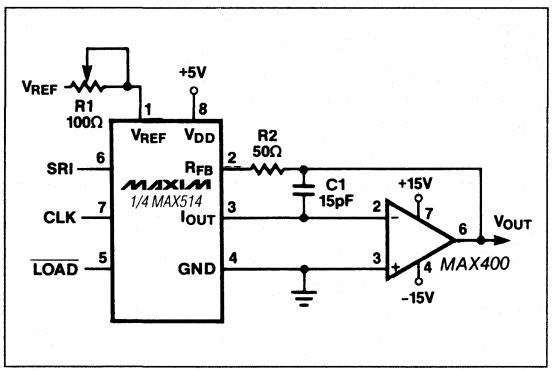


Figure 3. Unipolar Operation for 1/4 of MAX514

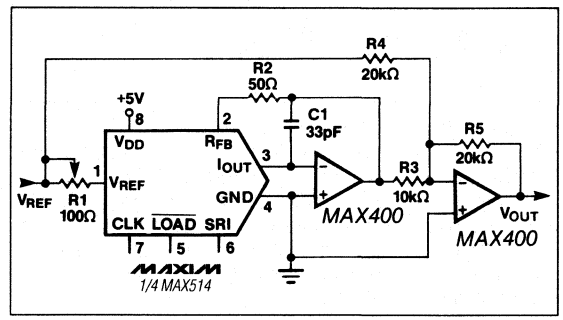


Figure 4. Bipolar Operation for 1/4 of MAX514

Table 1. Unipolar Binary Code Table for Circuit of Figure 3

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	0

Table 2. Offset Binary Code Table for Circuit of Figure 4

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

Table 3. Twos Complement Code Table

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
0111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0000	0
1111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

instruction to make the MAX514 work with twos-complement coding. Table 3 shows the code relationships to output voltage for the twos-complement operation.

To adjust the circuit, load the DAC with a code of 1000 0000 0000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is used to adjust the ratio of R3 and R4 for 0V out. Full-scale error can be trimmed by loading the DAC with all 0s or all 1s, and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. Gain adjustment will not be necessary in many applications, in which case resistors R1 and R2 in Figure 4 can be omitted. If gain trimming is desired, low tempco (<300ppm/°C) resistors should be used for R1 and R2.

Single-Supply Operation (Voltage Mode)

The MAX514 can be conveniently used in voltage mode with a single supply. I_{OUT} must not be allowed to go 0.3V lower than GND or 0.3V higher than V_{DD}. Otherwise, internal protection diodes may turn on, causing high current flow and possible damage to the device.

Figure 5 shows the MAX514 connected as a voltage-output DAC. I_{OUT} is connected to the reference voltage source and GND is grounded ($\overline{I_{OUTA}}$, on the SO package, should also be grounded). The DAC output now appears at the V_{REF} pin, which has a constant impedance equal to the reference input resistance (typically 11kΩ). This output should be buffered with an op amp when lower output impedance is required. The R_{FB} pin is not used in this mode.

The input impedance of the reference input (I_{OUT}) for this mode is code dependent, and the circuit response time

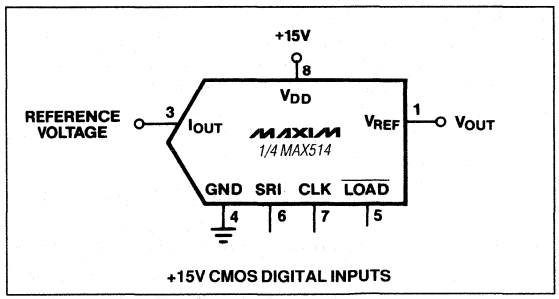


Figure 5. Single-Supply Operation for 1/4 of MAX514 Using Voltage Switching Mode

depends on the reference source's behavior with changing load conditions.

Since a negative reference is not required for a positive output when operating in voltage mode, the complete circuit can be powered from a single supply. Note that, when operating in voltage mode, the reference input (I_{OUT}) must always be positive and is limited to no more than 2.5V when V_{DD} is 15V. If the reference voltage is greater than 2.5V or V_{DD} is reduced, resistance mismatches in the DAC's internal NMOS switches result in degraded integral nonlinearity (INL) and differential nonlinearity (DNL).

The unipolar and bipolar circuits in Figures 3 and 4 can all be converted to voltage output mode.

Applications Information

Output Amplifier Offset

For best linearity, I_{OUT}, $\overline{I_{OUTA}}$, and GND should be terminated at exactly 0V. In most applications, I_{OUT} is connected to the summing junction of an inverting op amp. The amplifier's input offset voltage can degrade the DAC's linearity by causing I_{OUT} to be terminated to a non-zero voltage. The resulting error is:

$$\text{Error Voltage} = V_{OS}\,(1 + R_{FB} / R_O)$$

where V_{OS} is the op amp's offset voltage and R_O is the output resistance of the DAC. R_O is a function of the digital input code, and varies from approximately 11kΩ to 33kΩ. The error voltage range is then typically 4/3V_{OS} to 2V_{OS}, a change of 2/3V_{OS}. An amplifier with 3mV of offset, therefore, degrades linearity by 2mV — almost a full LSB when a 10V reference voltage is used. For best linearity, amplifiers with low offset voltage (such as the MAX400) should be used as output amplifiers for the MAX514. A good rule of thumb is that V_{OS} should be no more than 1/10LSB.

The output-amplifier input bias current (I_B) can also limit performance since I_B x R_{FB} generates an offset error. I_B should, therefore, be much less than the DAC output

CMOS Quad, 12-Bit, Serial-Input Multiplying DAC

current for 1LSB, which is typically 250nA with a 10V reference voltage. One-tenth of this value, 25nA, is recommended. Offset and linearity can also be impaired if the output amplifier noninverting input is grounded through a "bias-current compensation resistor." This resistor adds to the offset at this pin and should not be used. Best performance is obtained when the noninverting input is directly connected to GND.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op amp must be considered.

Another error source in dynamic applications is parasitic signal coupling from the V_{REF} inputs to I_{OUT}. This coupling is primarily a function of board layout and lead-to-lead package capacitance. Noise signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is usually dependent upon the circuit-board layout and on-chip capacitive coupling. Guard traces between the digital input, V_{REF} inputs, and I_{OUT} pins minimize layout-induced feedthrough. Each DAC output follows the digital inputs when the corresponding $\overline{LOAD}$ pin is low. In this state, invalid outputs and voltage glitches can appear at the DAC outputs. Keeping the $\overline{LOAD}$ inputs high until all of the data is shifted into the DAC eliminates this problem.

Compensation

A compensation capacitor, C1, may be required when the DAC is used with a high-speed output amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC output capacitance, C_{OUT}, and the internal feedback resistor, R_{FB}. The value of this capacitor depends on the type of op amp used, but it typically ranges from 10pF to 33pF. Too small a value causes output ringing, while excessive capacitance overdamps the output. The size of C1 can be minimized and the output voltage settling time improved by keeping the circuit-board trace and stray capacitance at I_{OUT} at low as possible.

The capacitance at each I_{OUT} pin (C_{OUT}) is code dependent and is typically 55pF with all switches connected to GND, and 85pF with all switches connected to I_{OUT}.

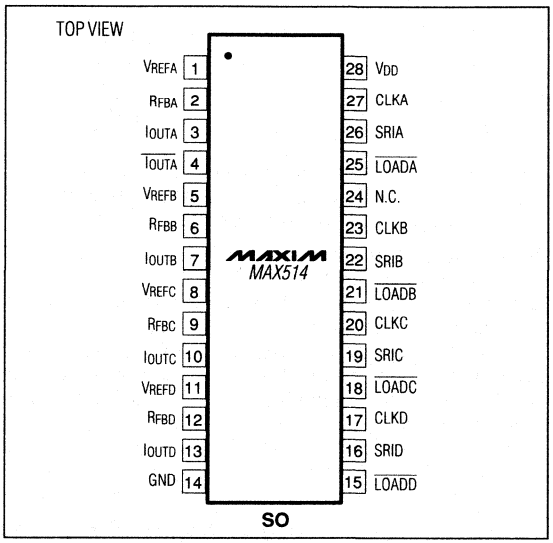
Grounding and Bypassing

Since I_{OUT} and the noninverting input of the output amplifier are sensitive to offset voltages, nodes that are to be grounded should be connected directly to a "single point" ground through a separate, low-resistance (less than 0.2Ω) connection. The current at I_{OUT} and GND varies with input code, creating a code-dependent error if these terminals are connected to GND (or a "virtual ground") through a resistive path.

A 1µF bypass capacitor, in parallel with a 0.01µF ceramic capacitor, should be connected across the DAC V_{DD} and GND as close to the pins as possible.

The MAX514 has high-impedance digital inputs. To minimize noise pick-up and prevent static charge accumulation if the pins are left floating (such as when a circuit card is left unconnected), they should be tied to either V_{DD} or GND through high-value resistors (1MΩ).

Pin Configurations (continued)



19-4500; Rev. 1; 5/92

MAXIM

Calibrated Quad 12-Bit Voltage-Output D/A Converters

General Description

The MAX526/MAX527 contain four 12-bit, voltage-output digital-to-analog converters (DACs). Precision output buffer amplifiers are included on-chip to provide voltage outputs. The MAX527 operates with ±5V power supplies, while the MAX526 utilizes -5V and +12V to +15V supplies. Offset, gain, and linearity are factory calibrated to provide the MAX526's 1LSB total unadjusted error (TUE).

These devices feature double-buffered interface logic with a 12-bit input register and a 12-bit DAC register. Data in the DAC register sets the DAC output voltage. The MAX526/MAX527 have an 8-bit-wide data bus. Data is loaded into the input register using two write operations with an 8-bit LSB write load and a 4-bit MSB write load. An asynchronous load DAC ($\overline{LDAC}$) input transfers data from the input register to the DAC register. All logic inputs are TTL and CMOS compatible.

The MAX526/MAX527 are available in 24-pin, 300 mil plastic DIP, Ceramic SB, and wide SO packages.

Applications

Minimum Component Count Analog Systems

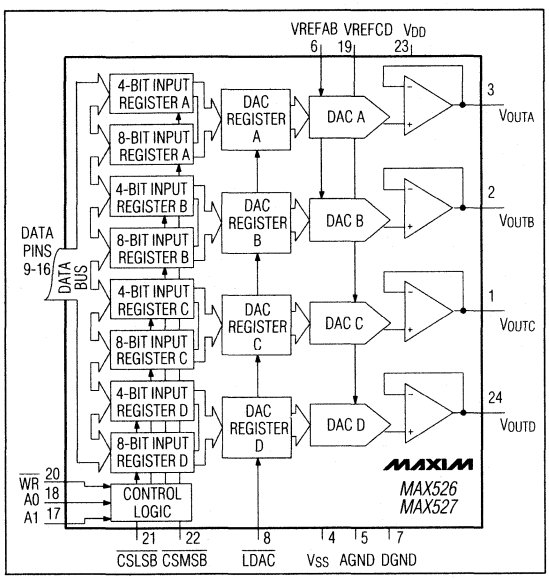
Digital Offset/Gain Adjustment

Arbitrary Function Generators

Industrial Process Controls

Automatic Test Equipment

Functional Diagram



Features

- ♦ **Full 12-Bit Performance Without Adjustments**
- ♦ **1LSB Total Unadjusted Error (MAX526)**
- ♦ **Buffered Voltage Outputs**
- ♦ **Fast Output Settling**
  3µs for MAX526
  5µs for MAX527
- ♦ **Double-Buffered Digital Inputs**
- ♦ **Microprocessor and TTL/CMOS Compatible**
- ♦ **±5V Supply Operation (MAX527)**

Ordering Information

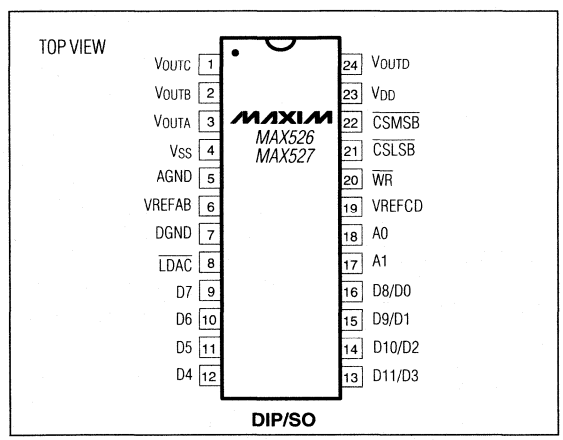
PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX526ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX526BCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX526ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX526BCWG	0°C to +70°C	24 Wide SO	±1
MAX526BC/D	0°C to +70°C	Dice*	±1
MAX526AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX526BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX526AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX526BEWG	-40°C to +85°C	24 Wide SO	±1
MAX526AMYG	-55°C to +125°C	24 Narrow Ceramic SB**	±1/2
MAX526BMYG	-55°C to +125°C	24 Narrow Ceramic SB**	±1

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

***Contact factory for availability and processing to MIL-STD-883.*

Pin Configuration



Calibrated Quad 12-Bit Voltage-Output D/A Converters

ABSOLUTE MAXIMUM RATINGS – MAX526

V_{DD} to AGND or DGND ..... -0.3V, +17V
V_{SS} to AGND or DGND ..... -7V, +0.3V
Digital Input Voltage to AGND or DGND .... 0.3V, V_{DD} + 0.3V
VREF to AGND or DGND ..... -0.3V, V_{DD} + 0.3V
V_{OUT} to AGND or DGND ..... V_{DD}, V_{SS}
Maximum Current into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 13.33mW/°C above +70°C) 733mW
Wide SO (derate 11.76mW/°C above +70°C) 647mW
Ceramic SB (derate 14.29mW/°C above +70°C) ... 1143mW

Operating Temperature Ranges:
MAX526_C_G ..... 0°C to +70°C
MAX526_E_G ..... -40°C to +85°C
MAX526_MYG ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX526

(V_{DD} = +15V, V_{SS} = -5V, VREF = 10V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE – ANALOG SECTION (R_L = 5kΩ, C_L = 100pF)							
Resolution	N			12			Bits
Total Unadjusted Error	TUE	MAX526A				±1.0	LSB
		MAX526B				±2.0	
		MAX526AC				±2.0	
		MAX526BC				±3.0	
		MAX526AE				±2.5	
		MAX526BE				±3.5	
		MAX526AM				±3.0	
		MAX526BM				±4.0	
Integral Nonlinearity	INL	MAX526A			±0.15	±0.50	LSB
		MAX526B				±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error		MAX526A	T_A = +25°C			±1.0	LSB
		MAX526B				±2.0	
		MAX526AC				±2.0	
		MAX526BC				±3.0	
		MAX526AE				±2.5	
		MAX526BE				±3.5	
		MAX526AM				±3.0	
		MAX526BM				±4.0	
Gain Error					-0.1	±1.0	LSB
Power-Supply Rejection	$\Delta Gain/\Delta V_{DD}$	V_{DD} from +10.8V to +16.5V	T_A = +25°C		±0.001	±0.01	LSB/%
	$\Delta Gain/\Delta V_{SS}$	V_{SS} from -4.5V to -5.5V			±0.001	±0.01	
	$\Delta Offset/\Delta V_{DD}$	V_{DD} from +10.8V to +16.5V			±0.007	±0.075	
	$\Delta Offset/\Delta V_{SS}$	V_{SS} from -4.5V to -5.5V			±0.003	±0.03	
MATCHING PERFORMANCE							
Total Unadjusted Error	TUE	MAX526AC/AE	T_A = +25°C			±1.0	LSB
		MAX526BC/BE				±2.0	
Gain Error			T_A = +25°C		0.1	±1.0	LSB
Offset Error		MAX526AC/AE	T_A = +25°C		0.5	±1.0	LSB
		MAX526BC/BE			0.5	±2.0	
Integral Nonlinearity	INL	MAX526AC/AE/BC/BE	T_A = +25°C		0.2	±1.0	LSB

ELECTRICAL CHARACTERISTICS – MAX526 (continued)

(V_{DD} = +15V, V_{SS} = -5V, VREF = 10V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
REFERENCE INPUT (Note 1)							
Reference Input Range	REF			2		V_{DD} - 4	V
Reference Input Resistance	RREF			5			kΩ
MULTIPLYING MODE PERFORMANCE							
Reference 3dB Bandwidth					700		kHz
Reference Feedthrough		Input code = all 0s	VREF = 10Vp-p at 400HZ		-100		dB
			VREF = 10Vp-p at 4000HZ		-82		
Total Harmonic Distortion plus Noise	THD+N	VREF = $2V_{p-p}$ at 50kHz			0.012		%
DIGITAL INPUTS							
Input High Voltage	V_{INH}			2.4			V
Input Low Voltage	V_{INL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}				1.0	µA
Input Capacitance	C_{IN}	(Note 2)				10	pF
DYNAMIC PERFORMANCE (R_L = 5kΩ, C_L = 100pF)							
Voltage-Output Slew Rate					5		V/µs
Output Settling Time		To ±1/2LSB of full scale			3		µs
Digital Feedthrough					5		nV-s
Digital Crosstalk					5		nV-s
POWER SUPPLIES							
Positive Supply Range	V_{DD}			10.8		16.5	V
Negative Supply Range	V_{SS}			-4.5		-5.5	V
Positive Supply Current	I_{DD}	(Note 3)	T_A = +25°C		11	20	mA
						28	
Negative Supply Current	I_{SS}	(Note 3)	T_A = +25°C		8	18	mA
						26	

Note 1: See *Reference Input* section.
Note 2: Guaranteed by design. Not production tested.
Note 3: Digital inputs at 2.4V; with digital inputs at 0V, I_{DD} decreases typically by 1.5mA at +25°C.

9

TIMING CHARACTERISTICS – MAX526

(V_{DD} = +15V, V_{SS} = -5V, VREF = 10V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width	t_{CS}		100			ns
$\overline{WR}$ Pulse Width	t_{WR}		100			ns
$\overline{CS}$ to $\overline{WR}$ Setup	t_{CWS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold	t_{CWH}		0			ns
Data Valid to $\overline{WR}$ Setup	t_{DS}		75			ns
Data to $\overline{WR}$ Hold	t_{DH}		10			ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}		120			ns
Address to $\overline{WR}$ Setup	t_{AS}		25			ns
Address to $\overline{WR}$ Hold	t_{AH}		0			ns

Calibrated Quad 12-Bit Voltage-Output D/A Converters

ABSOLUTE MAXIMUM RATINGS – MAX527

V_{DD} to AGND to DGND ..... -0.3V, +12V
V_{SS} to AGND to DGND ..... -7V, +0.3V
Digital Input Voltage to AGDN to DGND .... 0.3V, V_{DD} + 0.3V
VREF to AGND to DGND ..... -0.3V, V_{DD} + 0.3V
V_{OUT} to AGND to DGND ..... V_{DD}, V_{SS}
Maximum Current into Any Pin 50mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 13.33mW/°C above +70°C) 733mW
Wide SO (derate 11.76mW/°C above +70°C) 647mW
Ceramic SB (derate 14.29mW/°C above +70°C) ... 1143mW

Operating Temperature Ranges:
MAX527_C_G ..... 0°C to +70°C
MAX527_E_G ..... -40°C to +85°C
MAX527_MYG ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS – MAX527

(V_{DD} = +5V, V_{SS} = -5V, VREF = +2.5V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STATIC PERFORMANCE – ANALOG SECTION (R_L = 5kΩ, C_L = 100pF)							
Resolution	N			12			Bits
Integral Nonlinearity	INL	MAX527A			±0.15	±0.50	LSB
		MAX527B				±1	
Differential Nonlinearity	DNL	Guaranteed monotonic				±1	LSB
Offset Error		MAX527A	T_A = +25°C			±3	mV
		MAX527B				±6	
		MAX527AC				±6	
		MAX527BC				±9	
		MAX527AE				±7	
		MAX527BE				±11	
		MAX527AM				±9	
		MAX527BM				±12	
Gain Error					-0.1	±1.0	LSB
Power-Supply Rejection	ΔGain/ΔV_{DD}	V_{DD} from +4.5V to +5.5V	T_A = +25°C		±0.002	±0.02	LSB/%
	ΔGain/ΔV_{SS}	V_{SS} from -4.5V to -5.5V			±0.002	±0.02	
	ΔOffset/ΔV_{DD}	V_{DD} from +4.5V to +5.5V			±0.005	±0.05	
	ΔOffset/ΔV_{SS}	V_{SS} from -4.5V to -5.5V			±0.005	±0.05	
MATCHING PERFORMANCE							
Gain Error			T_A = +25°C		0.1	±1.0	LSB
Offset Error		MAX527AC/AE	T_A = +25°C		0.5	±5	LSB
		MAX527BC/BE			0.5	±10	
Integral Nonlinearity	INL	MAX527AC/AE/BC/BE	T_A = +25°C		0.2	±1.0	LSB
REFERENCE INPUT (Note 1)							
Reference Input Range	REF			1.2		V_{DD} - 2.20	V
Reference Input Resistance	RREF			5			kΩ

ELECTRICAL CHARACTERISTICS (continued) – MAX527

(V_{DD} = +5V, V_{SS} = -5V, VREF = +2.5V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MULTIPLYING MODE PERFORMANCE							
Reference 3dB Bandwidth					700		kHz
Reference Feedthrough		400Hz			-100		dB
		4000Hz			-82		
Total Harmonic Distortion plus Noise	THD+N	VREF = 850mV$_{p-p}$ at 100kHz			0.024		%
DIGITAL INPUTS							
Input High Voltage	V_{INH}			2.4			V
Input Low Voltage	V_{INL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}				1.0	µA
Input Capacitance	C_{IN}	(Note 2)				10	pF
DYNAMIC PERFORMANCE (R_L = 5kΩ, C_L = 100pF)							
Voltage-Output Slew Rate					3		V/µs
Output Settling Time		To ±1/2LSB of full scale			5		µs
Digital Feedthrough					5		nV-s
Digital Crosstalk					5		nV-s
POWER SUPPLIES							
Positive Supply Range	V_{DD}			4.75		5.5	V
Negative Supply Range	V_{SS}			-4.5		-5.5	V
Positive Supply Current	I_{DD}	Note 4	T_A = +25°C		5.5	12	mA
						18	
Negative Supply Current	I_{SS}	Note 4	T_A = +25°C		3.6	10	mA
						16	

Note 1: See *Reference Input* section.
Note 2: Guaranteed by design. Not production tested.
Note 4: Digital inputs at 2.4V.

TIMING CHARACTERISTICS – MAX527

(V_{DD} = +5V, V_{SS} = -5V, VREF = +2.5V, AGND = DGND = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

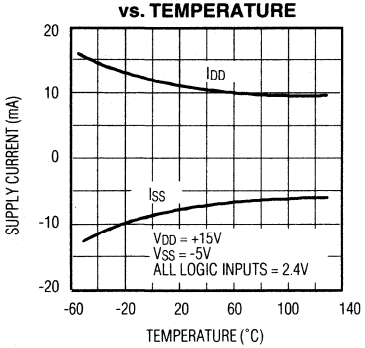
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width	t_{CS}	MAX527_C/E	180			ns
		MAX527_M	200			
$\overline{WR}$ Pulse Width	t_{WR}	MAX527_C/E	180			ns
		MAX527_M	200			
$\overline{CS}$ to $\overline{WR}$ Setup	t_{CWS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold	t_{CWH}		0			ns
Data Valid to $\overline{WR}$ Setup	t_{DS}		75			ns
Data to $\overline{WR}$ Hold	t_{DH}		0			ns
$\overline{LDAC}$ Pulse Width	t_{LDAC}	MAX527_C/E	120			ns
		MAX527_M	150			
Address to $\overline{WR}$ Setup	t_{AS}		25			ns
Address to $\overline{WR}$ Hold	t_{AH}		0			ns

Calibrated Quad 12-Bit Voltage-Output D/A Converters

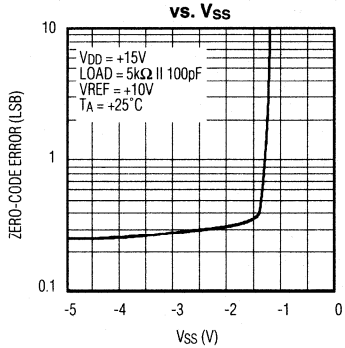
Typical Operating Characteristics

MAX526

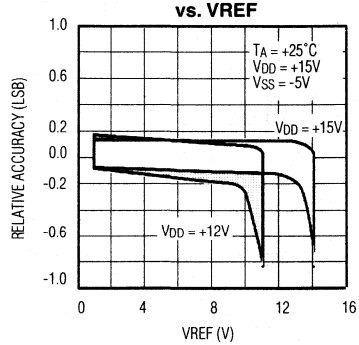
MAX526
SUPPLY CURRENT
vs. TEMPERATURE



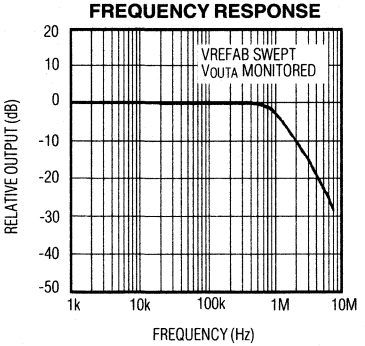
MAX526
OFFSET ERROR
vs. VSS



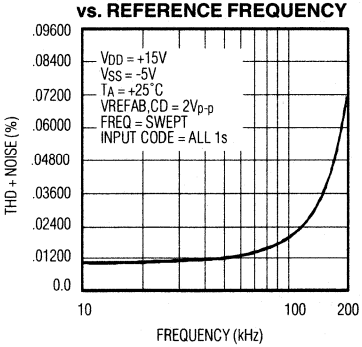
MAX526
RELATIVE ACCURACY
vs. VREF



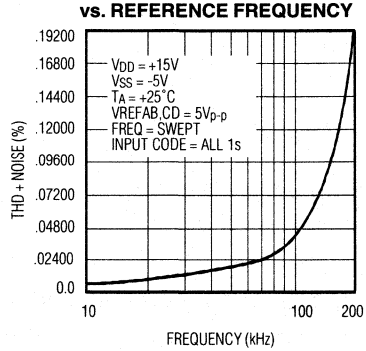
MAX526
REFERENCE VOLTAGE INPUT
FREQUENCY RESPONSE



MAX526
THD + NOISE AT DAC OUTPUT
vs. REFERENCE FREQUENCY



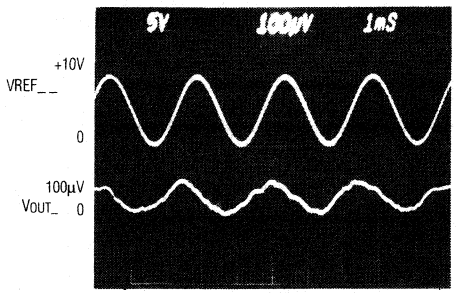
MAX526
THD + NOISE AT DAC OUTPUT
vs. REFERENCE FREQUENCY



Calibrated Quad 12-Bit Voltage-Output D/A Converters

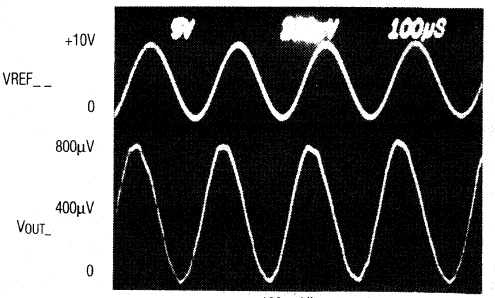
Typical Operating Characteristics (continued)

MAX526
REFERENCE
FEEDTHROUGH AT 400Hz



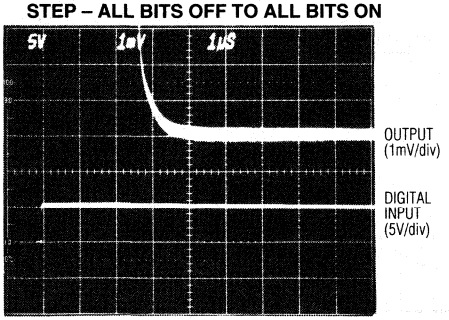
1ms/div
TOP: REFERENCE IN 5V/div
BOTTOM: V_{OUTA} 100µV/div
INPUT CODE = ALL 0s

MAX526
REFERENCE
FEEDTHROUGH AT 4000Hz



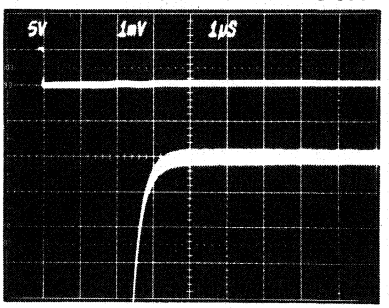
100µs/div
TOP: REFERENCE IN 5V/div
BOTTOM: V_{OUTA} 200µV/div
INPUT CODE = ALL 0s

MAX526
POSITIVE SETTLING TIME TO FULL-SCALE STEP – ALL BITS OFF TO ALL BITS ON



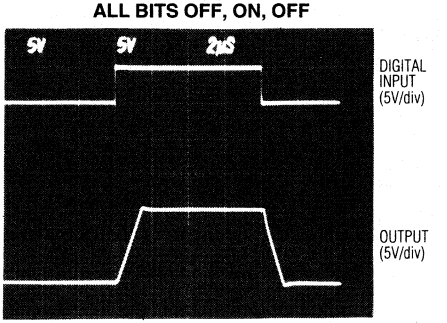
VREF = 10V, C_L = 100pF, R_L = 5kΩ

MAX526
NEGATIVE SETTLING TIME TO FULL-SCALE STEP – ALL BITS ON TO ALL BITS OFF



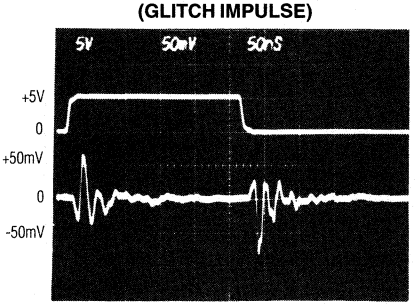
VREF = 10V, C_L = 100pF, R_L = 5kΩ

MAX526
DYNAMIC RESPONSE
ALL BITS OFF, ON, OFF



V_{DD} = +15V, V_{SS} = -5V, VREF = 10V, C_L = 100pF, R_L = 5kΩ

MAX526
DIGITAL FEEDTHROUGH
(GLITCH IMPULSE)



50ns/div
TOP: DIGITAL TRANSITION ON ALL DATA BITS 5V/div
BOTTOM: DAC OUPUT WITH $\overline{WR}$ HIGH 50mV/div

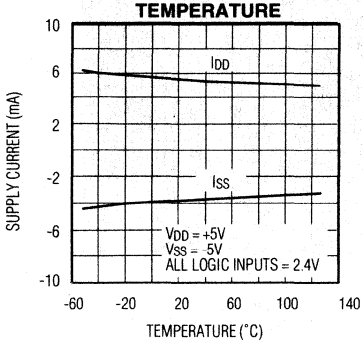
9

Calibrated Quad 12-Bit Voltage-Output D/A Converters

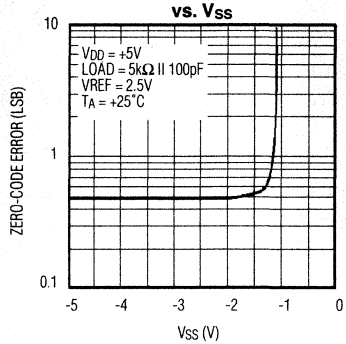
Typical Operating Characteristics

MAX527

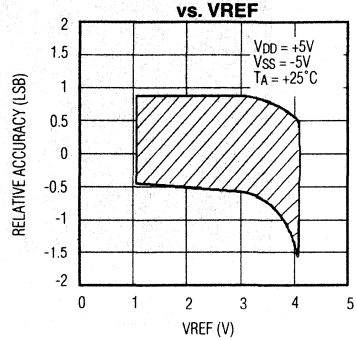
MAX527 SUPPLY CURRENT vs. TEMPERATURE



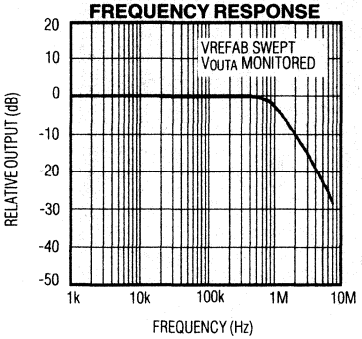
MAX527 OFFSET ERROR vs. VSS



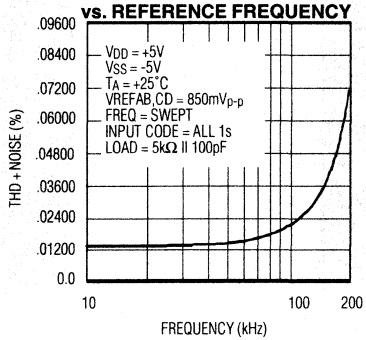
MAX527 RELATIVE ACCURACY vs. VREF



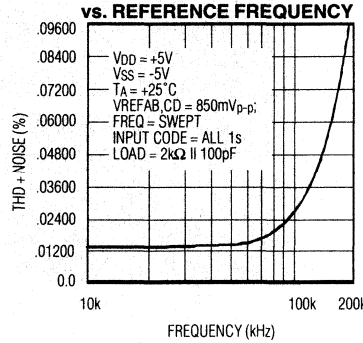
MAX527 REFERENCE VOLTAGE INPUT FREQUENCY RESPONSE



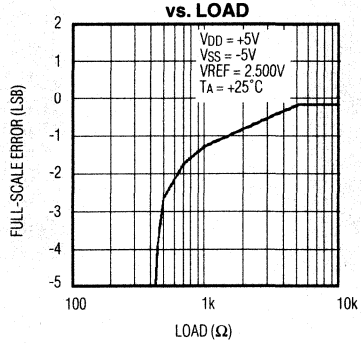
MAX527 THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY



MAX527 THD + NOISE AT DAC OUTPUT vs. REFERENCE FREQUENCY

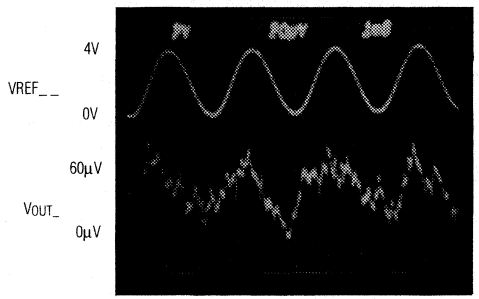


MAX527 FULL-SCALE ERROR vs. LOAD



Typical Operating Characteristics (continued)

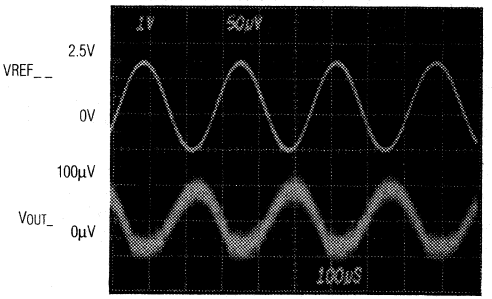
MAX527
REFERENCE
FEEDTHROUGH AT 400Hz



1ms/div

TOP: REFERENCE IN 2V/div
BOTTOM: VOUTA 20µV/div
INPUT CODE = ALL 0s

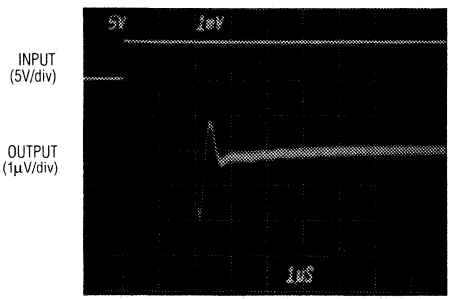
MAX527
REFERENCE
FEEDTHROUGH AT 4000Hz



100µs/div

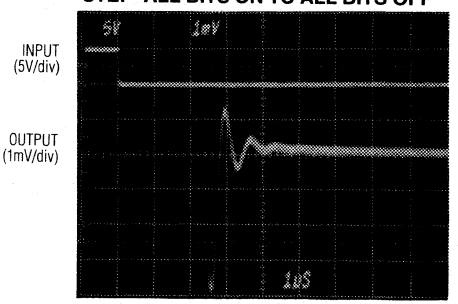
TOP: REFERENCE IN 5V/div
BOTTOM: VOUTA 50µV/div
INPUT CODES = ALL 0s

MAX527
POSITIVE SETTLING TIME TO FULL-SCALE STEP–ALL BITS OFF TO ALL BITS ON



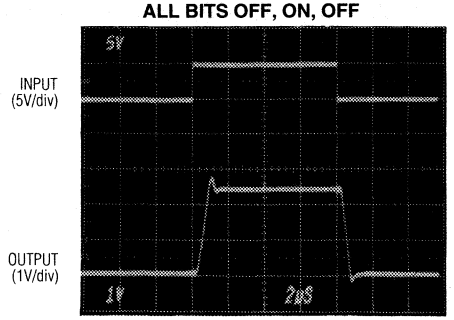
C_L = 100pF, R_L = 5kΩ, VREF = 2.5V

MAX527
NEGATIVE SETTLING TIME TO FULL-SCALE STEP–ALL BITS ON TO ALL BITS OFF



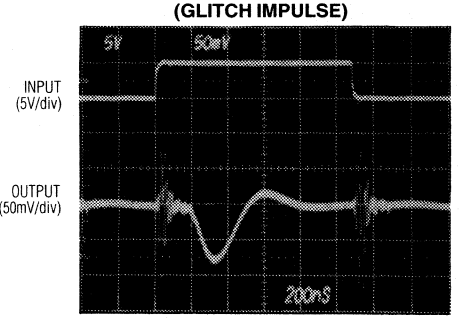
C_L = 100pF, R_L = 5kΩ, VREF = 2.5V

MAX527
DYNAMIC RESPONSE
ALL BITS OFF, ON, OFF



V_{DD} = +15V, V_{SS} = -5V, VREF = 2.5V, C_L = 100pF; R_L = 5kΩ

MAX527
DIGITAL FEEDTHROUGH
(GLITCH IMPULSE)



200ns/div

TOP: DIGITAL TRANSITION ON ALL DATA BITS 5V/div
BOTTOM: DAC OUPUT WITH WR HIGH 50mV/div

Calibrated Quad 12-Bit Voltage-Output D/A Converters

Pin Description

PIN	NAME	FUNCTION
1	V_{OUTC}	DAC C Output Voltage
2	V_{OUTB}	DAC B Output Voltage
3	V_{OUTA}	DAC A Output Voltage
4	V_{SS}	Negative Power Supply
5	AGND	Analog Ground
6	VREFAB	Reference Voltage Input for DAC A and DAC B
7	DGND	Digital Ground
8	$\overline{LDAC}$	Load DAC Input (active low). Driving this asynchronous input low transfers the contents of each input register to its respective DAC register.
9	D7	Data Bit 7
10	D6	Data Bit 6
11	D5	Data Bit 5
12	D4	Data Bit 4
13	D11/D3	Data Bit 11 (MSB) if $\overline{CSMSB}$ is low and $\overline{CSLSB}$ is high. Data Bit 3 (MSB) if $\overline{CSMSB}$ is high and $\overline{CSLSB}$ is low.
14	D10/D2	Data Bit 10 (MSB) if $\overline{CSMSB}$ is low and $\overline{CSLSB}$ is high. Data Bit 2 (MSB) if $\overline{CSMSB}$ is high and $\overline{CSLSB}$ is low.
15	D9//D1	Data Bit 9 (MSB) if $\overline{CSMSB}$ is low and $\overline{CSLSB}$ is high. Data Bit 1 (MSB) if $\overline{CSMSB}$ is high and $\overline{CSLSB}$ is low.
16	D8/D0	Data Bit 8 (MSB) if $\overline{CSMSB}$ is low and $\overline{CSLSB}$ is high. Data Bit 0 (MSB) if $\overline{CSMSB}$ is high and $\overline{CSLSB}$ is low.
17	A1	DAC Address Select Bit (MSB)
18	A0	DAC Address Select Bit (LSB)
19	VREFCD	Reference Voltage Input for DAC C and DAC D
20	$\overline{WR}$	Write Input (active low). $\overline{WR}$ along with $\overline{CSMSB}$ and $\overline{CSLSB}$ load data into the DAC input register selected by A1 and A0.
21	$\overline{CSLSB}$	Chip Select for LS Byte (active low). Selects the lower 8 bits of the addressed input register.
22	$\overline{CSMSB}$	Chip Select for MS Nibble (active low). Selects the upper 4 bits of the addressed input register.
23	V_{DD}	Positive Supply Voltage
24	V_{OUTD}	DAC D Output Voltage

Detailed Description

Analog Section

The MAX526/MAX527 contain four voltage output DACs. The DACs are "inverted" R-2R ladder networks that convert 12-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltages. The MAX526/MAX527 have two reference inputs: one shared by DAC A and DAC B (VREFAB), and the other shared by DAC C and DAC D (VREFCD). These inputs allow different full-scale output voltage ranges for each pair of DACs (Figure 1).

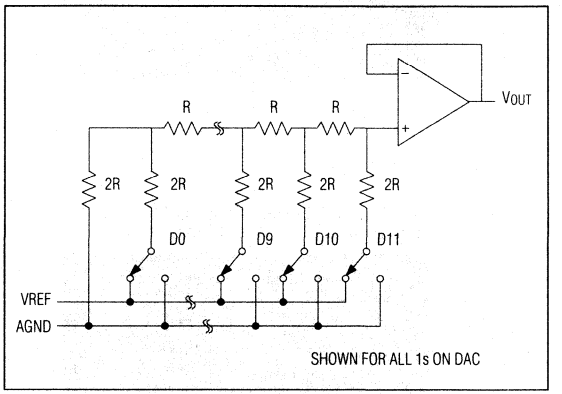


Figure 1. Simplified DAC Circuit Diagram

Reference Input

The MAX526/MAX527 can be used for multiplying applications. The reference accepts both DC and AC signals. The voltage at each VREF input sets the full-scale output voltages for its respective DACs. The input impedance of the VREF inputs are code dependent, with the lowest value (typically 6kΩ for VREFAB or VREFCD) occuring when the input code is 0101 0101 0101. The maximum value, typically 60kΩ, occurs when the input code is 0000 0000 0000. Since the input impedance at VREF is code dependent, load regulation of the reference used is important.

Calibrated Quad 12-Bit Voltage-Output D/A Converters

The guaranteed minimum input impedance of each reference input of the MAX526/MAX527 is 5kΩ. When the reference inputs are driven from the same source, the minimum impedance that must be driven by the reference source is 2.5kΩ. A voltage reference such as the MAX674 would typically deviate by 0.165LSB (0.33LSB worst case) when simultaneously driving both MAX526 reference inputs at 10V. Improve accuracy by driving VREFAB and VREFCD separately or by using a reference with superior load regulation, such as the MAX670/MAX671.

Using an op amp to buffer the reference is another way to obtain high accuracy. The closed-loop output impedance of the op amp should be kept below 0.05Ω. This ensures errors of less than 0.08LSB when driving both reference inputs simultaneously. The MAX400 or OP07 are suitable for this application. The input capacitance at VREF is also code dependent and typically varies from 125pF to 300pF.

V_{OUTA-D} are represented by a digitally programmable voltage source as:

$$V_{OUT} = (N_B \times VREF) / 4096$$

where N_B is the numeric value of the DAC's binary input code (0 to 4095).

Output Buffer Amplifiers

All MAX526/MAX527 voltage outputs are internally buffered by precision unity-gain followers with a typical slew rate of 5V/µs for the MAX526 and 3V/µs for the MAX527.

With a full-scale transition at the MAX526 output (0V to +10V or +10V to 0V), the typical settling time to ±1/2LSB is 3µs when loaded with 5kΩ in parallel with 100pF (loads less than 5kΩ degrade performance). Typical output dynamic response and settling performance of the MAX526 output amplifier are shown in the *Typical Operating Characteristics* section.

With a full-scale transition at the MAX527 output (0V to +2.5V or +2.5V to 0V), the typical settling time to ±1/2LSB is 5µs when loaded with 5kΩ in parallel with 100pF (loads less than 5kΩ degrade performance). Typical output dynamic response and settling performance of the MAX527 output amplifiers are shown in the *Typical Operating Characteristics* section.

Digital Inputs and Interface Logic

Digital inputs are compatible with both TTL and 5V CMOS logic. The MAX526/MAX527 interface with microprocessors using an 8-bit-wide data bus. The double-buffered input structure consists of a 12-bit (8 + 4) input register and a 12-bit DAC register for each of the four DACs.

Each DAC's analog output reflects the data held in its DAC register. Address lines A0 and A1 select which DAC receives data from the data bus, as shown in Table 1. All MAX526/MAX527 control inputs are level-triggered. Figure 2 shows the MAX526/MAX527 input control logic.

Table 1. DAC Addressing

A1	A0	SELECTED INPUT REGISTER
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

$\overline{CSMSB}$, $\overline{CSLSB}$, and $\overline{WR}$ load from the data bus to the input register selected by A0 and A1. Pulling $\overline{CSLSB}$ and $\overline{WR}$ low loads the lower 8 bits of the input register, while $\overline{CSMSB}$ and $\overline{WR}$ load the upper 4 bits. The order in which the data is loaded into the input register (i.e. upper 4 bits first or lower 8 bits first) is not important. It is possible to concurrently load the full 12 bits of the input register by pulling $\overline{CSLSB}$, $\overline{CSMSB}$, and $\overline{WR}$ low. Note that the same data will be written to the 4MSBs (D11-D8) and the 4LSBs (D3-D0), respectively. If the DACs are configured in the unipolar output mode (see Figure 5 and Table 3), this method can be used to quickly zero the DAC outputs.

Data is latched into the selected input register on the rising edge of $\overline{WR}$. Alternatively, data will be latched into

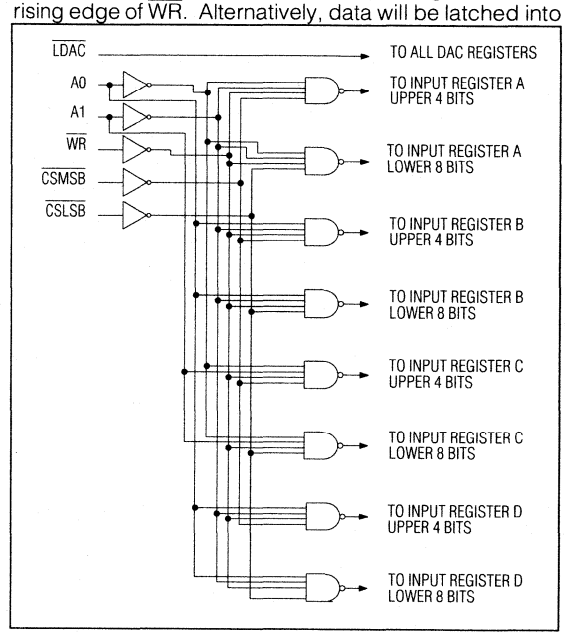


Figure 2. Input Control Logic

Calibrated Quad 12-Bit Voltage-Output D/A Converters

Table 2. Write-Cycle Truth Table

$\overline{CSLSB}$	$\overline{CSMSB}$	$\overline{WR}$	$\overline{LDAC}$	FUNCTION
L	H	L	H	Loads LS byte into selected input register
L	H	↓	H	Latches LS byte into selected input register
↓	H	L	H	Latches LS byte into selected input register
H	L	L	H	Loads MS nibble into selected input register
H	L	↓	H	Latches MS nibble into selected input register
H	↓	L	H	Latches MS nibble into selected input register
X	X	H	L	Transfers data from input registers into DAC registers. DAC outputs reflect data held in their respective input registers
H	H	H	↓	Latches the four DAC registers. Input registers cannot be written to.
H	L	L	L	Loads MS nibble into selected input register and loads input registers into DAC registers.
↓	X	H	H	No operation. Device is not selected.
L	L	L	L	Loads all 12 bits of selected input register. Transfers data from input registers into DAC registers. DAC outputs reflect data held in their respective input registers.
L	L	L	H	Loads all 12 bits into selected input register.
L	H	L	L	Loads LS byte into selected input register. Transfers data from input registers into DAC registers. DAC outputs reflect data held in their respective input registers.
H	H	L	L	Transfers data from input registers into DAC registers. DAC outputs reflect data held in their respective input registers.
H	H	L	H	No operation

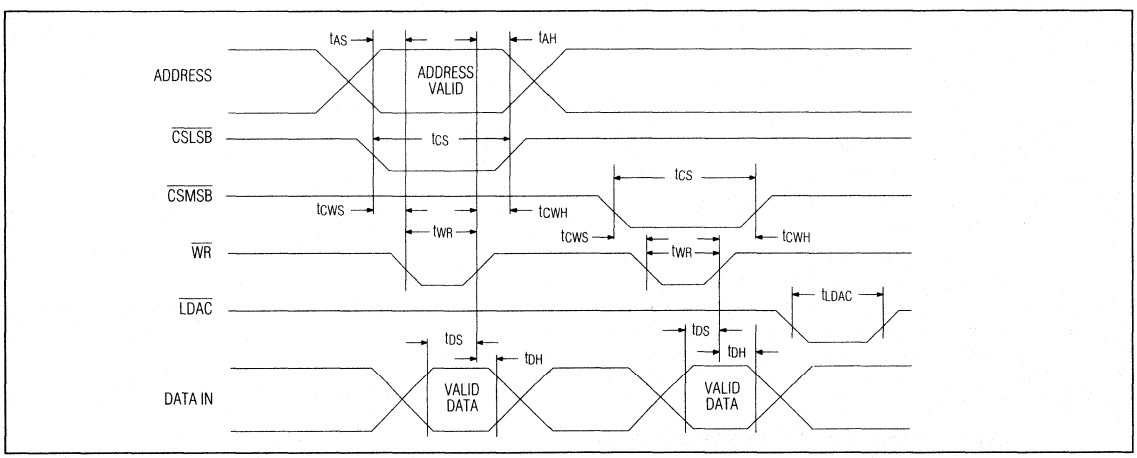


Figure 3. Write-Cycle Timing

the lower 8 bits of the input register on the rising edge of CSLSB, and the upper 4 bits will be latched on the rising edge of CSMSB.

Data is transferred from all input registers to the DAC registers by pulling LDAC low. This simultaneously updates all four DACs. Since LDAC is asynchronous with respect to WR, be sure that incorrect data is not latched to the output. Table 2 shows the truth table for operation of WR, LDAC, CSLSB, and CSMSB. Figure 3 shows the MAX526 /MAX527write-cycle timing.

Application Information

Ground Management

Digital or AC transient signals between AGND and DGND can create noise at the analog outputs. It is recommended that AGND and DGND be tied together at the DAC and that this point be tied to the highest quality ground available. If separate ground buses are used, two clamp diodes (1N914 or equivalent) should be connected in inverse parallel between AGND and DGND. This will ensure that the two ground pins always remain within one diode drop of each other.

Careful PCB ground layout minimizes crosstalk between DAC outputs, reference inputs, and digital inputs. Figure 4 shows a suggested circuit-board layout for minimizing crosstalk.

Unipolar Output

In unipolar operation, the output voltages and the reference inputs are the same polarity. Figure 5 shows the MAX526/MAX527 unipolar output circuit. The unipolar output codes are listed in Table 3.

Table 3. Unipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+VREF\left(\frac{4095}{4096}\right)$
1000 0000 0001	$+VREF\left(\frac{2049}{4096}\right)$
1000 0000 0000	$+VREF\left(\frac{2048}{4096}\right)=\frac{+VREF}{2}$
0111 1111 1111	$+VREF\left(\frac{2047}{4096}\right)$
0000 0000 0001	$+VREF\left(\frac{1}{4096}\right)$
0000 0000 0000	0V

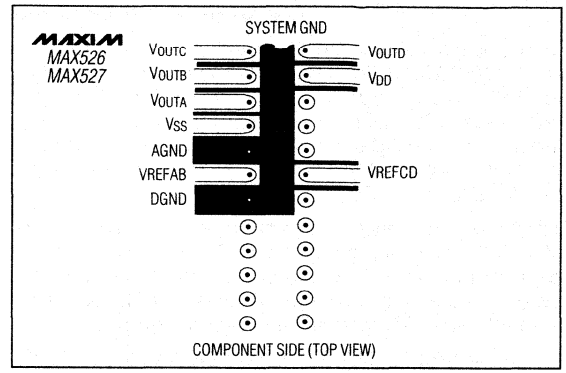


Figure 4. Suggested PCB Layout for Minimizing Crosstalk

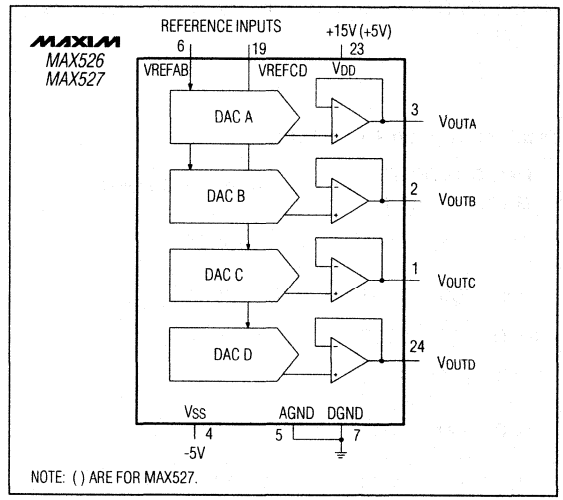


Figure 5. Unipolar Output Circuit

Bipolar Output

The MAX526/MAX527 outputs may be configured for bipolar output operation using Figure 6's circuit. One op amp and two resistors are required per channel. With R1 = R2:

$$V_{OUT} = VREF\ ((2N_B / 4096) - 1)$$

where N_B is the numeric value of the DAC's binary input code.

Table 4 shows the digital code vs. output voltage for the circuit in Figure 6.

Calibrated Quad 12-Bit Voltage-Output D/A Converters

Using an AC Reference

In applications where VREF has AC signal components, the MAX526/MAX527 have multiplying capability within the VREF input range specifications. Figure 7 shows a technique for applying a sine wave signal to the reference input where the AC signal is offset before being applied to VREF. Note that VREF must never be more negative than DGND.

Total harmonic distortion plus noise (THD + N) of the MAX526 is typically less than 0.012% with input frequencies up to 35kHz for $5V_{p-p}$ swing; up to 50kHz for 2V swing. The typical -3dB frequency is 700kHz, as shown in the *Typical Operating Characteristics* graphs.

For the MAX527, THD + N is typically less than 0.024% with input frequencies greater than 100kHz, a signal amplitude of 850mV, and a load of 5kΩ in parallel with 100pF. With a 2kΩ load in parallel with 100pF, the MAX527's THD is below 0.024% for input frequencies up to 95kHz.

Table 4. Bipolar Code Table

DAC CONTENTS MSB LSB	ANALOG OUTPUT
1111 1111 1111	$+VREF\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+VREF\left(\frac{1}{2048}\right)$
1000 0000 0000	0V
0111 1111 1111	$-VREF\left(\frac{1}{2048}\right)$
0000 0000 0001	$-VREF\left(\frac{2047}{2048}\right)$
0000 0000 0000	$-VREF\left(\frac{2048}{2048}\right) = -VREF$

NOTE: $1LSB = (VREF)\left(\frac{1}{4096}\right)$

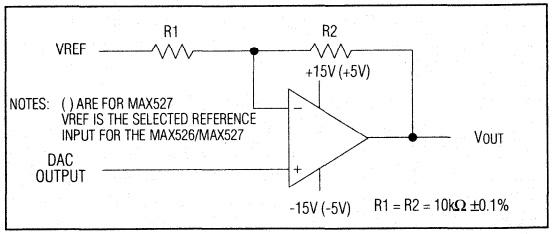


Figure 6. Bipolar Output Circuit

Offsetting AGND

AGND can be biased above DGND to provide an arbitrary nonzero output voltage for a "0" input code. This application is shown in Figure 8. The output voltage at V_{OUTA} is:

$$V_{OUTA} = V_{BIAS} + N_B \times V_{IN}$$

where N_B is the numeric value of the DAC's binary input code. Since AGND is common to all four DACs, all outputs will be offset by V_{BIAS} in the same manner. Note that AGND should not be biased more negative than DGND

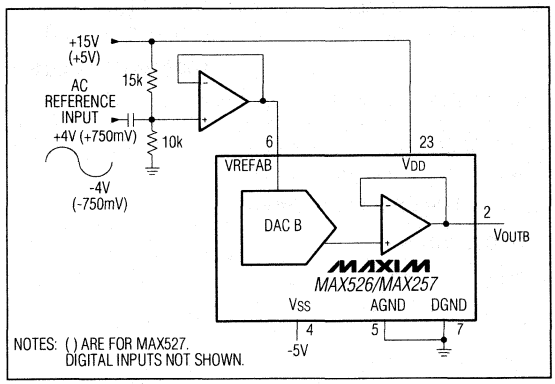


Figure 7. AC Reference Input Circuit

Supply Voltage and Decoupling

For full MAX526 performance, V_{DD} should be 4V higher than VREF in the 10.8V to 16.5V range. When using the MAX527, V_{DD} should be at least 2.2V higher than VREF in the 4.75V to 5.5V range. Both V_{DD} and V_{SS} supplies should be bypassed with a 4.7µF capacitor in parallel with a 0.1µF capacitor to AGND, with short lead lengths as close to the supply pins as possible.

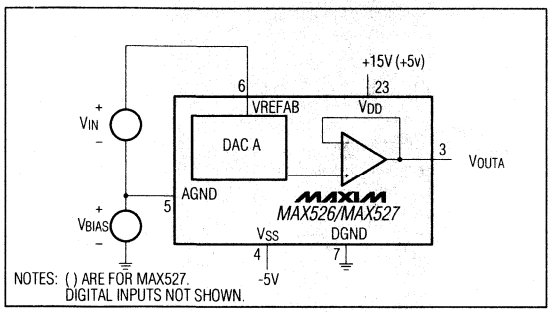


Figure 8. AGND Bias Circuit

Power-Supply Sequencing

On power-up, V_{SS} should come up first, V_{DD} next, followed by VREFAB or VREFCD. If supply sequencing is not possible, tie an external Schottky diode between V_{SS} and AGND as shown in Figure 9.

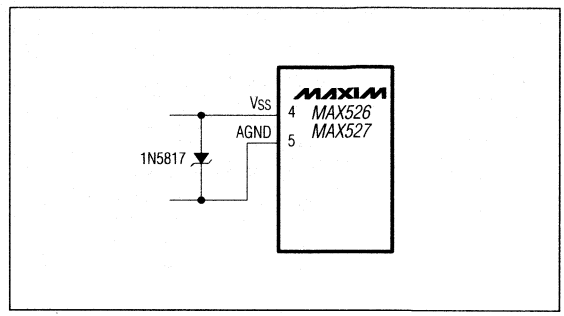


Figure 9. When V_{SS} and V_{DD} cannot be sequenced, tie a Schottky diode between V_{SS} and AGND.

9

Calibrated Quad 12-Bit Voltage-Output D/A Converters

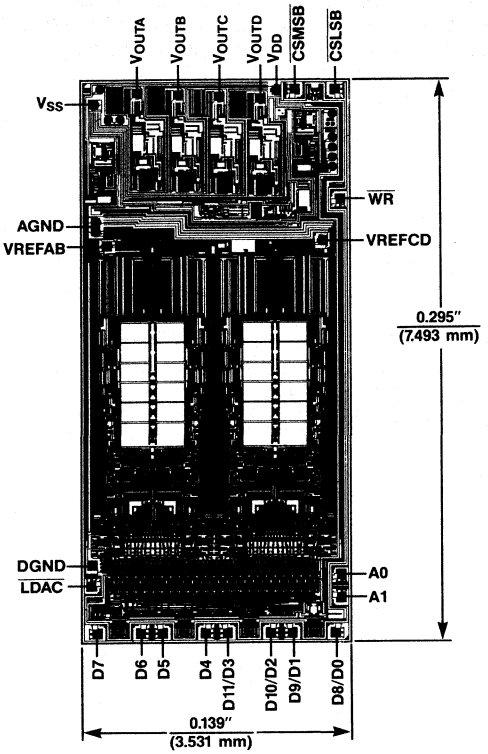
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSBs)
MAX527ACNG	0°C to +70°C	24 Narrow Plastic DIP	±1/2
MAX527BCNG	0°C to +70°C	24 Narrow Plastic DIP	±1
MAX527ACWG	0°C to +70°C	24 Wide SO	±1/2
MAX527BCWG	0°C to +70°C	24 Wide SO	±1
MAX527BC/D	0°C to +70°C	Dice*	±1
MAX527AENG	-40°C to +85°C	24 Narrow Plastic DIP	±1/2
MAX527BENG	-40°C to +85°C	24 Narrow Plastic DIP	±1
MAX527AEWG	-40°C to +85°C	24 Wide SO	±1/2
MAX527BEWG	-40°C to +85°C	24 Wide SO	±1
MAX527AMYG	-55°C to +125°C	24 Narrow Ceramic SB**	±1/2
MAX527BMYG	-55°C to +125°C	24 Narrow Ceramic SB**	±1

** Contact factory for dice specifications.*
***Contact factory for availability and processing to MIL-STD-883.*

Chip Topography

MAX526/MAX527



SUBSTRATE CONNECTS TO V_{DD};
TRANSISTOR COUNT: 2720.

19-4193; Rev 1; 3/92

MAXIM

Octal 8-Bit Serial DACs with Output Buffer

General Description

The MAX528/MAX529 are monolithic devices consisting of an octal 8-bit voltage-output digital-to-analog converter (DAC) with a serial interface and two reference inputs. The MAX528 operates from a single supply up to +15V or from split supplies totaling up to 20V, including +5V/-15V, +12V/-5V, and +15V/-5V. The MAX529 operates from a single +5V supply or from ±5V split supplies. For both parts, a shutdown pin reduces current consumption to under 50µA, while retaining all internal DAC data.

Three output modes are serially programmable for each pair of 8 analog outputs. An unbuffered mode connects the internal R-2R DAC network directly to the output pin, reducing power consumption and avoiding the buffer's DC errors. A full-buffered mode inserts a buffer between the R-2R network and the output, providing +5mA/-2mA output drive. Half-buffered output mode is similar, but uses less power while still providing up to +5mA of output drive in a unipolar output configuration.

Serial data can be "daisy-chained" from one device to another. On power-up, all data bits are reset to 0, and analog outputs enter the unbuffered mode.

Applications

Digital Gain and Offset Adjustment

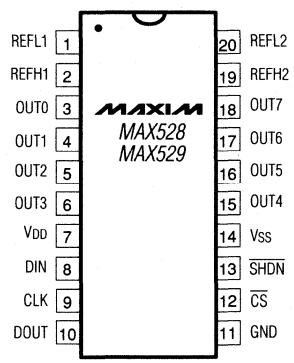
Digital Calibration

Multiple Trim Pot Replacement

Microcontrolled Analog Outputs

Pin Configurations

TOP VIEW



DIP

Wide SO on last page

Features

- ♦ **8 Buffered Noninverting Outputs**
- ♦ **Buffer Disable Control**
- ♦ **2 Pairs of Differential Reference Inputs**
- ♦ **3-Wire Serial Interface**
- ♦ **Single +5V or Dual ±5V Supply Opertion (MAX529)**
- ♦ **Low-Power Shutdown**
- ♦ **Stable Driving Output Capacitance Loads**

Ordering Information

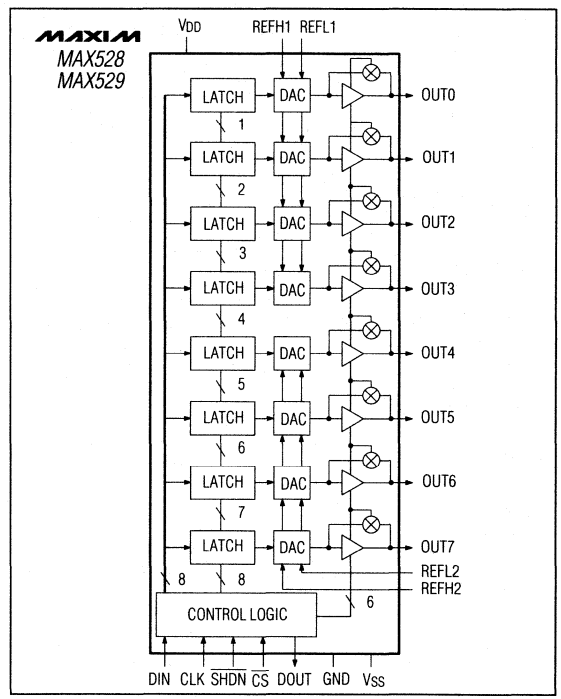
PART	TEMP. RANGE	PIN-PACKAGE
MAX528CPP	0°C to +70°C	20 Plastic DIP
MAX528CWG	0°C to +70°C	24 Wide SO
MAX528C/D	0°C to +70°C	Dice*
MAX528EPP	-40°C to +85°C	20 Plastic DIP
MAX528EWG	-40°C to +85°C	24 Wide SO
MAX528MJP	-55°C to +125°C	20 CERDIP**

Ordering Information continued on last page.

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Functional Diagram



9

Octal 8-Bit Serial DACs with Output Buffer

ABSOLUTE MAXIMUM RATINGS - MAX528

V_{DD} to GND ..... -0.3V to +17V
V_{DD} to V_{SS} ..... -0.3V to +22V
V_{SS} to GND ..... -17V to +0.3V
REFH1 - REFL1, REFH2 - REFL2 ..... -0.3V to +12V
REFH1 - V_{SS}, REFH2 - V_{SS} ..... +17V
REFH1, REFH2 ..... REFL_ - 0.3V to V_{DD} + 0.3V
REFL1, REFL2 ..... V_{SS} - 0.3V to REFH_ + 0.3V
OUT(1-8) ..... V_{SS} - 0.3V to V_{DD} + 0.3V
OUT(1-8) to V_{SS} ..... +17V
OUT(1-8) Current ..... ±20mA
DIN, CLK, CS, DOUT ..... -0.3V to V_{DD} + 0.3V
SHDN ..... V_{SS} - 0.3V to V_{DD} + 0.3V

DOUT Current ..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX528C_ _ ..... 0°C to +70°C
MAX528E_ _ ..... -40°C to +85°C
MAX528MJP ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS - MAX528

(Unbuffered Mode: V_{DD} = +12V, V_{SS} = 0V; Full-Buffered Mode: V_{DD} = +12V, V_{SS} = -5V; GND = 0V, REFH = +5V, REFL = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	UNBUFFERED MODE (Note 1)			FULL-BUFFERED MODE (Note 2)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC PERFORMANCE									
Resolution			8			8			Bits
Relative Accuracy (Note 3)	RLE			±0.3	±1.0		±0.3	±1.0	LSB
Differential Nonlinearity (Note 4)	DNL	Guaranteed monotonic		±0.3	±1.0		±0.3	±1.0	LSB
Full-Scale Error	FSE	R_{LOAD} = open			±1/2				LSB
Gain Error (Note 5)		R_{LOAD} = open					-0.2		%
		R_{LOAD} = 5kΩ				0.0	-1.3	-2.5	%
Zero-Code Error					±5			±60	mV
Zero-Code Tempco				±5			±100		µV/°C
DAC Output Resistance	R_{OUT}		8.5k	13k	20k		55	100	Ω
DAC Output Resistance Match	$\Delta R_{OUT}/R_{OUT}$			0.5			5.0		%
V_{DD} Supply Rejection Ratio (Note 6)	PSRR--V_{DD}	DAC code = 55 (hex)		0.1	1.0		0.3	2.0	mV/V
V_{SS} Supply Rejection Ratio (Notes 4,6)	PSRR--V_{SS}	DAC code = 55 (hex)		0.1	1.0		0.8	5.0	mV/V
REFERENCE INPUT									
Voltage Range (Note 7)	REFH	REFH - REFL = 11V max	REFL		V_{DD}-3	REFL		V_{DD}-3	V
	REFL		V_{SS}		REFH	V_{SS}+1.5		REFH	
Input Resistance (Note 8)	REFH1/REFL1, or REFH2/REFL2	DAC code = 55 (hex)	2.0	3.4		2.0	3.4		kΩ
Input Capacitance	C_{REFH}	DAC loaded with 0s		40			40		pF
		DAC loaded with 1s		250			125		
AC Feedthrough		REFH=10kHz, 0-10V_{p-p} sinewave, all DACs at code 00 (hex)		-70			-70		dB

ELECTRICAL CHARACTERISTICS - MAX528 (continued)

(Unbuffered Mode: V_{DD} = +12V, V_{SS} = 0V; Full-Buffered Mode: V_{DD} = +12V, V_{SS} = -5V; GND = 0V, REFH = +5V, REFL = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	UNBUFFERED MODE (Note 1)			FULL-BUFFERED MODE (Note 2)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER REQUIREMENTS									
Positive Supply Range	V_{DD}		10.8		16.5	10.8		16.5	V
Negative Supply Range	V_{SS}		0		-5.5	-1.5		-5.5	V
Positve Supply Current	I_{DD}	DIN = CLK = 0V, $\overline{CS}$ = $\overline{SHDN}$ = 5V		0.3	1.0		5.5	9.0	mA
Negative Supply Current	I_{SS}	DIN = CLK = 0V, $\overline{CS}$ = $\overline{SHDN}$ = 5V		0.1	0.5		5.5	9.0	mA
I_{DD} at Shutdown	I_{DD}	$\overline{SHDN}$ = low			50			50	µA
I_{SS} at Shutdown	I_{SS}	$\overline{SHDN}$ = low			50			50	µA
DYNAMIC PERFORMANCE (Note 7)									
V_{OUT} Settling Time		To ±1/2LSB; C_{LOAD} = 20pF, from rising edge of $\overline{CS}$		1	3		0.6	2.0	µs
Digital Coupling		Serial input: 1MHz CLK, DIN alternating 1s and 0s (0.5MHz), C_L = 20pF, 0V to 5V input levels at CLK, DIN		20			20		mVp-p
Crosstalk		Full-scale output transition on all 7 other channels ($\overline{CS}$ high)		40			20		nV-s
		1LSB output transition on all 7 other channels ($\overline{CS}$ high)		2			10		

DIGITAL AND SWITCHING CHARACTERISTICS - MAX528

(V_{DD} = +12V, V_{SS} = -5V, REFH = +5V, REFL = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS DIN, CLK, $\overline{CS}$, $\overline{SHDN}$						
Input High Voltage	V_{INH}	DIN, CLK, $\overline{CS}$	2.4			V
Input Low Voltage	V_{INL}	DIN, CLK, $\overline{CS}$			0.8	V
Input High Voltage	V_{INH}	$\overline{SHDN}$	3.0			V
Input Low Voltage	V_{INL}	$\overline{SHDN}$			0.5	V
Input Hysteresis		DIN, CLK, $\overline{CS}$		0.1		V
Input Leakage Current		V_{IN} = 0V or V_{DD}			±1	µA
Input Capacitance (Note 7)					10	pF
DIGITAL OUTPUT, DOUT, open drain output, 1kΩ pull-up resistor to +5V						
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
Output High Leakage	I_{LKG}	V_{OUT} = 0V to V_{DD}			±10	µA
Output High Capacitance (Note 7)	C_{OUT}				15	pF

Octal 8-Bit Serial DACs with Output Buffer

DIGITAL AND SWITCHING CHARACTERISTICS - MAX528 (continued)

(V_{DD} = +12V, V_{SS} = -5V, REFH = +5V, REFL = 0V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
CLK Pulse Width High	t_{CH}		80			ns
CLK Pulse Width Low	t_{CL}		80			ns
DIN to CLK High Setup	t_{DS}		40			ns
DIN to CLK High Hold	t_{DH}		15			ns
$\overline{CS}$ Low to CLK High Setup	t_{CSS0}		50			ns
$\overline{CS}$ High to CLK High Setup	t_{CSS1}		50			ns
Delay, CLK Low to Low $\overline{CS}$	t_{CSH0}		0			ns
Delay, CLK High to High $\overline{CS}$	t_{CSH1}		50			ns
$\overline{CS}$ Pulse Width	t_{CSW}		130			ns
CLK High to DOUT Data Valid (Note 9)	t_{DO}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V	15 (Note 7)		130	ns
$\overline{CS}$ Low to DOUT Enable (Note 10)	t_{DV}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V			90	ns
$\overline{CS}$ High to DOUT Disable (Note 10)	t_{TR}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V			90	ns

Note 1: Unbuffered mode – buffers disabled. No output load.
Note 2: Full-buffered mode – buffers enabled; bipolar output mode; R_{LOAD} = 5kΩ.
Note 3: Relative accuracy in unbuffered mode guaranteed by relative accuracy test in full-buffered mode.
Note 4: Specification in Unbuffered Mode column guaranteed by design only. Not subject to test.
Note 5: Gain error with full-buffered mode enabled = no-load gain error - (DAC output resistance/R_{LOAD}). Example: -0.2% typ no-load error - (55Ω/5kΩ) = -1.3% typ error for 5kΩ load.
Note 6: PSRR tested over supply range specified under power requirements; PSRR = (V_{OUT1} - V_{OUT2})/($V_{SUPPLY1}$ - $V_{SUPPLY2}$).
Note 7: Guaranteed by design, not subject to test.
Note 8: Input resistance tested only under Unbuffered Mode conditions in Note1 above.
Note 9: V_{OH} = 2.4V, V_{OL} = 0.8V.
Note 10: t_{DV} and t_{TR} are defined as the time required for DOUT to change 0.5V.

ABSOLUTE MAXIMUM RATINGS - MAX529

V_{DD} to GND ..... -0.3V to +7V
V_{DD} to V_{SS} ..... -0.3V to +12V
V_{SS} to GND ..... -7V to +0.3V
REFH1 - REFL1, REFH2 - REFL2 ..... -0.3V to +12V
REFH1 - V_{SS}, REFH2 - V_{SS} ..... +12V
REFH1, REFH2 ..... REFL_ - 0.3V to V_{DD} + 0.3V
REFL1, REFL2 ..... V_{SS} - 0.3V to REFH_ + 0.3V
OUT(1-8) ..... V_{SS} - 0.3V to V_{DD} + 0.3V
OUT(1-8) to V_{SS} ..... +12V
OUT(1-8) Current ..... ±20mA
DIN, CLK, CS, DOUT ..... -0.3V to V_{DD} + 0.3V
SHDN ..... V_{SS} - 0.3V to V_{DD} + 0.3V

DOUT Current ..... ±20mA
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 11.11mW/°C above +70°C) 889mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
CERDIP (derate 11.11mW/°C above +70°C) 889mW
Operating Temperature Ranges:
MAX528C_ _ ..... 0°C to +70°C
MAX528E_ _ ..... -40°C to +85°C
MAX528MJP ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS - MAX529

(Unbuffered Mode: V_{DD} = +5V, V_{SS} = GND = 0V, REFH = +2.5V, REFL = 0V; Full-Buffered Mode: V_{DD} = +5V, V_{SS} = -5V, GND = 0V, REFH = +2.5V, REFL = -2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	UNBUFFERED MODE (Note 1)			FULL-BUFFERED MODE (Note 2)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC PERFORMANCE									
Resolution			8			8			Bits
Relative Accuracy (Note 3)	RLE			±0.3	±1.0		±0.3	±1.0	LSB
Differential Nonlinearity (Note 4)	DNL	Guaranteed monotonic		±0.3	±1.0		±0.3	±1.0	LSB
Full-Scale Error	FSE	R_{LOAD} = open			±1/2				LSB
Gain Error (Note 5)		R_{LOAD} = open					-0.2		%
		R_{LOAD} = 5kΩ				0.0	-1.3	-2.5	%
Unipolar Offset Error		DAC code = 00 (hex)			±5				mV
Bipolar Offset Error		DAC code = 80 (hex)						±60	mV
Offset Error Tempco				±5			±100		µV/°C
DAC Output Resistance	R_{OUT}		8.5k	13k	20k		55	100	Ω
DAC Output Resistance Match	$\Delta R_{OUT}/R_{OUT}$			0.5			5.0		%
V_{DD} Supply Rejection Ratio (Note 6)	PSRR--V_{DD}	DAC code = 55 (hex)		1.5	5		3	10	mV/V
V_{SS} Supply Rejection Ratio (Notes 4,6)	PSRR--V_{SS}	DAC code = 55 (hex)		0.3	2		1	5	mV/V
REFERENCE INPUT									
Voltage Range (Note 7)	REFH		REFL		V_{DD} - 2.25	REFL		V_{DD} - 2.25	V
	REFL		V_{SS}		REFH	V_{SS} + 1.5		REFH	
Input Resistance (Note 8)	REFH1/REFL1, or REFH2/REFL2	DAC code = 55 (hex)	2.0	3.4		2.0	3.4		kΩ
Input Capacitance	C_{REFH}	DAC loaded with 0s		40			40		pF
		DAC loaded with 1s		250			125		

Octal 8-Bit Serial DACs with Output Buffer

ELECTRICAL CHARACTERISTICS - MAX529 (continued)

(Unbuffered Mode: V_{DD} = +5V, V_{SS} = GND = ON, REFH = +2.5V, REFL = 0V; Full-Buffered Mode: V_{DD} = +5V, V_{SS} = -5V, GND = 0V, REFH = +2.5V, REFL = -2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	UNBUFFERED MODE (Note 1)			FULL-BUFFERED MODE (Note 2)			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC Feedthrough		REFH=10kHz, 0-2.5V_{p-p} sinewave, all DACs at code 00 (hex)		-70			-70		dB
POWER REQUIREMENTS									
Positive Supply Range	V_{DD}		4.75		5.25	4.75		5.25	V
Negative Supply Range	V_{SS}		0		-5.5	-4.5		-5.5	V
Positve Supply Current	I_{DD}	$\overline{DIN}$ = $\overline{CLK}$ = 0V, $\overline{CS}$ = $\overline{SHDN}$ = 5V		0.3	1.0		5.5	9.0	mA
Negative Supply Current	I_{SS}	$\overline{DIN}$ = $\overline{CLK}$ = 0V, $\overline{CS}$ = $\overline{SHDN}$ = 5V		0.1	0.5		5.5	9.0	mA
I_{DD} at Shutdown	I_{DD}	$\overline{SHDN}$ = low			50			50	µA
I_{SS} at Shutdown	I_{SS}	$\overline{SHDN}$ = low			50			50	µA
DYNAMIC PERFORMANCE (Note 7)									
V_{OUT} Settling Time		To ±1/2LSB; C_{LOAD} = 20pF, from rising edge of $\overline{CS}$		1	3		0.6	2.0	µs
Digital Coupling		Serial input: 1MHz CLK, DIN alternating 1s and 0s (0.5MHz), C_L = 20pF, 0V to 5V input levels at CLK, DIN		20			20		mVp-p
Crosstalk		Full-scale output transition on all 7 other channels ($\overline{CS}$ high)		40			20		nV-s
		1LSB output transition on all 7 other channels ($\overline{CS}$ high)		2			10		

DIGITAL AND SWITCHING CHARACTERISTICS - MAX529

(V_{DD} = +5V, V_{SS} = -5V, REFH = +2.5V, REFL = -2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS DIN, CLK, $\overline{CS}$		$\overline{SHDN}$				
Input High Voltage	V_{INH}	DIN, CLK, $\overline{CS}$	2.4			V
Input Low Voltage	V_{INL}	DIN, CLK, $\overline{CS}$			0.8	V
Input High Voltage	V_{INH}	$\overline{SHDN}$	3.0			V
Input Low Voltage	V_{INL}	$\overline{SHDN}$			0.5	V
Input Hysteresis		DIN, CLK, $\overline{CS}$		0.1		V
Input Leakage Current		V_{IN} = 0V or V_{DD}			±1	µA
Input Capacitance (Note 7)					10	pF
DIGITAL OUTPUT, DOUT, open drain output, 1.3kΩ pull-up resistor to +5V						
Output Low Voltage	V_{OL}	I_{SINK} = 3.5mA			0.4	V
Output High Leakage	I_{LKG}	V_{OUT} = 0V to V_{DD}			±10	µA
Output High Capacitance (Note 7)	C_{OUT}				15	pF

DIGITAL AND SWITCHING CHARACTERISTICS - MAX529 (continued)

(V_{DD} = +5V, V_{SS} = -5V, REFH = +2.5V, REFL = -2.5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

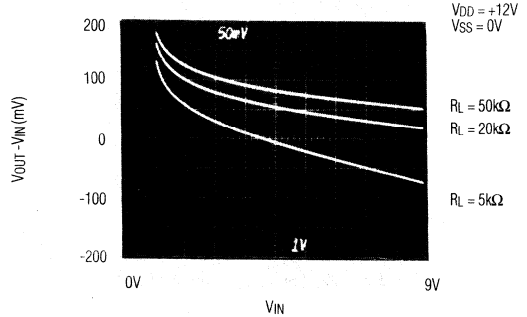
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SWITCHING CHARACTERISTICS						
CLK Pulse Width High	t_{CH}		125			ns
CLK Pulse Width Low	t_{CL}		125			ns
DIN to CLK High Setup	t_{DS}		50			ns
DIN to CLK High Hold	t_{DH}		20			ns
$\overline{CS}$ Low to CLK High Setup	t_{CSS0}		50			ns
$\overline{CS}$ High to CLK High Setup	t_{CSS1}		50			ns
Delay, CLK Low to Low $\overline{CS}$	t_{CSH0}		0			ns
Delay, CLK High to High $\overline{CS}$	t_{CSH1}		50			ns
$\overline{CS}$ Pulse Width	t_{CSW}		300			ns
CLK High to DOUT Data Valid (Note 9)	t_{DO}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V	20 (Note 7)		200	ns
$\overline{CS}$ Low to DOUT Enable (Note 10)	t_{DV}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V			120	ns
$\overline{CS}$ High to DOUT Disable (Note 10)	t_{TR}	C_{LOAD} = 20pF, Rpullup = 1kΩ to 5V			120	ns

Note 1: Unbuffered mode – buffers disabled. No output load.
Note 2: Full-buffered mode – buffers enabled; bipolar output mode; R_{LOAD} = 5kΩ.
Note 3: Relative accuracy in unbuffered mode guaranteed by relative accuracy test in full-buffered mode.
Note 4: Specification in Unbuffered Mode column guaranteed by design only. Not subject to test.
Note 5: Gain error with full-buffered mode enabled = no-load gain error - (DAC output resistance/R_{LOAD}). Example: -0.2% typ no-load error - (55Ω/5kΩ) = -1.3% typ error for 5kΩ load.
Note 6: PSRR tested over supply range specified under power requirements; PSRR = (V_{OUT1} - V_{OUT2})/($V_{SUPPLY1}$ - $V_{SUPPLY2}$).
Note 7: Guaranteed by design, not subject to test.
Note 8: Input resistance tested only under Unbuffered Mode conditions in Note1 above.
Note 9: V_{OH} = 2.4V, V_{OL} = 0.8V.
Note 10: t_{DV} and t_{TR} are defined as the time required for DOUT to change 0.5V.

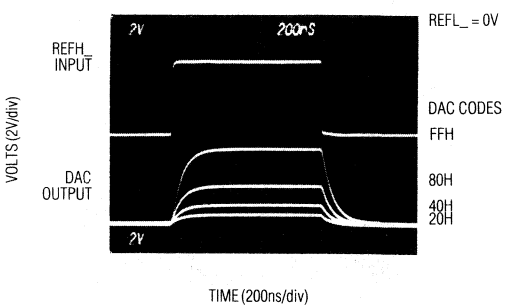
Typical Operating Characterisitics

MAX528

MAX528
HALF-BUFFERED GAIN AND LINEARITY ERROR vs. V_{IN} (OUTPUT VOLTAGE OF R-2R LADDER)



MAX528
FULL-BUFFERED STEP RESPONSE FOR VARIOUS CODES, NO LOAD

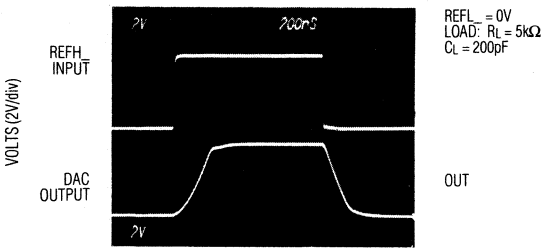


9

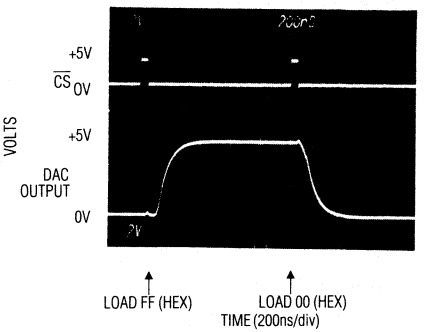
Octal 8-Bit Serial DACs with Output Buffer

Typical Operating Characterisitics (continued)

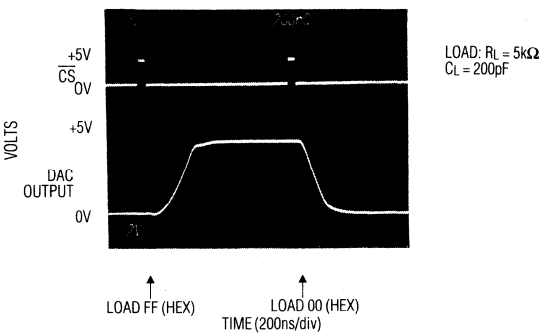
MAX528
FULL-BUFFERED STEP RESPONSE



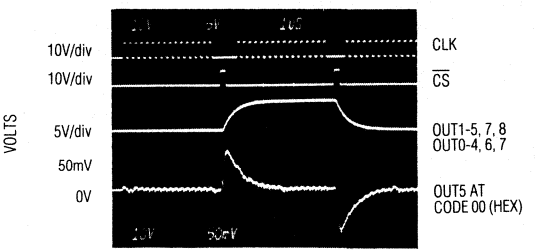
MAX528
FULL-BUFFERED SETTLING TIME
CODE CHANGE (00-FF-00), NO LOAD



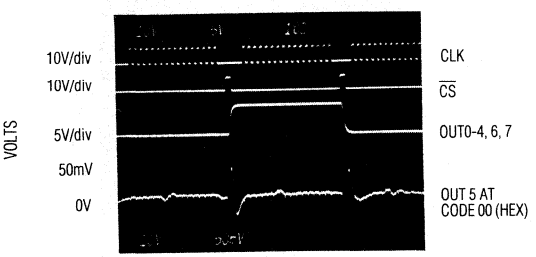
MAX528
FULL-BUFFERED SETTLING TIME
CODE CHANGE (00-FF-00)



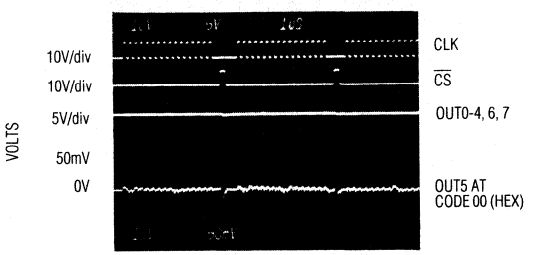
MAX528
UNBUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (00-FF-00), NO LOAD



MAX528
FULL-BUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (00-FF-00), NO LOAD



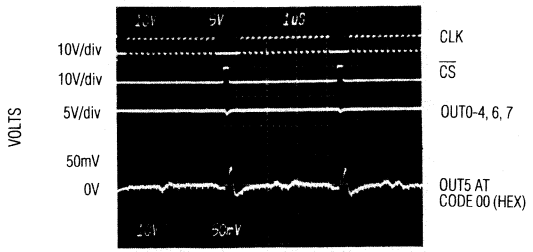
MAX528
UNBUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (7F-80-7F), NO LOAD



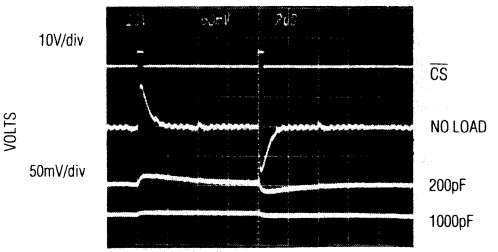
Octal 8-Bit Serial DACs with Output Buffer

Typical Operating Characteristics (continued)

MAX528
FULL-BUFFERED OFF-CHANNEL GLITCH CODE CHANGE (7F-80-7F), NO LOAD

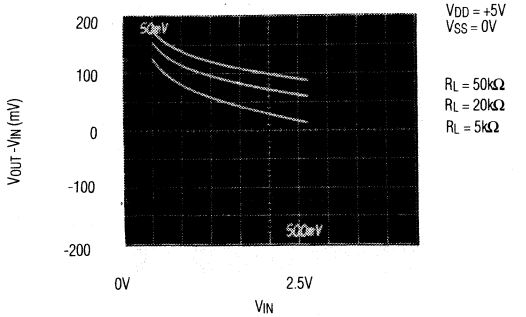


MAX528
UNBUFFERED OUTPUT GLITCH FILTERING

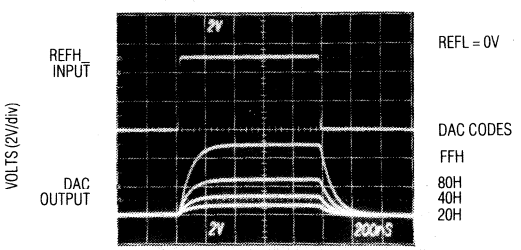


MAX529

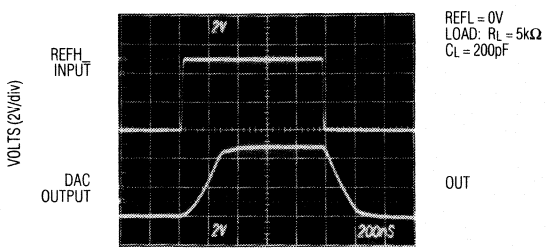
MAX529
HALF-BUFFERED GAIN AND LINEARITY ERROR vs. V_{IN} (OUTPUT VOLTAGE OF R-2R LADDER)



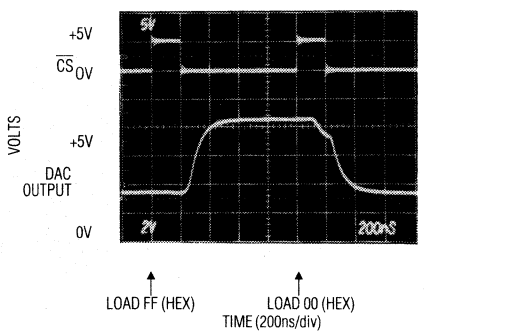
MAX529
FULL-BUFFERED STEP RESPONSE FOR VARIOUS CODES, NO LOAD



MAX529
FULL-BUFFERED STEP RESPONSE



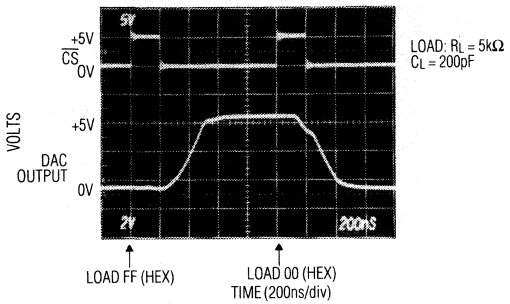
MAX529
FULL-BUFFERED SETTLING TIME CODE CHANGE (00-FF-00), NO LOAD



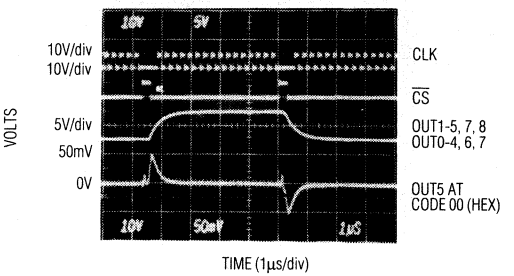
Octal 8-Bit Serial DACs with Output Buffer

Typical Operating Characteristics (continued)

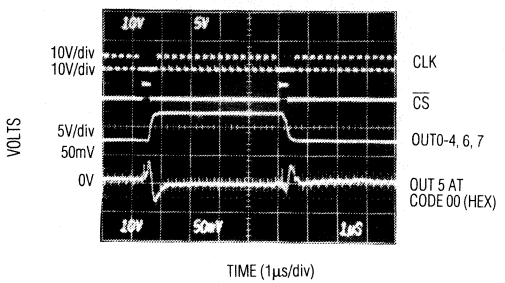
MAX529
FULL-BUFFERED SETTLING TIME
CODE CHANGE (00-FF-00)



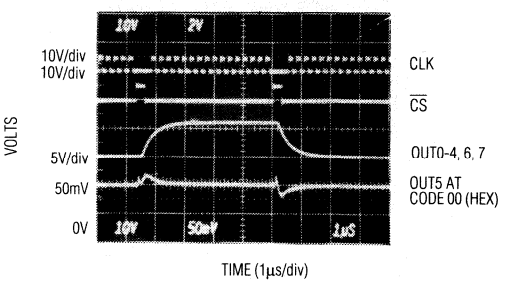
MAX529
UNBUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (00-FF-00), NO LOAD



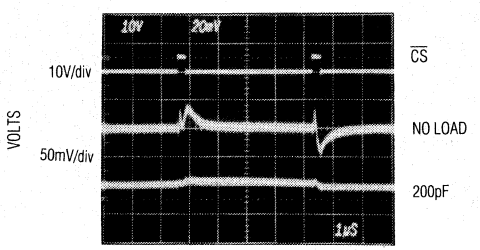
MAX529
FULL-BUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (00-FF-00), NO LOAD



MAX529
UNBUFFERED OFF-CHANNEL GLITCH
CODE CHANGE (00-FF-00), NO LOAD



MAX529
UNBUFFERED OUTPUT
GLITCH FILTERING



Pin Description

PIN DIP	PIN SO	NAME	FUNCTION
–	1, 12, 13, 24	N.C.	No Connect. These pins are not internally connected.
1	2	REFL1	Reference 1 Input Low. Must be more negative than REFH1 and more positive than V_{SS}.
2	3	REFH1	Reference 1 Input High. Must be more positive than REFL1 and more negative than V_{DD}.
3	4	OUT0	Output Voltage 0. The product of the digital code for channel 0 and (REFH1 - REFL1), referenced to REFL1.
4	5	OUT1	Output Voltage 1. The product of the digital code for channel 1 and (REFH1 - REFL1), referenced to REFL1.
5	6	OUT2	Output Voltage 2. The product of the digital code for channel 2 and (REFH1 - REFL1), referenced to REFL1.
6	7	OUT3	Output Voltage 3. The product of the digital code for channel 3 and (REFH1 - REFL1), referenced to REFL1.
7	8	V_{DD}	Positive Analog and Digital Supply.
8	9	DIN	Digital Input. CMOS and TTL compatible serial programming input.
9	10	CLK	Clock Input. CMOS and TTL compatible clock input.
10	11	DOUT	Digital Output. Open-drain N-channel FET output, requires external pull-up resistor; serial data output, shifted 16 bits from DIN.
11	14	GND	Digital Ground. Connect to 0V. (Analog signals are referenced to their respective REFL voltage, not GND).
12	15	$\overline{CS}$	$\overline{CHIP\ SELECT}$. Connect to logic low to program serially. Connect to logic high to latch data and turn off internal shift register. Rising edge of $\overline{CS}$ transfers new data into data registers and changes DAC output.
13	16	$\overline{SHDN}$	$\overline{SHUTDOWN}$. Connect to logic high for normal operation, to GND for shutdown mode.
14	17	V_{SS}	Negative Analog Supply. Connect to GND for single-supply operation. Connect to negative supply for bipolar DAC outputs.
15	18	OUT4	Output Voltage 4. The product of the digital code for channel 4 and (REFH2 - REFL2), referenced to REFL2.
16	19	OUT5	Output Voltage 5. The product of the digital code for channel 5 and (REFH2 - REFL2), referenced to REFL2.
17	20	OUT6	Output Voltage 6. The product of the digital code for channel 6 and (REFH2 - REFL2), referenced to REFL2.
18	21	OUT7	Output Voltage 7. The product of the digital code for channel 7 and (REFH2 - REFL2), referenced to REFL2.
19	22	REFH2	Reference 2 Input High. Must be more positive than REFL2 and more negative than V_{DD}.
20	23	REFL2	Reference 2 Input Low. Must be more negative than REFH2 and more positive than V_{SS}.

Octal 8-Bit Serial DACs with Output Buffer

Detailed Description

Circuit Operation

The MAX528/MAX529 contain 8 latched digital-to-analog converters (DACs), 8 buffer amplifiers, 2 reference inputs, and serial control logic. Buffer amplifiers may also be bypassed by internal switches, allowing three output modes: unbuffered, full-buffered, and half-buffered.

Any or all of the 8 voltage outputs can be programmed with 16 serial data bits.

DAC Output Range

The MAX528/MAX529 provide 8 voltage outputs (OUT0-OUT7) from 2 reference inputs. Each reference voltage has 2 input pins, REFH and REFL. The OUT0-OUT3 output voltages are derived from REFH1 and REFL1 while OUT4-OUT7 are derived from REFH2 and REFL2. For each reference, REFH must be more positive than REFL. A DAC output voltage is the product of its programmed 8-bit code and its reference input voltage. For example, the output voltage of OUT5 is:

OUT5 = (REFH2 - REFL2) (nn/256 + REFL2),

where nn = 8-bit code for OUT5, with a range of 0-255 (00 to FF hex.)

The reference inputs are independent of one another. REFH can range within 3V of V_{DD}. REFL can be as low as V_{SS} in unbuffered and half-buffered modes, but must be at least 1.5V above V_{SS} in full-buffered mode. For the MAX528, V_{SS} can be any negative voltage from -15V to 0V, provided that V_{DD}-V_{SS} is no more than 20V. For the MAX529, V_{SS} can be any negative voltage from 0V to -5V. In all modes, REFH must be no more than 12V greater than REFL.

Although the MAX528/MAX529 have a digital ground (GND) pin, they contain no internal analog ground. The upper and lower limits of any DAC output are the voltages to which REFH and REFL are connected.

Shutdown

To conserve power, the MAX528/MAX529 can be shut down by pulling $\overline{SHDN}$ low. V_{CC} and V_{SS} supply currents drop to less than 50µA, but reference current will still be drawn. Reference current is code dependent and can be reduced to nearly 0 (leakage only) by writing 0s to all DACs.

Note: To ensure that register data is retained during shutdown, $\overline{CS}$ must be high when entering or leaving shutdown mode.

Buffer Output Modes

DAC outputs can be programmed for one of three buffer modes: unbuffered, full-buffered, and half-buffered. Buffers must be activated in pairs, and full- or half-buffered mode must be selected in banks of four as shown in Table 1 (see *Digital Interface* section).

Table 1. Buffer Output-Mode Selection Codes (Address 00 hex, D6 = X, D7 = 1)

Mode	OUT0, 1	OUT2, 3	OUT4, 5	OUT5, 6
Unbuffered (D0, D3=X)	D5 = 0	D4 = 0	D2 = 0	D1 = 0
Full-Buffered	D5 = 1	D4 = 1	D2 = 1	D1 = 1
	D3 = 1		D0 = 1	
Half-Buffered	D5 = 1	D4 = 1	D2 = 1	D1 = 1
	D3 = 0		D0 = 0	

Unbuffered Mode

Unbuffered mode connects the internal 20kΩ R-2R DAC network (Figure 1) directly to OUT. Buffer circuitry is disabled, reducing power consumption as well as offset errors contributed by the internal buffer amplifier (see *Electrical Characteristics*). Driving high-resistance loads (1MΩ and up) improves accuracy. Output range in unbuffered mode is from the negative supply rail (V_{SS}) to V_{DD} - 3V for the MAX528 (V_{SS} to V_{DD} -2.25V for MAX529).

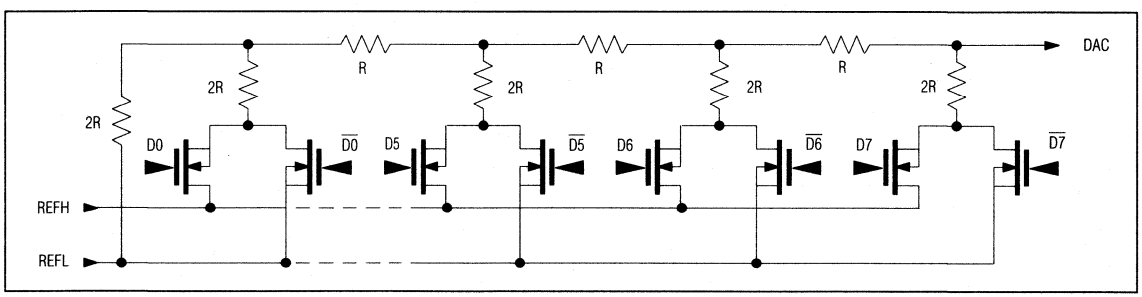


Figure 1. R-2R Inverted Ladder DAC Structure

Unbuffered mode also operates effectively with lower resistance loads, but output loading may generate gain (full-scale) error. This will not affect linearity because DAC output resistance (between 8.5kΩ and 20kΩ) does not change with code. The magnitude of the expected gain error is the ratio of the DAC output impedance (typically 13kΩ) to the DC load resistance at the output.

Another advantage of unbuffered operation is that output filtering uses small capacitors and no resistors. The Unbuffered Output Glitch Filtering photos in the *Typical Operating Characteristics* show the feedthrough effect of changing all channels but one from full-scale to zero. On the rising edge of $\overline{CS}$ (top trace), energy is coupled into the unchanged channel (2nd trace, unfiltered), producing a 70mV, 1µs pulse for the MAX528, and a 40mV, 5µs pulse for the MAX529. The third and fourth traces of the MAX528 photo show how this pulse is suppressed using 200pF and 1000pF load capacitors with the MAX528. The third trace of the MAX529 photo shows this pulse suppression using a 200pF load capacitor with the MAX529.

Full-Buffered Mode

Full-buffered mode (Figure 2) activates both sections of the buffer amplifer, lowering the output impedance to typically 55Ω and allowing +5mA/-2mA output currents to be supplied. The buffer amplifier output swing is from V_{SS} + 1.5V to V_{DD} - 3V (V_{SS} = +1.5V to V_{DD} - 2.25V for MAX529). The key advantage of this mode is that changes in load current cause minimal output change.

Half-Buffered Mode

Half-buffered mode (Figure 3) activates only the top half of the output stage, and therefore sources current only. Its advantage is that it maintains output swing to V_{SS} while providing a buffered output. Output swing is from V_{SS} to V_{DD} - 3V (V_{SS} = +1.5V to V_{DD} - 2.25V for MAX529). Current consumption is reduced to typically 1.7mA (compared to 5.5mA for full-buffered) if all buffers use half-buffered mode.

Using an AC Reference with the MAX528

In applications where the reference has AC signal components, the MAX528 has multiplying capability within the REFH and REFL specifications. Figure 4 shows a technique for attenuating an AC signal by superimposing it on a DC voltage prior to REFH. As the DAC code changes, the AC output changes, as does the DC level. The output DC level is removed by capacitively coupling to the next stage. Note that the peak negative voltage at REFH must not swing below REFL.

Digital Interface

Serial Interface

Serial data at DIN is clocked in on the rising edge of CLK, while $\overline{CS}$ is low and $\overline{SHDN}$ is high (Figure 5). Data can be loaded at clock rates up to 6.25MHz (4MHz for MAX529). Logic inputs are CMOS and TTL compatible. The serial output DOUT is an open-drain N-channel FET that sinks up to 5mA and requires an external pull-up resistor (typically 4.7kΩ) to V_{DD}. Output data changes on the rising edge of CLK.

Any number of MAX528s or MAX529s can be daisy-chained by connecting the DOUT pin of one device (with pullup resistor) to the $\overline{DIN}$ pin of the following device in the chain. CLK and $\overline{CS}$ are bussed together. Clock period and t_{CSS0} ($\overline{CS}$ low to CLK high) must be increased to account for data delays between devices.

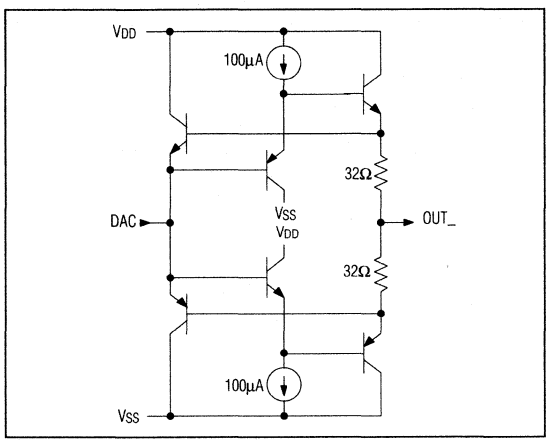


Figure 2. Simplifed Full-Buffered Output Circuit

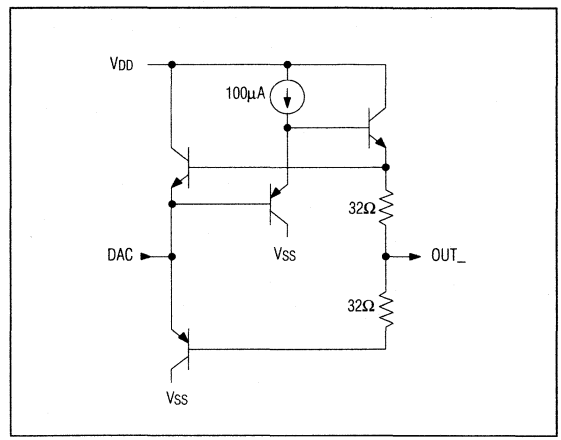


Figure 3. Simplifed Half-Buffered Output Circuit

Octal 8-Bit Serial DACs with Output Buffer

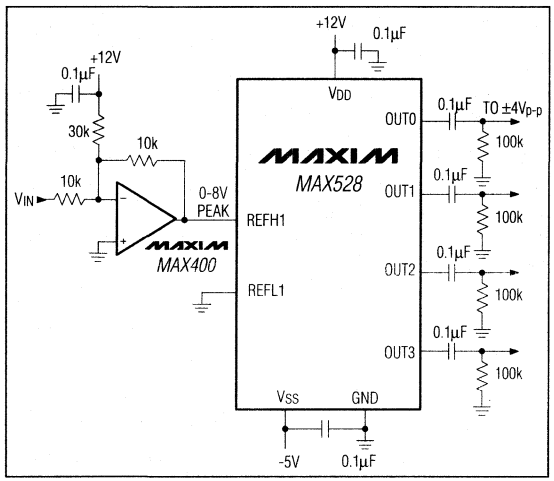


Figure 4. Using an AC Reference with the MAX528

If capacitive loading at the DOUT-to-DIN junction between two devices is 50pF or less, then the required t_{CSS0} becomes the sum of t_{DV} (enable) and t_{DS} (setup times), which is 130ns (90ns + 40ns) for MAX528 and t_{CSS0} 170ns (120ns + 50ns) for the MAX529.

Maximum clock rate is influenced by pullup resistor size as well as capacitive loading: $f_{CLK}max = 1/(t_{DO} + t_{DS} + 0.65t_{RC})$, where t_{DO} = 130ns, t_{DS} = 40ns, and t_{RC} is the pullup resistor and capacitive load product. So for a 1kΩ pullup and 50pF load, the MAX528 $f_{CLK}max$ is 4.7MHz; for a 4.7kΩ pullup with 50pF load, $f_{CLK}max$ drops to 2.8MHz. A similar calculation can be made for the MAX529, using t_{DO} = 200ns, and t_{DS} = 50ns.

DAC Programming

The MAX528/MAX529 are programmed by 16 data bits in two 8-bit bytes, the address pointer bits (A7-A0) followed by the data byte (D7-D0). These bits enter a shift register serially through DIN: A7 first, and D0 last. The data exits DOUT 16 clock cycles later in the same order.

Data at DIN is shifted into the first register (while all 16 register bits shift forward one stage) on a rising CLK edge, while holding $\overline{CS}$ low and $\overline{SHDN}$ high. This must occur 16 times to load all data bits into the shift registers. On the rising edge of $\overline{CS}$, data in the 16 shift registers is transferred as addressed and CLK is disabled.

There are three types of instructions: NOP, SET DAC, and set buffer modes.

No Operation

No Operation (NOP) is implemented when all 8 address pointer bits (A7-A0) and data bit D7 are logic 0. Data in D6-D0 is ignored. When this instruction is clocked in, no registers are updated and the outputs remain unchanged. NOP is a place-saver when multiple MAX528/MAX529s are daisy-chained.

SET DAC

SET DAC is implemented when at least one of the 8 address pointer bits (A7-A0) is logic 1. SET DAC updates the digital code of any or all DAC registers (and their corresponding DAC outputs) to a single new value. The new value is contained in the data byte (D7-D0). Each address pointer bit (A7-A0) selects a DAC output. Any combination of outputs can be updated simultaneously with one 16-bit instruction. Remember that address 0000 0000 is reserved for NOP and set buffer modes.

SET DAC does not change the buffer modes.

Set Buffer Modes

Set buffer modes is implemented when all 8 address pointer bits (A7-A0) are logic 0 and data bit D7 is 1. (see Table 1). Data in D6 is ignored. When this instruction is issued, data bits D5-D0 are transferred to the mode registers only; the DAC registers are unchanged.

Enabling and disabling the 8 buffers is done in four pairs by data bits D1, D2, D4, and D5. D1 controls buffers 6 and 7, D2 controls buffers 4 and 5, D4 controls buffers 2 and 3, and D5 controls buffers 0 and 1. A logic 1 enables a buffer pair (full-buffered or half-buffered mode); a logic 0 disables a buffer pair (unbuffered mode).

Full-buffered and half-buffered modes are set by two data bits, D0 and D3. D0 controls OUT4 through OUT7; D3 controls OUT0 through OUT3. A logic 1 enables full-buffered mode; a logic 0 enables half-buffered mode. These data bits apply only when buffer output pairs are enabled by a 1 in D1, D2, D4, or D5.

The set buffer modes instruction does not update the DAC registers.

Programming Data

Table 2. Programming NOP

Data Direction: First >----------> Last

Function	Address Pointer Bits								Data Byte							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
NOP	0	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X

X = Don't Care

Table 3. Programming SET DAC Outputs

Function	Address Pointer Bits								Data Byte							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
SET DAC Outputs	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

DAC code, 0000 0000 to 1111 1111 (00 Hex through FF Hex) D7 = MSB; D0 = LSB.
AX = set DAC register X to digital value D7-D0. A7 = OUT7...A0 = OUT0. Logic 1 sets the DAC register to new DAC code in D7-D0; logic 0 ignores D7-D0 code and keeps previous code. At least one of theses 8 bits must be 1 (A7-A0 = 01 hex to FF hex).

Table 4. Programming Set Buffer Modes

Function	Address Pointer Bits								Data Byte							
	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Set Buffer Modes	0	0	0	0	0	0	0	0	1	X	0&1	2&3	0/3	4&5	6&7	4/7

X = Don't Care (D6)
0&1 (D5) = buffer enable for OUT0 and OUT1. Logic 1 = buffers enabled, 0 = buffers disabled (unbuffered mode). Similar remarks apply to 2&3 (D4), 4&5 (D2), and 6&7 (D1).
0/3 (D3) = buffer modes for OUT0-3. Logic 1 = full-buffered mode, 0 = half-buffered mode. D3 has no meaning when D4 and D5 are both 0.
4/7 (D0) = buffer modes for OUT4-7. Logic 1 = full-buffered mode, 0 = half-buffered mode. D0 has no meaning when D1 and D2 are both 0.

Programming Examples

Example 1: Set OUT0, OUT2, OUT7 to binary value 0100 1110 (4E hex). Leave OUT1, OUT3, OUT4, OUT5, and OUT6 unchanged, and leave buffer states unchanged.

Data Direction: First >----------> Last

	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Example 1	1	0	0	0	0	1	0	1	0	1	0	0	1	1	1	0

Example 2: Set all DACs except OUT6 to binary value 0000 0000 (00 hex). Leave OUT6 unchanged, and leave buffer states unchanged.

	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Example 2	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Example 3: Disable all buffers (unbuffered mode). Leave DAC data unchanged.

	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Example 3	0	0	0	0	0	0	0	0	1	X	0	0	X	0	0	X

X = Don't Care

Example 4: (1) Enable OUT0 and OUT1 buffers in full-buffered mode; put OUT2 and OUT3 in unbuffered mode. (2) Enable OUT6 and OUT7 buffers in half-buffered mode; put OUT4 and OUT5 in unbuffered mode. Leave DAC data unchanged.

	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Example 4	0	0	0	0	0	0	0	0	1	X	1	0	1	0	1	0

X = Don't Care

Octal 8-Bit Serial DACs with Output Buffer

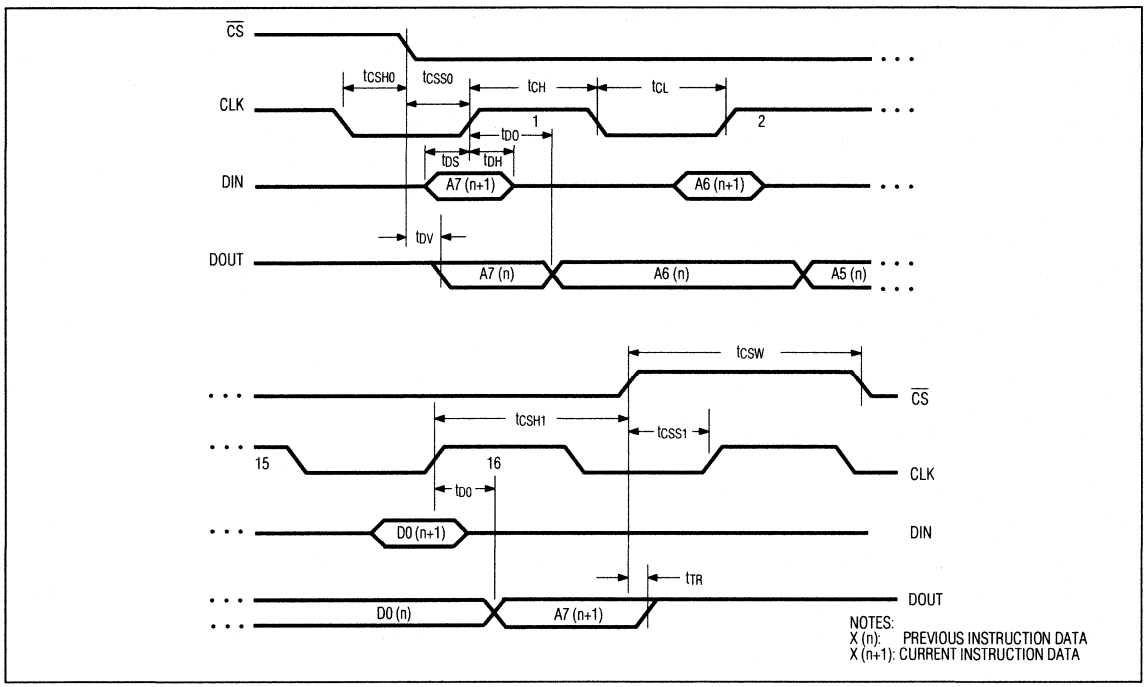


Figure 5. Timing Diagram

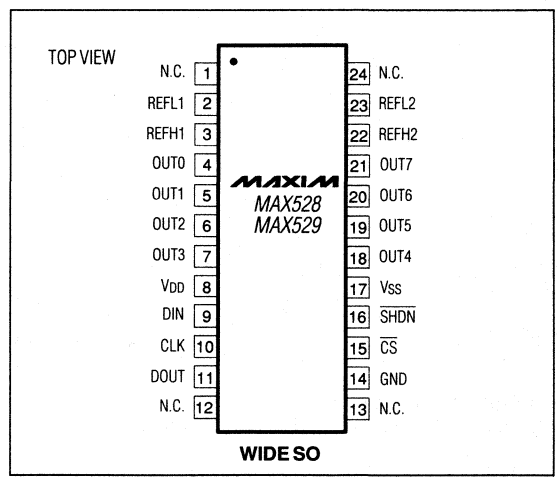
Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
MAX529CPP	0°C to +70°C	20 Plastic DIP
MAX529CWG	0°C to +70°C	24 Wide SO
MAX529C/D	0°C to +70°C	Dice*
MAX529EPP	-40°C to +85°C	20 Plastic DIP
MAX529EWG	-40°C to +85°C	24 Wide SO
MAX529MJP	-55°C to +125°C	20 CERDIP**

* *Contact factory for dice specifications.*

** *Contact factory for availability and processing to MIL-STD-883.*

Pin Configurations (continued)



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

Complete, Dual, 12-Bit, Serial-Input, Voltage-Output MDAC

General Description

The MAX532 is a complete, dual, serial-input, 12-bit multiplying digital-to-analog converter (MDAC) with output amplifiers. No external user trims are required to achieve full specified performance. The MAX532's 3-wire/4-wire serial interface minimizes the number of package pins, so it uses less board space than parallel-interface parts. A digital output pin provides for cascading serial devices.

When used with microprocessors (µPs) with a serial port, the MAX532 minimizes digital-noise feedthrough from its logic input pins to its analog outputs. To further reduce noise, the µP serial port can be used as a dedicated analog bus and kept inactive while the MAX532 is in use. Serial interfacing also simplifies opto-coupler-isolated or transformer-isolated applications.

The MAX532 is specified with ±12V to ±15V power supplies. All logic inputs are TTL and CMOS compatible. It comes in space-saving 16-pin DIP and wide SO packages.

Features

- ♦ **Two 12-Bit MDACs with Output Amplifiers**
- ♦ **Fast 3-Wire/4-Wire Interface**
- ♦ **4µs Typ Settling Time to ±1/2 LSB**
- ♦ **Low Differential Nonlinearity: ±1LSB Max**
- ♦ **Low Integral Nonlinearity: ±1/2LSB Max**
- ♦ **Gain Accuracy to ±2LSB**
- ♦ **Low Gain Tempco: 2ppm/°C Typ**
- ♦ **Operates from ±12V to ±15V Supplies**
- ♦ **TTL/CMOS Compatible**
- ♦ **Available in 16-Pin DIP and Wide SO Packages**

Applications

Automatic Test Equipment

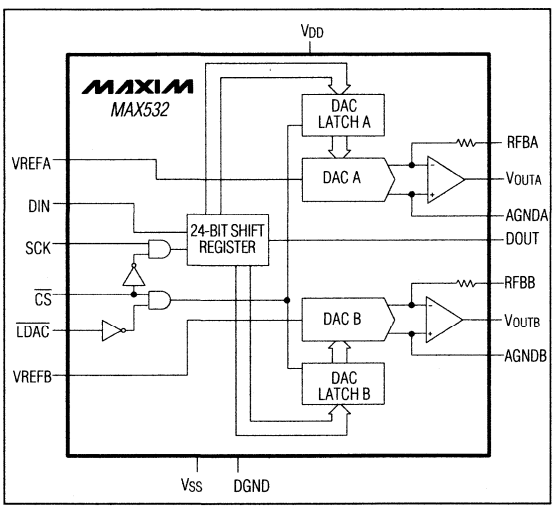
Arbitrary Waveform Generators

Programmable Power Supplies

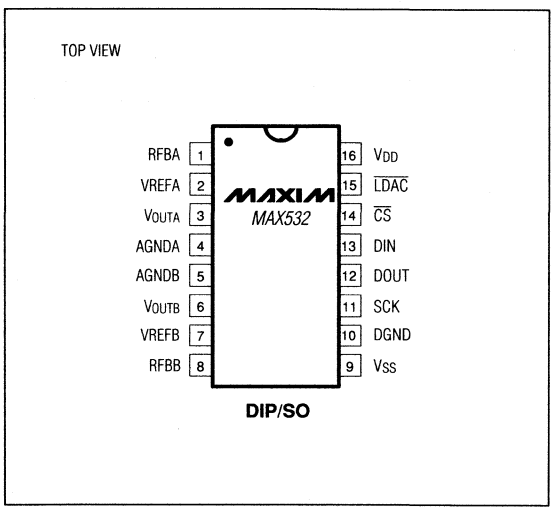
Motion Control Systems

Servo Controls

Functional Diagram



Pin Configuration



9

Display Drivers/Timers/Counters

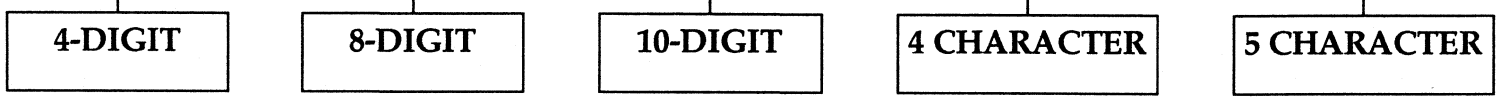
10

* Advance Information – first page of data sheet in preparation.

Part Number	Output	Display Format	Input Format	Input Formula	Number of Annunciators	LCD or LED	Features	Price† 1000-up ($)
ICM7211	4 digit	Hexadecimal or code B	Multiplexed or microprocessor interface	4-bits data	No independent annunciators	LCD	Muxed version, 4 digit strobes; Interfaced version, 2 digit address	2.42
ICM7212	4 digit	Hexadecimal or code B	Multiplexed or microprocessor interface	4-bits data	No independent annunciators	LED	Muxed version, 4 digit strobes; Interfaced version, 2 digit address	2.05
MAX7219	8 digit	7 segment or no decode	Serial entry	8-bits data 8-bits address	No independent annunciators	LED	True 3-wire serial interface	3.99
MAX7220	8 digit	7 segment or no decode	Parallel entry	8-bits data	No independent annunciators	LED	20ns access time	††
MAX7231	8 digit	Hexadecimal or code B	Parallel entry	4-bits data 2-bits annunciator 3-bit address	16	LCD	"A" & "B" versions, both annunciators on COM3; "C" version, annunciators on COM1 & COM3	4.50
ICM7218/ ICM7228	8 digit	Hexadecimal or no decode	Parallel entry	6-bits data	No independent annunciators	LED	"A" version drives common anode display; "B" version drives common cathode display	4.33
MAX7232	10 digit	Hexadecimal or code B	Serial entry	4-bits data 2-bits annunciator 4-bit address	20	LCD	"A" & "B" versions, both annunciators on COM3; "C" version, annunciators on COM1 & COM3	4.37
MAX7233	4 char.	64 character ASCII	Parallel entry	6-bits ASCII data 2-bit address	No independent annunciators	LCD	"A" version, half-width numbers; "B" version, full-width numbers	4.06
MAX7234	5 char.	64 character ASCII	Serial entry	6-bits ASCII data 3-bit address	No independent annunciators	LCD	"A" version, half-width numbers; "B" version, full-width numbers	4.51

† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.
†† Future product – contact factory for pricing and availability.

DISPLAY DRIVERS



4-DIGIT	8-DIGIT	10-DIGIT	4 CHARACTER	5 CHARACTER
ICM7211	★ MAX7219	MAX7232	MAX7233	MAX7234
ICM7212	★ MAX7220			
	MAX7231			
	ICM7218			
	ICM7228			

ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

25MHz High-Speed Function Generator

General Description

The MAX038 is a high-speed function generator, capable of producing accurate, high-frequency triangle, sawtooth, sine, square and pulse waveforms with a minimum of external components. The frequency of operation is controlled by an internal 2.5V bandgap voltage reference and the external resistor and capacitor combine to cover a frequency range of 0.01Hz to 25MHz. The duty cycle can be varied over a wide range by applying a control signal (±2.5V) to the DADJ pin, enabling the generation of sawtooth waveforms and pulse width modulation. Frequency modualtion and frequency sweeping can be accomplished over a wide range by applying a control voltage (±2.5V) to the FADJ pin. A key advantage is that the duty cycle and frequency controls are non-interactive which simplifies its use.

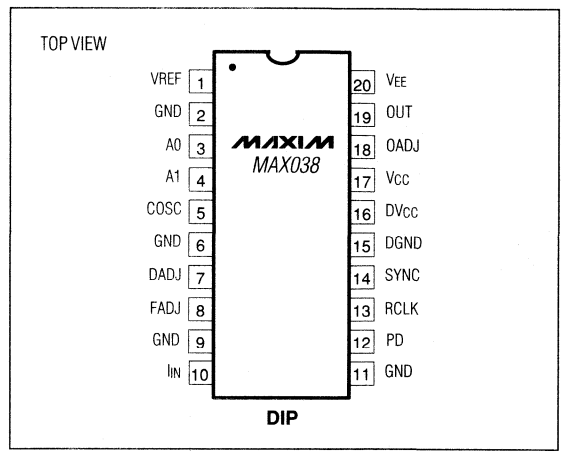
Sine, square, or triangle waveforms can be selected at the output by setting the appropriate code at the TTL compatible select pins A0 & A1. The output signal for all waveforms is a $2V_{p-p}$ signal which is symmetric about ground. The low-impedance output can drive up to ±20mA. The TTL compatible SYNC output at the internal oscillator frequency maintains 50% duty cycle regardless of the duty cycle of the other waveforms. Other devices in the system can be synchronized to the local oscillator via the SYNC output.

Conversely the internal oscillator can be synchronized to an external TTL level clock signal source connected with the RCLK pin and the addition of an external lowpass filter to the PD output.

Features

- **Operating Frequency Range 0.1Hz to 25MHz**
- **Triangle, Sawtooth, Sine, Square, and Pulse Waveforms**
- **Non-Interacting Frequency and Duty Cycle Adjustments**
- **Frequency Sweep Range (0.1 x f_O) to (2 x f_O)**
- **Variable Duty Cycle 10% to 90%**
- **Low-Impedance Output Buffer**
- **Low-Distortion Sine Wave < 1%**
- **Low Temperature Drift < 200ppm**

Pin Configuration



MAXIM

Voltage References

* Advance Information – first page of data sheet in preparation.

Part Number	Voltage	Temp. Drift (ppm/°C max)	Initial Accuracy T_A = +25°C (%F.S. max)	Quiescent Current (mA max)	Noise 0.1Hz-10Hz (µVp-p) max (typ)	Package Options[1]	Temp. Range[2]	Features	Price† 1000-up ($)
ICL8069	1.2	10 to 100	2	0.05	5 (10Hz - 10kHz)	TO-52, TO-92, SO*	C, M, E	Micropower two-terminal reference	0.98
MAX872	2.5	40	0.2	0.010	(60)	DIP, SO	C, E	V_{CC} = V_{OUT} +,2V	2.14
MX580	2.5	10 to 85	0.4 to 3	1.5	(60)	TO-52, SO**	C, M	Low-drift bandgap reference	2.71
MX584	2.5	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C, M	Low-drift, programmable reference	3.09
MAX874	4.096	40	0.2	0.010	(60)	DIP, SO	C, E	V_{CC} = V_{OUT} +,2V	2.14
MAX675	5.0	12 to 20	0.15	1.4	15	DIP, SO, TO-99, CERDIP	C, E, M	Low-drift, low-noise bandgap reference	3.40
MX584	5.0	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C, M	Low-drift, programmable reference	3.09
REF02	5.0	8.5 to 250	0.3 to 2	1.4	15	DIP, SO, TO-99, CERDIP	C, M	Low-drift bandgap reference	2.09
MX584	7.5	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C, M	Low-drift, programmable reference	3.09
MAX670	10.0	3 to 10	0.025	14	50	SB Ceramic	E, M	Kelvin connected, ultra-low drift reference	32.78
MAX671	10.0	1 to 10	0.01	14	50	SB Ceramic	C, E, M	Kelvin connected, ultra-low drift reference	31.84
MAX674	10.0	12 to 20	0.15	1.4	30	DIP, SO, TO-99, CERDIP	C, E, M	Low-drift, low-noise bandgap reference	3.40
MX581	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-39, SO***	C, M	Low-drift bandgap reference	3.07
MX584	10.0	5 to 30	0.05 to 0.3	1	(50)	TO-99, DIP, SO, CERDIP	C, M	Low-drift, programmable reference	3.09
MX2700	10.0	3 to 10	0.025 to 0.05	14	(50)	SB Ceramic	I, M	Ultra-low drift voltage reference	17.60
MX2710	10.0	1 to 5	0.01	14	(30)	SB Seramic	C	Ultra-low drift voltage reference	22.20
REF01	10.0	8.5 to 65	0.3 to 1	1.4	30	DIP, SO, TO-99, CERDIP	C, M	Low-drift bandgap reference	2.21
MX2701	-10.0	3 to 10	0.025 to 0.05	14	(50)	SB Ceramic	I, M	Ultra-low drift voltage reference	21.56

* The ICL8069 is available in a 2-pin TO-52 and TO-92 package, or an 8-pin SO package.
** The MX580 is avilable in a 3-pin TO-52 and 8-pin SO package.
*** The MX581 is available in a 3-pin TO-39 and 8-pin SO package.
[1] Package Options: DIP = Dual-In-Line Package, PLCC = Plastic Leaded Chip Carrier (quad pack), FP = Flat Pack
[2] Temp Ranges: C = 0°C to +70°C, I = -25°C to +85°C, E = -40°C to +85°C, M = -55°C to +125°C
† Prices provided are for design guidance and are FOB USA. International prices will differ due to local duties, taxes, and exchange rates.

REFERENCES

VOLTAGE OUT

1.2 VOLTS

ICL8069
(10-100ppm/°C)

2.5 VOLTS

★ **MAX872**
(IQ = 10µA, 40ppm/°C)

MX580
(10-85ppm/°C)

MX584
(5-30ppm/°C)

4.0 VOLTS

★ **MAX874**
(IQ = 10µA, 40ppm/°C)

5.0 VOLTS

MAX675
(12-20ppm/°C)

MX584
(5-30ppm/°C)

REF02
(8.5-250ppm/°C)

7.5 VOLTS

MX584
(5-30ppm/°C)

10.0 VOLTS

MAX670
(3-10ppm/°C)

MAX671
(1-10ppm/°C)

MAX674
(12-20ppm/°C)

MX2700
(3-10ppm/°C)

MX2710
(1-5ppm/°C)

MX581
(5-30ppm/°C)

MX584
(5-30ppm/°C)

REF01
(8.5-65ppm/°C)

-10.0 VOLTS

MX2701
(3-10ppm/°C)

★ New product since the publication of the 1990 Short Form Product Guide.

19-0005; Rev 0; 6/92

MAXIM

10μA, Low-Dropout, 2.5V Precision Voltage Reference

General Description

The MAX872 precision micropower voltage reference consumes a maximum of only 10μA and operates from supply voltages up to 20V. The MAX872 sources 250μA with $V_{IN} \geq V_{OUT} + 0.2V$, making it ideal for use with +3V supplies. The MAX872 is trimmed to 2.5V ±0.2%, and features a maximum 40ppm/°C drift.

Features

- ♦ **10μA Max Supply Current**
- ♦ **+2.7V to +20V Operating Voltage Range**
- ♦ **40ppm/°C Max Drift**
- ♦ **±0.2% Output Tolerance**
- ♦ **80μV/V Line Regulation**
- ♦ **600μV/mA Max Load Regulation Over Temp**
- ♦ **±250μA Load Current**

Applications

Handheld Instruments

Battery-Operated Equipment

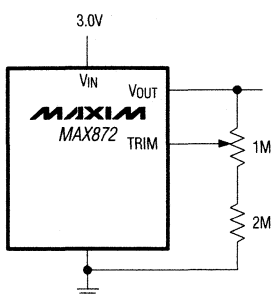
Power-Supplies

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX872CPA	0°C to +70°C	8 Plastic DIP
MAX872CSA	0°C to +70°C	8 SO
MAX872C/D	0°C to +70°C	Dice*
MAX872EPA	-40°C to +85°C	8 Plastic DIP
MAX872ESA	-40°C to +85°C	8 SO

** Dice are specified at T_A +25°C, DC parameters only.*

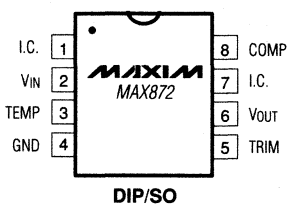
Typical Operating Circuit



REFERENCE WITH TRIMMED OUTPUT

Pin Configuration

TOP VIEW



DIP/SO

11

10µA, Low-Dropout, 2.5V Precision Voltage Reference

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 24V
Output Short-Circuit Duration ..... Indefinite to Either Supply
C_{COMP} Input ..... -0.3V to V_{OUT}
TRIM Input ..... -0.3V to (V_{IN} + 0.3V)
TEMP Output ..... -0.3V to (V_{IN} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW

Operating Temperature Ranges:
MAX872C_ ..... 0°C to +70°C
MAX872E_ ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature Range (Tj) ..... -65°C to +160°C
Lead Temperature (soldering, 10 sec) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 2.7V, I_L = 0mA, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}	I_L = 0mA	2.495	2.500	2.505	V
Output Voltage Noise	e_n	0.1Hz to 10Hz		60		μV_{p-p}
Line Regulation	V_{OUT}/V_{IN}	V_{IN} = 4.5V to 20V		4	12	µV/V
		V_{IN} = 2.7V to 5.5V		80	250	
Load Regulation	V_{OUT}/I_{OUT}	Sourcing 0mA to 0.25mA		0.2	0.5	mV/mA
		Sinking 0mA to -0.25mA		1.5	4.0	
Quiescent Supply Current	I_Q			6.5	10.0	µA
Change in Supply Current vs. V_{IN}	I_Q/V_{IN}	V_{IN} = 2.7V to 20V		0.35	0.55	µA/V
Short-Circuit Output Current	I_{SC}	V_{OUT} short to GND		2	6	mA
		V_{OUT} short to V_{IN}		3	9	
TEMP Voltage	V_{TEMP}			690		mV
V_{OUT} Adjustment Range	V_{TRIM}	$V_{IN} \geq V_{OUT}$ + 0.2V	+75/-20	+100/-25		mV
Long-Term Drift	$V_{OUT(T)}$			TBD		ppm/month

ELECTRICAL CHARACTERISTICS

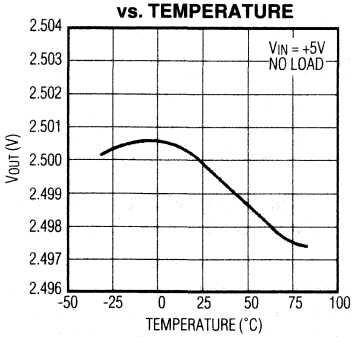
(V_{IN} = 2.7V, I_L = 0mA, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V_{OUT}	I_L = 0mA	MAX872C	2.4905		2.5095	V
			MAX872E	2.4880		2.5120	
Temperature Coefficient	TCV_{OUT}				20	40	ppm/°C
Line Regulation	V_{OUT}/V_{IN}	V_{IN} = 4.5V to 20V				20	µV/V
		V_{IN} = 2.7V to 5.5V				300	
Load Regulation	V_{OUT}/I_{OUT}	Sourcing 0mA to 0.25mA				0.6	mV/mA
		Sinking 0mA to -0.25mA	MAX872C			6.0	
			MAX872E			8.0	
Quiescent Supply Current	I_Q	No load				15	µA
Change in Supply Current vs. V_{IN}	I_Q/V_{IN}	V_{IN} = 2.7V to 20V				0.7	µA/V
V_{OUT} Adjustment Range	V_{TRIM}	$V_{IN} \geq V_{OUT}$ + 0.2V		+75/-20	+100/-75		mV
TEMP Output Voltage Tempco	TCV_{TEMP}				2.3		mV/°C

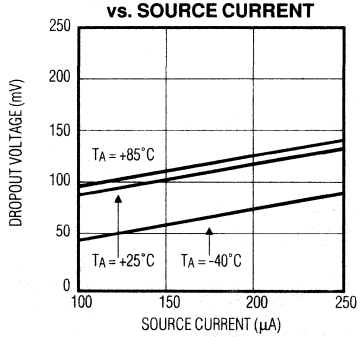
10µA, Low-Dropout, 2.5V Precision Voltage Reference

Typical Operating Characteristics

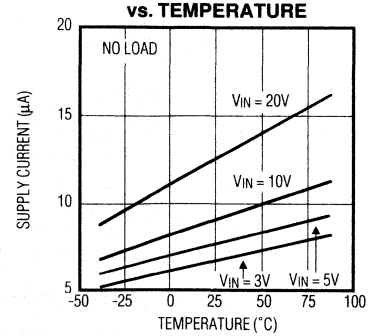
OUTPUT VOLTAGE vs. TEMPERATURE



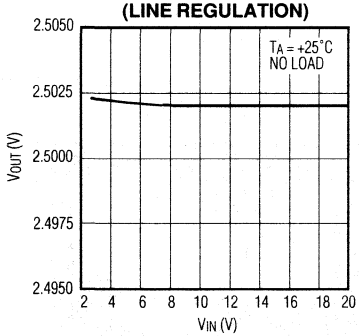
DROPOUT VOLTAGE vs. SOURCE CURRENT



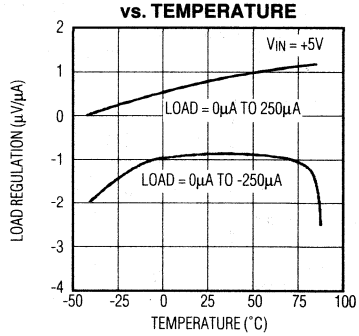
SUPPLY CURRENT vs. TEMPERATURE



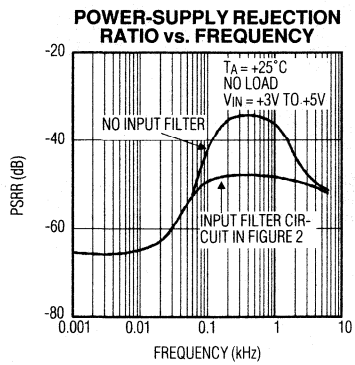
OUTPUT VOLTAGE vs. INPUT VOLTAGE (LINE REGULATION)



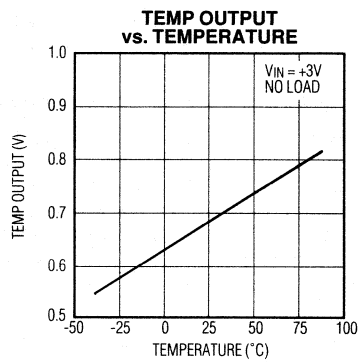
LOAD REGULATION vs. TEMPERATURE



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



TEMP OUTPUT vs. TEMPERATURE



10µA, Low-Dropout, 2.5V Precision Voltage Reference

Pin Description

PIN	NAME	DESCRIPTION
1, 7	I.C.	Internal Connection – make no connection to this pin.
2	V_{IN}	Input Voltage
3	TEMP	Temperature Proportional Output Voltage – generates an output voltage proportional to package temperature.
4	GND	Ground
5	TRIM	Output Voltage Trim – connect to the center of a voltage divider for output trimming. Otherwise, make no connection.
6	V_{OUT}	Reference Output
8	COMP	Compensation Input – connect a C_{LOAD}/100 capacitor from V_{OUT} to COMP to provide capacitive load compensation.

Applications Information

Trimming the Output Voltage

The MAX872's output voltage is trimmed for 0.2% tolerance. If additional V_{OUT} trimming is desired, connect a 1MΩ potentiometer in series with a 2MΩ resistor between V_{OUT} and ground, and connect the potentiometer's wiper to TRIM as in Figure 1.

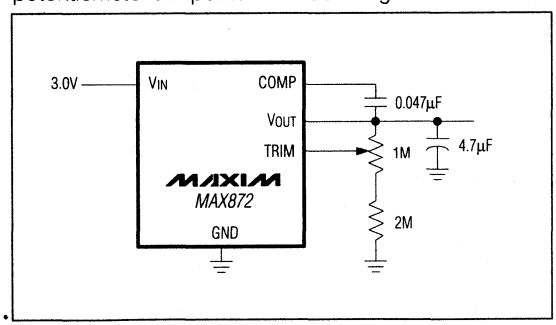


Figure 1. Adjusting V_{OUT} with TRIM Input

Adjusting V_{OUT} from its factory-trimmed voltage typically changes the output voltage tempco by 7ppm/°C per 100mV.

Reducing Input Ripple with an Input Filter

The Power-Supply Rejection Ratio vs. Frequency graph in the *Typical Operating Characteristics* shows ripple rejection between 10Hz and 2kHz. An input RC filter with a pole less than 10Hz, as shown in Figure 2, further attenuates input ripple within this band. The voltage drop across the input resistor (due to supply and load current) slightly increases the dropout voltage by (I_{LOAD} + I_{SUPPLY})(R).

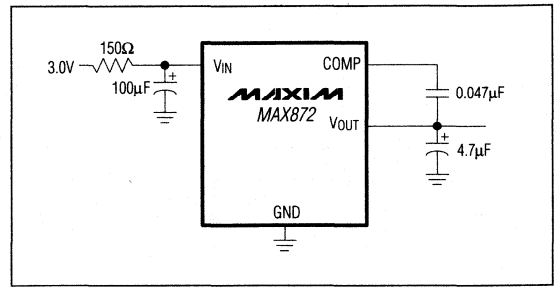


Figure 2. Input Filter Reduces Input Ripple

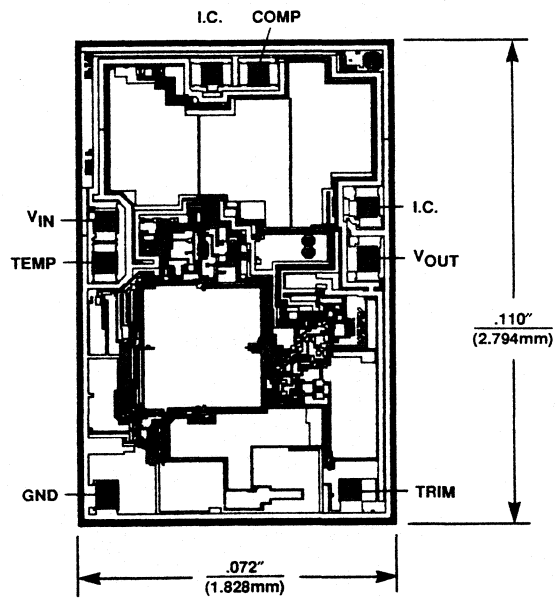
Choosing the Output and Compensation Capacitors

The output capacitor reduces load transients. The type of output capacitor is not critical; however, if the total load capacitance (C_{LOAD} = output capacitor + other capacitive load) is larger than 1000pF, connect a compensation capacitor with a value of C_{LOAD}/100 between COMP and V_{OUT}.

TEMP Output

TEMP provides an output voltage proportional to the MAX872 junction temperature. TEMP must be buffered or connected to a high-impedance input.

Chip Topography



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

6/92

MAXIM

Low-Power, Low-Drift, +2.5V Precision Voltage Reference

General Description

The MAX873 is a low-power, low-drift, precision voltage reference with a +2.5V stable output. It operates with a maximum quiescent current of 280µA while maintaining a temperature coefficient of 7ppm/°C.

The MAX873's low drift, line regulation, and load regulation make it ideal for use with 8-, 10-, and 12-bit data-acquisition systems.

Applications

Data-Acquisition Systems

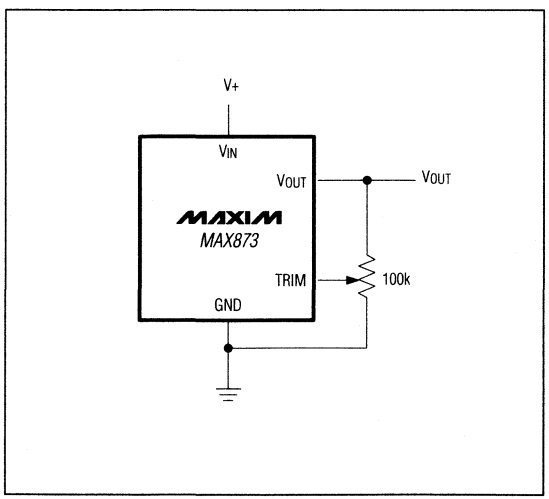
Portable Instrumentation

Logic-Powered Analog Systems

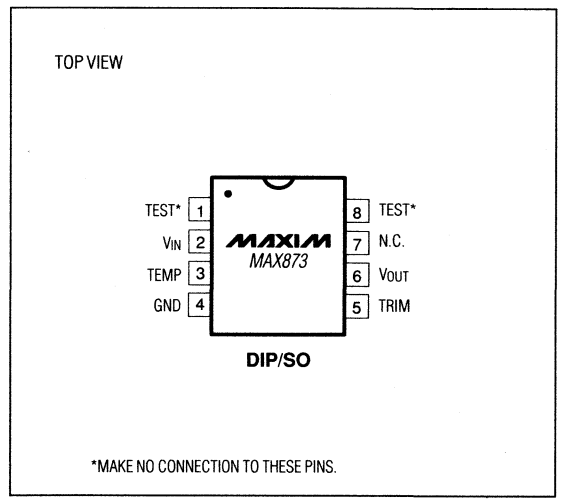
Features

- ♦ **280µA Max Supply Current**
- ♦ **Low Temperature Coefficient — 7ppm/°C**
- ♦ **+2.5V Output Tolerance — ±0.06% Max**
- ♦ **15ppm/mA Max Load Regulation**
- ♦ **4ppm/V Max Line Regulation**
- ♦ **±90mV Adjustable Output Voltage**
- ♦ **+2.0mV/°C Temperature Voltage Output**
- ♦ **All Grades Available in DIP and SO**

Typical Operating Circuit



Pin Configuration



ADVANCE INFORMATION

All information in this data sheet is preliminary and subject to change.

7/92

MAXIM

10μA, Low-Dropout, 4.096V Precision Voltage Reference

General Description

The MAX874 precision micropower voltage reference consumes a maximum of only 10μA and operates from supply voltages up to 20V while providing a precise output of 4.096V. The MAX874 sources 250μA with $V_{IN} \geq (V_{OUT} + 0.2V)$, making it ideal for use with +5V supplies. The MAX874 is trimmed to 4.096V ± 0.2%, and features a maximum 40ppm/°C drift.

Features

- ♦ **10μA Max Supply Current**
- ♦ **+4.3V to +20V Operating Voltage Range**
- ♦ **40ppm/°C Max Drift**
- ♦ **±0.2% Output Tolerance**
- ♦ **150μV/V Max Line Regulation Over Temp**
- ♦ **600μV/mA Max Load Regulation Over Temp**
- ♦ **±250μA Load Current**

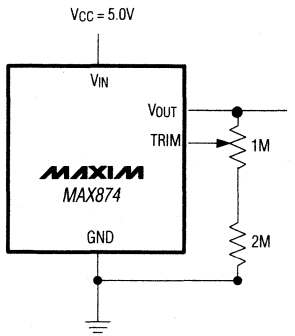
Applications

Hand-Held Instruments

Battery-Operated Equipment

Power Supplies

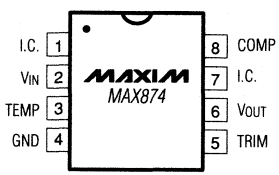
Typical Operating Circuit



REFERENCE WITH TRIMMED OUTPUT

Pin Configuration

TOP VIEW



DIP/SO

MAXIM

Appendix

A

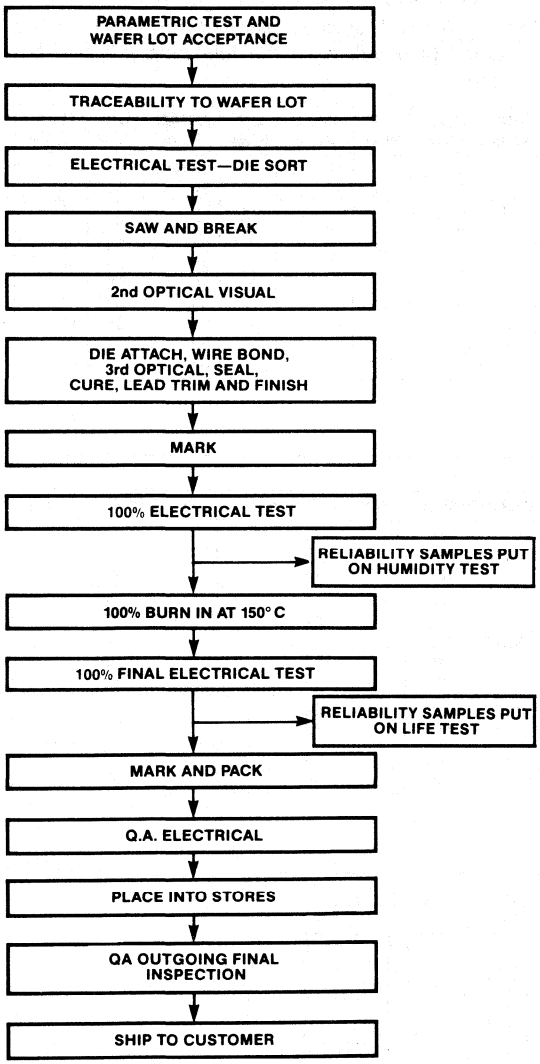
* Advance Information – first page of data sheet in preparation.

Wafer Inspection

All wafers are fabricated using specifically developed processes with extremely tight control. Each must pass numerous in-process check-points for oxide thickness, critical dimensions, pin hole densities, and other requirements, and must comply with Maxim's demanding Electrical and Physical Specifications.

Finished wafers are inspected optically to detect any physical defects. Then they are parametrically tested to insure full conformity to Maxim's specifications. Our parametric measurement capability has been specially designed by Maxim to make the precision measurements which are mandatory to insure reliability and reproducibility in analog circuits. We believe this quality control technology to be the best in the industry, capable of resolving below IpA current levels, and less than IpF capacitance. Maxim's proprietary software allows automatic measurement of subthreshold characteristics, fast surface state density, and other parameters which are crucial to predicting long term stability and reliability.

Every Maxim wafer is subject to this rigorous screening at no premium to our customers.



Testing

After wafer parametric inspection, each die is 100% tested prior to assembly. Once assembled, units are tested *over temperature.* This is not a common practice in the industry. By using the latest high speed automatic handling equipment, Maxim is able to offer "at temperature" testing for no additional cost.

Sophisticated testing is an integral part of delivering the highest quality data acquisition products. Maxim's analog test capability represents an order of magnitude improvement in accuracy, noise performance, and speed when compared to current industry standards. This provides the customer with total assurance that he will receive the part he paid for every time, without fail.

Product Conditioning and Qualification

Reliability of Maxim's products is further assured by subjecting parts to qualification cycles that include accelerated life tests equivalent to 20 million operating hours, as well as pressure and humidity (85°C/85%) cycles. In addition, *every unit shipped has been burned-in* (with the exception of reversed lead and Surface Mount Products—see below) to further reduce the possibility of field failure.

Products processed to this level are normally available from other manufacturers at a price premium, by ordering special process flows. *Maxim provides this testing and conditioning, including a 100% burn-in, at no additional cost.*

A

Maxim is committed to providing high quality, high reliability 8 to 60 lead plastic surface mount products. With few exceptions, every monolithic product will be offered in a surface mount package. These products are processed through the same manufacturing flow as the dual-in-line (DIP) plastic devices and are tested to the same stringent electrical and visual AQL levels, with the exception of 100% burn-in and cold test. They receive the same product conditioning and lot qualification as the DIPs. Maxim still assures the reliability of every lot by subjecting a sample from each lot to a long term life test prior to shipment.

Pin Convention

0.150" JEDEC SOIC (S) parts have the same pinout as in the 0.300" DIP package equivalents.

0.300" JEDEC SOIC (W) parts also have the same pinout as in the 0.300" DIP package except for selected products in the 16 lead. 14 lead products that are too large for the 0.150" 14 lead (S) package are made available in the 0.300" 16 lead (W) package.

Flatpack Pin Convention

No fixed convention exists for 40-lead products assembled in either 44-lead or 60-lead flatpack. Consult product marketing for specific pin-outs.

Quad Pack Pin Convention

1.) Devices in the 28 Lead Quad Pack are pin for pin number compatible with the DIP package. That is to say, pin 1 on the 28L Quad will be the same function as pin 1 on the DIP package.

2.) All 40 Lead devices planned for the 44 Lead Quad pack will have the following pin convention:

DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#	DIP PIN#	QUAD PIN#
	1 N/C		12 N/C		23 N/C		34 N/C
1	2	11	13	21	24	31	35
2	3	12	14	22	25	32	36
3	4	13	15	23	26	33	37
4	5	14	16	24	27	34	38
5	6	15	17	25	28	35	39
6	7	16	18	26	29	36	40
7	8	17	19	27	30	37	41
8	9	18	20	28	31	38	42
9	10	19	21	29	32	39	43
10	11	20	22	30	33	40	44

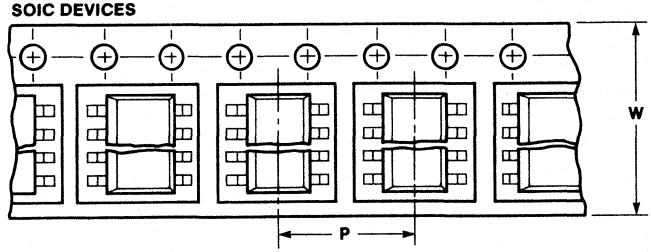
Surface Mount Packages In Reeled Tape

Maxim surface mount packages are normally shipped in antistatic plastic rails. They are also available mounted in pockets on embossed tape for customers using automatic placement systems. The tape is wound and shipped on reels.

The following table and diagrams indicate the tape sizes used for the various package types and the basic orientation convention used. Further tape and reel specifications can be found in the Electronic Industries Association (EIA) standard 481.

COMPONENT		TAPE SIZE mm (W)	PART PITCH mm (P)
SOIC	8L	12	8
	14L	16	8
	16L	16	8
SOIC	16L	16	12
	18L	24	12
	20L	24	12
	24L	24	12
	28L	24	12
PLCC	28L	24	16
	44L	32	24
PFP	44L	24	16
	60L	44	32

SOIC DEVICES



USER DIRECTION OF FEED

All of Maxim's standard products are available in die and wafer form. Every diffusion lot committed to die/wafer sales is qualified through a die sample assembled into packaged units. This sample is then subjected to "Packaged Unit Process Flow" the standard to ensure lot quality and reliability.

Electrical Specifications

All material committed to die/wafer sales is 100% electrically probed using Maxim's sophisticated test equipment. Most parameters tested are checked to limits that are more stringent than the data sheet 25°C worst case parameters.

Generally, the parameters or parameter limits listed in the packaged unit data sheets are tested during electrical probe. However some parameters are impossible to test or test with absolute accuracy on unassembled product. Information regarding any of these parameters/parameter limits may be obtained from the factory.

Physical Specifications

PARAMETER	4"	UNITS
Chip Thickness Backlapped wffers	15 ±1	mils
Die length/width tollerance	±1	mils
Bonding pads dimensions (minimum)	typical min =4x4 advanced min = 3x3	mils
Bonding pad and interconnect material thickness	10-12k	A
Storage temperature	-40 to +150	°C
Operating Temperature	-20 to +70	°C

Die and wafers are visually inspected according to MIL-STD-883, Method 2010, Condition B with modifications reflecting CMOS requirements.

Each die surface is protected by a planar passivation layer and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by plasma etching. The bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etch process.

Maxim guarantees die and wafer AQL levels as follows:

Visual	1.0%
Functional Electrical Testing	0.65%
Parametric DC Testing	2.5%
Untested Parameters	6.5%

Assembly Procedures

Handling

Maxim recommends that die and wafers be stored in a clean, dry ambient—preferably inert gas. Extreme care should be taken when handling die. Both electrical and visual damage can occur as a result of an unclean environment or harsh handling techniques.

Die Attach

To prevent oxidization the die attach operation should be done under a gaseous nitrogen ambient atmosphere. If an eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385°C and 435°C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150°C.

Bonding

Thermosonic or thermocompression gold ball bonding may be used with 1.0 or 1.3 mil diameter 99.99% pure gold wire. Ultrasonic bonding may be used with 1.0 or 1.25 mil diameter 99% aluminum/1% silicon wire.

Standard Die and Wafer Carrier Package

Die and wafers are packaged as shown in Figures 1 and 2, respectively.

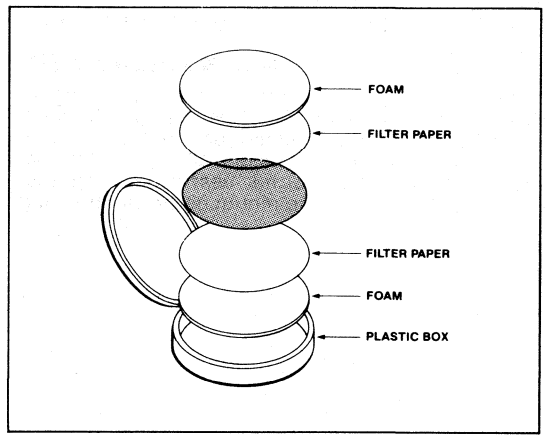


Figure 1. Wafer Carrier Package

A

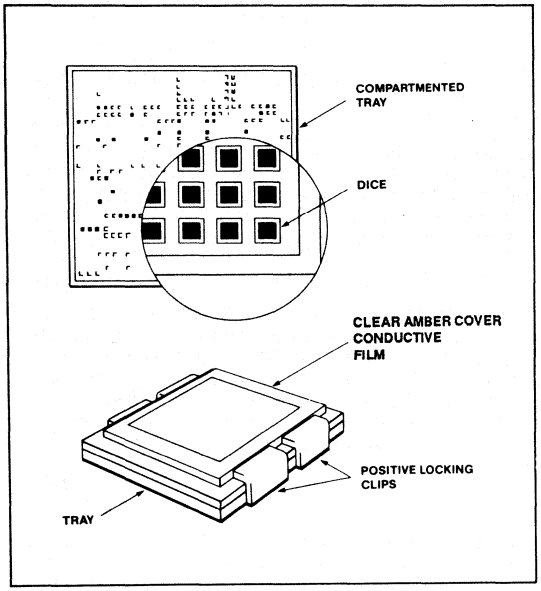


Figure 2. Die Carrier Package

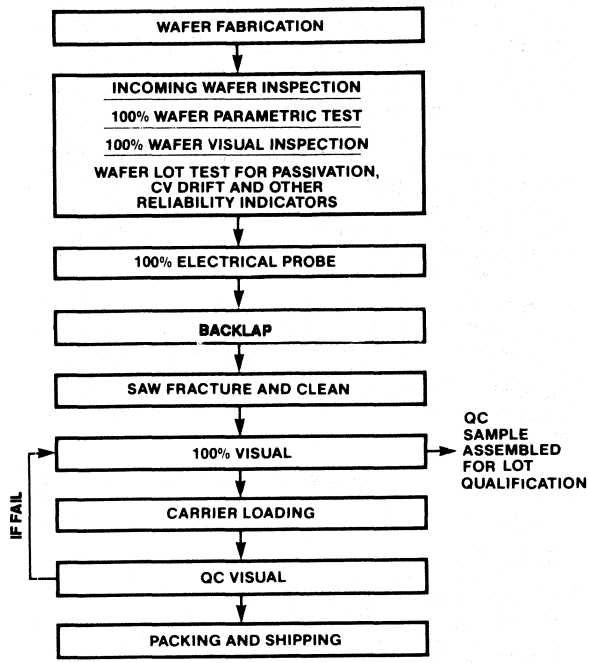
Changes

Maxim reserves the right to improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect die electrical limits, pad layouts, or maximum die sizes.

User Responsibility

Written notification of any non-conformance by Maxim or Maxim's dice specifications must be made within 75 days of the shipment date of the die to the user. Maxim assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

Dice Process Flow



Ordering Information

Die orders are identified by a /D suffix.
Example: ICL7109C/D

When ordering die in wafer form replace "D" in the part numbers with a "W"
Example: MAX7231C/D Die = MAX7231C/W Wafer.

/HR Program

Prior to the inception of the /883 program, Maxim offered its products in a high-reliability (/HR) flow. Maxim will continue to offer this highly successful processing program for customers requiring military-grade product, but who do not want to pay the substantial cost added for certified product in full compliance to MIL-STD-883.

The /HR program offers device processing that emulates Mil Method 5004 processing, including full-material traceability and process genealogy from incoming raw materials through final shipment. However, full QCI testing is only performed if requested. Only Group A of Mil Method 5005 is done per lot. Groups B, C, and D must be specifically requested when placing orders. This is done by placing a single letter suffix (B,C, or D) at the end of the ordered part number, as seen in the chart below.

In addition to the /HR flow for hermetic-packaged products, Maxim offers a High-Reliability (Hi-Rel) Plastic Flow. This flow screens plastic-encapsulated products built in standard plastic DIP and small-outline packages. Units are inspected for internal visual, temperature cycle per Mil-STD-883, Method 1010, 10 cycles, and external visual/ mechanical inspection prior to shipment to the testing facility. Screening includes 100% pre burn-in electrical test at T_A = +25°C, burn-in per Mil-STD-883, Method 1015. Post burn-in electrical test includes dynamic, static, AC, DC, and functional test at T_A = +25°C, with a 5% PDA applied to DC +25°C only. Screening to maximum operating temperature is performed 100% and minimum operating temperature is screened to 0.1% AQL. Group A lot acceptance must meet a standard sample plan for 0.1% AQL to the applicable detail specification.

Ordered Part #	Processing
MAX358MJE/HR	Device will be processed through the full /HR Flow emulating Mil Method 5004 and QCI tested to Group A of Mil Method 5005.
MAX358MJE/HRB	Same as above with the addition of Mil Method 5005 Group B testing. QCI contains both Group A and B.
MAX358MJE/HRC	Same as above except QCI includes Group C. QCI now contains Groups A, B, and C.
MAX358MJE/HRD	Same as above except QCI includes Group D. QCI now contains Groups A, B, C, and D.

To order /883 or /HR devices, contact the Maxim sales representative or distributor in your area.

/883 Program

Maxim began its High-Reliability (Hi-Rel) operation on July 1, 1988. At that time, our product offering was limited to 25 device types. But with the purchase of MAXFAB wafer-fabrication facility in December 1990, the Hi-Rel product group was expanded to include more than 140 device types. We began shipping our first /883-compliant products from MAXFAB in August 1991.

All /883 products manufactured by Maxim are in full compliance to paragraph 1.2.1 of MIL-STD-883. Electrical screening is performed per Method 5004, and QCI inspection per Method 5005, Groups A, B, C, and D.

We also offer Standard Military Drawings (SMDs) and products screened to Customer Source Control Drawings (SCDs). We invite you to visit our facility for a first-hand inspection, and look forward to serving you. Contact your local sales representative or the factory directly, (408) 737-7600 extension 6304, for free samples or literature. You may place small-quantity orders using your VISA or MasterCard.

Proprietary and Second Source Numbering System

Maxim's Proprietary Numbering System

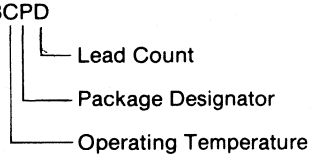
Maxim's proprietary product introductions are increasing at a significant rate. The devices are grouped by their functions into certain categories. Maxim presently uses a "MAX" as the prefix to the device's unique number. The categories are as follows:

MAX100-199	Analog-to-Digital Converters
MAX200-299	Interface
MAX300-399	Analog Switches and Multiplexers
MAX400-499	Op-Amps, Buffers and Video Amplifiers
MAX500-599	Digital-to-Analog Converters
MAX600-699	Power Supply Circuits and Voltage References
MAX700-799	µP Peripherals and Display Drivers
MAX800-899	Open
MAX900-999	Open

Within each category, blocks of numbers are reserved for sub-groups.

3 Letter Suffixes

EXAMPLE: MAX358CPD



Temperature Range

"C"	0°C to +70°C
"I"	-20°C to +85°C
"E"	-40°C to +85°C
"M"	-55°C to +125°C

Package

"A"	TO-237
"C"	TO-220
"D"	Ceramic Sidebraze
"F"	Ceramic Flat-Pack
"H"	TO-66
"J"	CERDIP Dual-In-Line
"K"	TO-3
"L"	Leadless, Ceramic
"M"	Plastic Flat Pack
"N"	Narrow Plastic Dual-In-Line
"P"	Plastic Dual-In-Line
"Q"	Plastic Chip Carrier (Quad Pak)
"R"	Narrow CERDIP (24 pin, 0.3" wide)
"S"	Small Outline, Slim (8 or more leads), 150 mil
"S"	TO-52 (2 or 3 leads)
"T"	TO-5 Type (also TO-78, TO-99, TO-100)
"U"	TO-72 Type (also TO-18, TO-71)
"V"	TO-39
"W"	Small Outline, Wide (300 mil)
"Z"	TO-92
"/D"	Dice
"/W"	Wafer
"-1"	On Package Information Indicates Hybrid Circuit

Number of Pins

"A"	8	"P"	20
"B"	10	"Q"	2
"C"	12	"R"	3
"D"	14	"S"	4
"E"	16	"T"	6
"F"	22	"U"	60
"G"	24	"V"	8 (0.200" pin circle, isolated case)
"H"	44		
"I"	28	"W"	10 (0.230" pin circle, isolated case)
"J"	32		
"L"	40	"Y"	8 (0.200" pin circle, case to pin 4)
"M"	48		
"N"	18	"Z"	10 (0.230" pin circle, case to pin 5)

4 Letter Suffixes

The first letter of the suffix is used to denote product grade, for example, MAX631ACPA means 5% output accuracy (A), the remaining 3 letters denote temperature range, package type and number of leads. Therefore, the MAX631ACPA operates over the 0°C to +70°C and is in a Plastic Dual-in-Line package and has 8 leads.

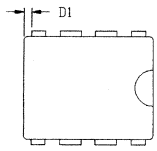
Second Source Products

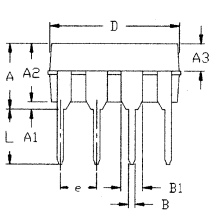
In most cases, Maxim's part number for a multiple source product follows the numbering system that is most widely accepted in the industry for that particular part, rather than our own convention. This includes original designators for package type, temperature range, and performance grades as well as the most commonly recognized prefix.

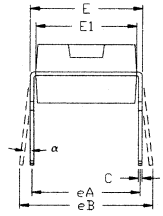
Multiple source products are frequently supplied by Maxim in packages or temperature ranges that are not supplied by other manufacturers. Whenever possible, such a device is given the part number that it would have if the original numbering convention were followed. For example, if a military temperature grade of a product is not supplied by other sources but is available from Maxim, the original manufacturer's designation for military temperature will be used. As a result, a specific part number supplied by Maxim may not be listed by the "original" manufacturer.

Package Information

This section contains physical dimensions and thermal data for all packages currently supplied by Maxim. Each drawing is followed by a two letter code which indicates package type (Plastic DIP, Small Outline, etc.) and number of leads. This code is also used, along with indicators for temperature range and device grade (where appropriate) in the part number suffix for each of Maxim's proprietary devices.



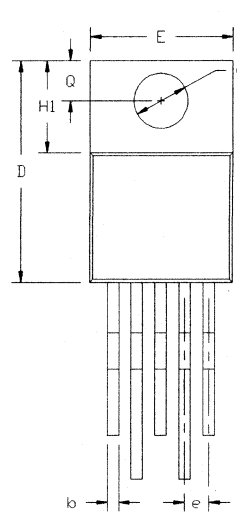


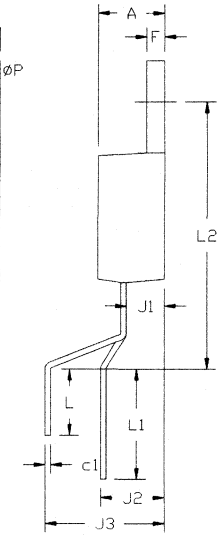


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.348	0.390	8.84	9.91
D1	0.005	0.035	0.13	0.89
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	BSC	2.54	BSC
eA	0.300	BSC	7.62	BSC
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010"
2. CONTROLLING DIMENSION: INCH
3. MEETS JEDEC MS-001 AB

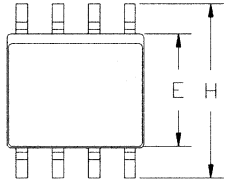
MAXIM PROPRIETARY INFORMATION
TITLE: 8L PDIP OUTLINE
APPROVAL | DWG 21-324 | REV A

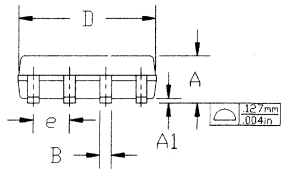


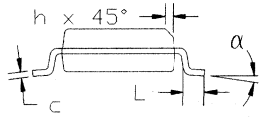


	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.140	0.190	3.56	4.82
b	0.015	0.040	0.38	1.01
c1	0.014	0.022	0.41	0.50
D	0.560	0.650	14.23	16.51
E	0.380	0.420	9.66	10.66
e	0.067 BSC		1.70 BSC	
F	0.045	0.055	1.14	1.39
H1	0.230	0.270	5.85	6.85
J1	0.080	0.115	2.04	2.92
J2	0.170	0.185	4.32	4.70
J3	0.327	0.335	8.31	8.51
L	0.170	0.200	4.32	5.08
L1	0.260	0.340	6.60	8.64
L2	0.700	0.720	17.78	18.29
ØP	0.139	0.161	3.54	4.08
Q	0.100	0.120	2.54	3.04

MAXIM PROPRIETARY INFORMATION
TITLE: CASE OUTLINE, TO-220 5L, STAGGERED
APPROVAL | DWG 21-0005 | REV 0 | 1/1



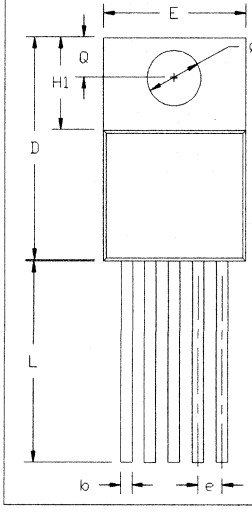


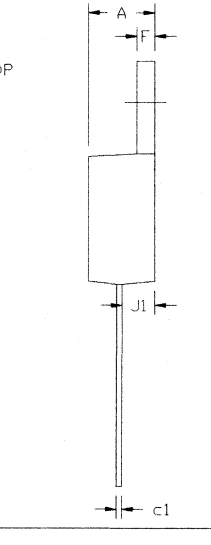


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 AA.

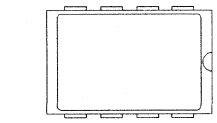
MAXIM PROPRIETARY INFORMATION
TITLE: 8L SOIC OUTLINE
APPROVAL | DWG 21-325 | REV A



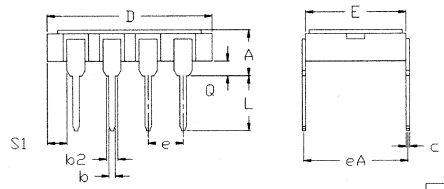


	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.140	0.190	3.56	4.82
b	0.015	0.040	0.38	1.01
c1	0.014	0.022	0.41	0.50
D	0.560	0.650	14.23	16.51
E	0.380	0.420	9.66	10.66
e	0.067 BSC		1.70 BSC	
F	0.045	0.055	1.14	1.39
H1	0.230	0.270	5.85	6.85
J1	0.080	0.115	2.04	2.92
L	0.500	0.580	12.70	14.73
ØP	0.139	0.161	3.54	4.08
Q	0.100	0.120	2.54	3.04

MAXIM PROPRIETARY INFORMATION
TITLE: CASE OUTLINE, TO-220 5L, STRAIGHT
APPROVAL | DWG 21-4737 | REV 0 | 1/1

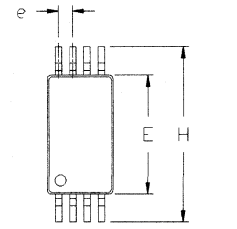


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
b	0.014	0.026	0.36	0.66
b2	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.45
D	---	0.405	---	10.29
E	0.220	0.310	5.59	7.87
eA	0.300	BSC	7.62	BSC
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	---	0.13	---

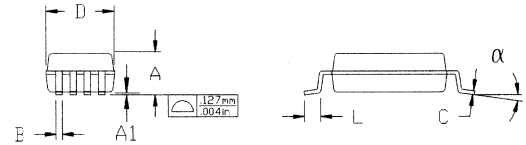


MEETS 1835 CASE "P"; D-4, CONFIGURATION #3
EXCEPT D AND S MAXIMUM DIMENSIONS.

MAXIM
PROPRIETARY INFORMATION
TITLE: 8L SIDEBRAZE OUTLINE
APPROVAL | DWG: 21-0327 | REV: A

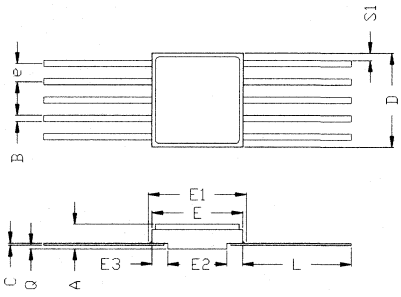


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
D	0.113	0.123	2.87	3.13
e	0.0256	BSC	0.65	BSC
E	0.205	0.212	5.20	5.38
H	0.301	0.311	7.65	7.9
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°



NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETER

MAXIM
PROPRIETARY INFORMATION
TITLE: CASE OUTLINE, SSOP, 8L
APPROVAL | DWG: 21-0004 | REV: 0 | 1/1

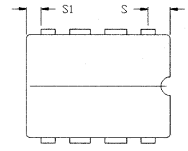


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.045	0.090	1.14	2.29
b	0.010	0.022	0.25	0.056
c	0.004	0.009	0.10	0.23
D	---	0.280	---	7.11
E	0.240	0.260	6.10	6.60
E1	---	0.300	---	7.62
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	N/A	N/A	N/A	N/A
L	0.250	0.370	6.35	9.40
Q	0.026	0.045	0.66	1.14
s1	0.005	---	0.13	---

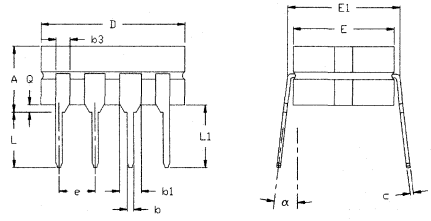
NOTES:
1. CONTROLLING DIMENSION: INCH
2. PACKAGE MEETS 1835 F4 CONFIGURATION B AND F4A CONFIGURATION B

MAXIM
PROPRIETARY INFORMATION
TITLE: 10L FLATPACK PACKAGE OUTLINE MIL 1835 COMPLIANT
APPROVAL | DWG: 21-0010 | REV: A | 1/1

F10-2

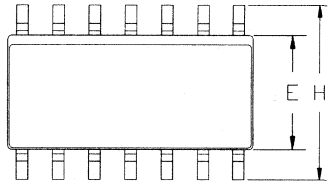


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
b	0.014	0.023	0.36	0.58
b1	0.038	0.065	0.97	1.65
b3	0.023	0.045	0.58	1.14
c	0.008	0.015	0.20	0.38
D	---	0.405	---	10.29
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
L1	0.150	---	3.81	---
Q	0.015	0.060	0.38	1.52
S	---	0.055	---	1.40
S1	0.005	---	0.13	---
α	0°	15°	0°	15°

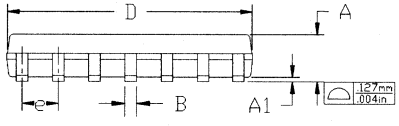


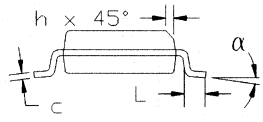
MEETS 38510 CASE "P"; D-4, CONFIGURATION #1

MAXIM
PROPRIETARY INFORMATION
TITLE: 8L CERDIP OUTLINE
APPROVAL | DWG: 21-326 | REV: C



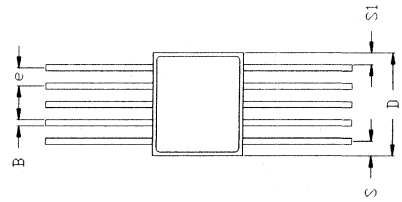
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.337	0.344	8.55	8.75
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

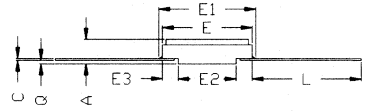




NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 AB.

MAXIM
PROPRIETARY INFORMATION
TITLE: 14L SOIC OUTLINE
APPROVAL | DWG: 21-331 | REV: A



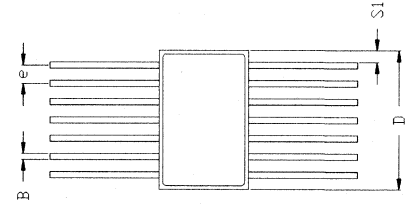


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
B	0.010	0.019	0.25	0.48
C	0.003	0.006	0.08	0.15
D	---	0.290	---	7.37
E	0.240	0.260	6.10	6.60
E1	---	0.280	---	7.11
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.250	0.370	6.35	9.40
Q	0.010	0.016	0.25	0.41
S	---	0.045	---	1.14
S1	0.005	---	0.13	---

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 38510 F-4A CONFIGURATION #2 EXCEPT DIMENSION "Q" MIN

F10-1

MAXIM
PROPRIETARY INFORMATION
TITLE: 10L FLATPACK PACKAGE OUTLINE NON-COMPLIANT DIMENSIONS
APPROVAL | DWG: 21-0014 | REV: A | 1/1

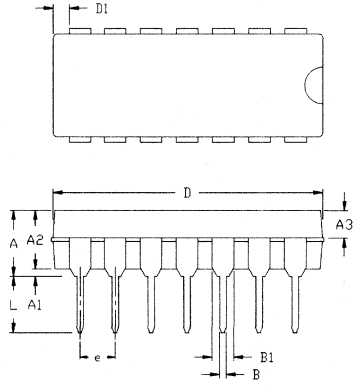


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.045	0.115	1.14	2.92
b	0.015	0.022	0.38	0.56
c	0.004	0.009	0.10	0.23
D	---	0.390	---	9.91
E	0.235	0.260	5.97	6.60
E1	---	0.290	---	7.37
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.270	0.370	6.86	9.40
Q	0.026	0.045	0.66	1.14
s1	0.005	---	0.13	---

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS MIL STD 1835 F-2A CONFIGURATION B

F14-2

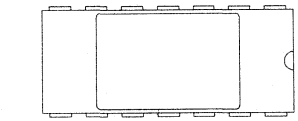
MAXIM
PROPRIETARY INFORMATION
TITLE: 14L FLATPACK PACKAGE OUTLINE MIL 1835 COMPLIANT
APPROVAL | DWG: 21-0011 | REV: A | 1/1



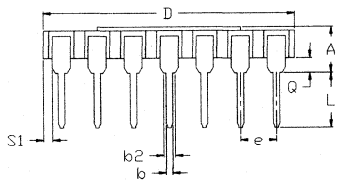
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.735	0.765	18.67	19.43
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	BSC	2.54	BSC
eA	0.300	BSC	7.62	BSC
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010"
2. CONTROLLING DIMENSION: INCH
3. MEETS JEDEC MS-001 AC

MAXIM
PROPRIETARY INFORMATION
TITLE: 14L PDIP OUTLINE
APPROVAL | DWG: 21-330 | REV: A

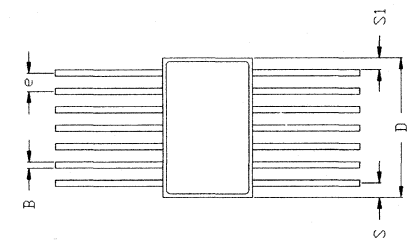


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
b	0.014	0.026	0.36	0.66
b2	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	---	0.785	---	19.94
E	0.220	0.310	5.59	7.87
eA	0.290	0.320	7.37	8.13
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	---	0.13	---



MEETS 1835 CASE "C"; D-1, CONFIGURATION #3

MAXIM
PROPRIETARY INFORMATION
TITLE: 14L SIDEBRAZE OUTLINE
APPROVAL | DWG: 21-0586 | REV: A

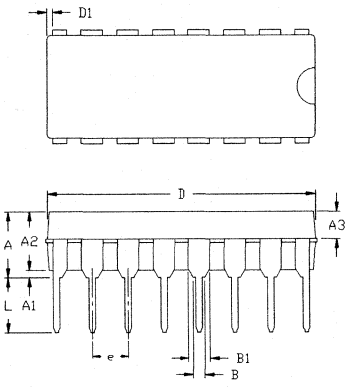


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.045	0.115	1.14	2.92
B	0.015	0.019	0.38	0.48
C	0.003	0.006	0.08	0.15
D	---	0.390	---	9.91
E	0.235	0.260	5.97	6.60
E1	---	0.290	---	7.37
E2	0.125	---	3.18	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.270	0.370	6.86	9.40
Q	0.012	0.030	0.30	0.76
S	---	0.045	---	1.14
S1	0.005	---	0.13	---

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 3851C F-2A CONFIGURATION #2
   EXCEPT DIMENSION "Q" MIN

MAXIM
PROPRIETARY INFORMATION
TITLE: 14L FLATPACK PACKAGE OUTLINE
NON-COMPLIANT DIMENSIONS
APPROVAL | DWG: 21-0012 | REV: A | 1/1

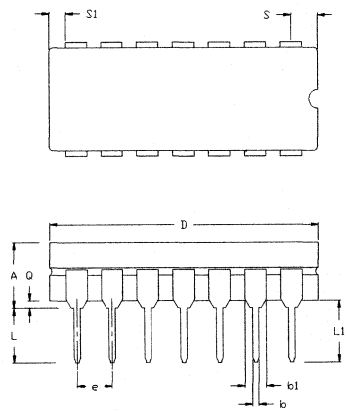
F14-1



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.745	0.765	18.92	19.43
D1	0.005	0.030	0.13	0.76
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	BSC	2.54	BSC
eA	0.300	BSC	7.62	BSC
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010"
2. CONTROLLING DIMENSION: INCH
3. MEETS JEDEC MS-001 AA

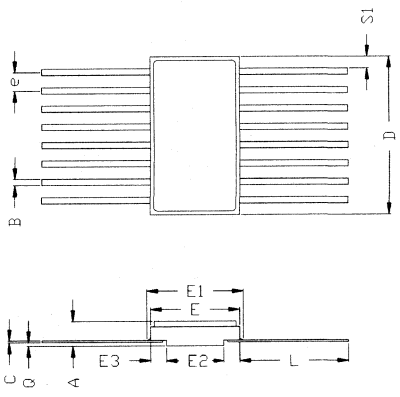
MAXIM
PROPRIETARY INFORMATION
TITLE: 16L PDIP OUTLINE
APPROVAL | DWG: 21-587 | REV: A



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
b	0.014	0.023	0.36	0.58
b1	0.038	0.065	0.97	1.65
c	0.008	0.015	0.20	0.38
D	---	0.785	---	19.94
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
L1	0.150	---	3.81	---
Q	0.015	0.060	0.38	1.52
S	---	0.098	---	2.49
S1	0.005	---	0.13	---
α	0°	15°	0°	15°

MEETS 38510 CASE "C"; D-1, CONFIGURATION #1

MAXIM
PROPRIETARY INFORMATION
TITLE: 14L CERDIP OUTLINE
APPROVAL | DWG: 21-332 | REV: B

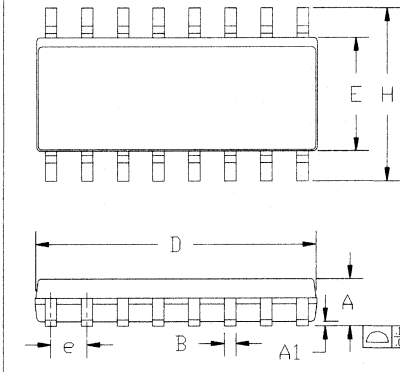


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.045	0.115	1.14	2.92
b	0.015	0.022	0.38	0.56
c	0.004	0.009	0.10	0.23
D	---	0.440	---	11.18
E	0.245	0.285	6.22	7.24
E1	---	0.315	---	8.00
E2	0.130	---	3.30	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.250	0.370	6.35	9.40
Q	0.026	0.045	0.66	1.14
s1	0.005	---	0.13	---

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS MIL STD 1835 F-5A CONFIGURATION B

F16-2

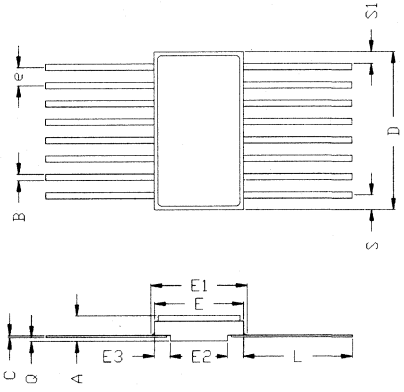
PROPRIETARY INFORMATION
TITLE: 16L FLATPACK PACKAGE OUTLINE MIL 1835 COMPLIANT
APPROVAL | DWG 21-0013 | REV A | 1/1



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.00
e	0.050	BSC	1.27	BSC
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-012 AC.

PROPRIETARY INFORMATION
TITLE: 16L (N) SOIC OUTLINE
APPROVAL | DWG 21-588 | REV B

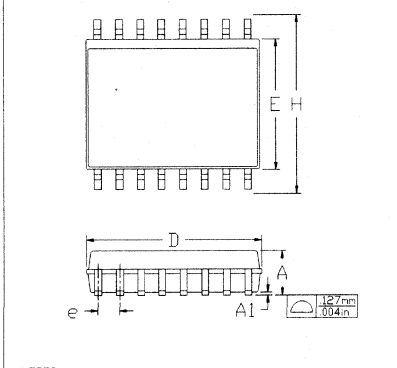


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.045	0.115	1.14	2.92
B	0.015	0.019	0.38	0.48
C	0.003	0.006	0.08	0.15
D	---	0.440	---	11.18
E	0.245	0.285	6.22	7.24
E1	---	0.315	---	8.00
E2	0.130	---	3.30	---
E3	0.030	---	0.76	---
e	0.050	BSC	1.27	BSC
k	---	---	---	---
L	0.250	0.370	6.35	9.40
Q	0.010	0.016	0.25	0.41
S	---	0.045	---	1.14
S1	0.005	---	0.13	---

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 38510 F-5A CONFIGURATION #2 EXCEPT DIMENSION "Q" MIN

F16-1

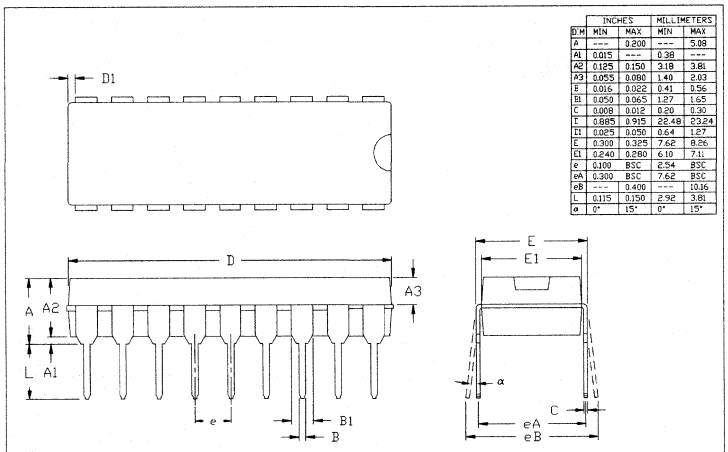
PROPRIETARY INFORMATION
TITLE: 16L FLATPACK PACKAGE OUTLINE NON-COMPLIANT DIMENSIONS
APPROVAL | DWG 21-828 | REV B | 1/1



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.398	0.413	10.10	10.50
e	0.050	BSC	1.27	BSC
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-013 AA.

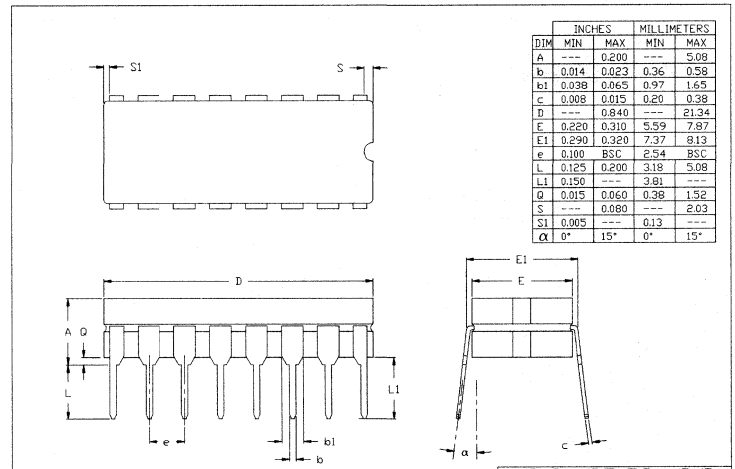
PROPRIETARY INFORMATION
TITLE: 16L (W) SOIC OUTLINE
APPROVAL | DWG 21-589 | REV B



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.885	0.915	22.48	23.24
E1	0.025	0.050	0.64	1.27
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	BSC	2.54	BSC
eA	0.300	BSC	7.62	BSC
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010"
2. CONTROLLING DIMENSION: INCH
3. MEETS JEDEC MS-001 AD

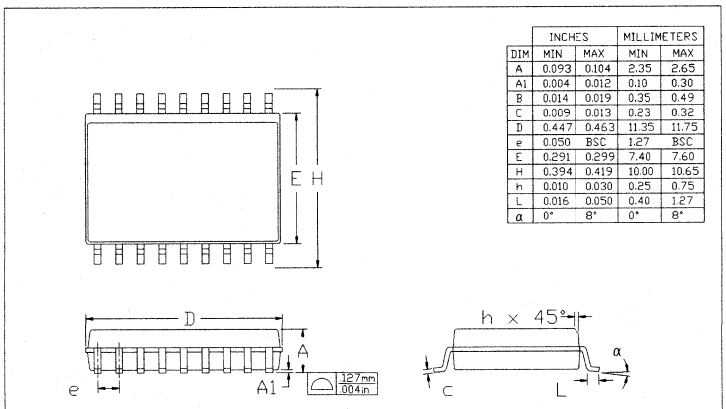
MAXIM
PROPRIETARY INFORMATION
TITLE: 18L PDIP OUTLINE
APPROVAL | DWG: 21-592 | REV: A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
b	0.014	0.023	0.36	0.58
b1	0.038	0.065	0.97	1.65
c	0.008	0.015	0.20	0.38
D	---	0.840	---	21.34
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
L1	0.150	---	3.81	---
Q	0.015	0.060	0.38	1.52
S	---	0.080	---	2.03
S1	0.005	---	0.13	---
α	0°	15°	0°	15°

MEETS 38510 CASE "E"; D-2, CONFIGURATION #1

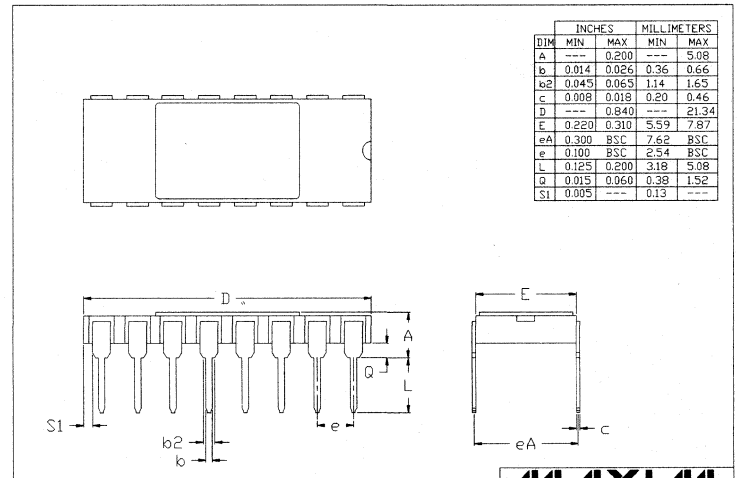
MAXIM
PROPRIETARY INFORMATION
TITLE: 16L CERDIP OUTLINE
APPROVAL | DWG: 21-590 | REV: B



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.447	0.463	11.35	11.75
e	0.050	BSC	1.27	BSC
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT
   TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-013 AB

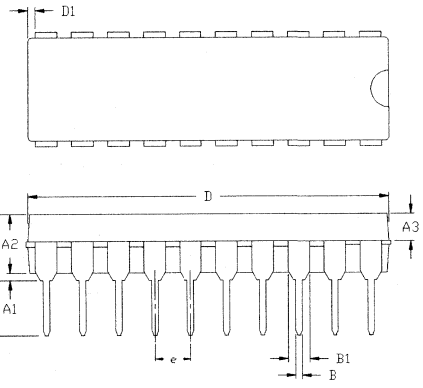
MAXIM
PROPRIETARY INFORMATION
TITLE: 18L SCIC OUTLINE
APPROVAL | DWG: | REV: A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
b	0.014	0.026	0.36	0.66
b2	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	---	0.840	---	21.34
E	0.220	0.310	5.59	7.87
eA	0.300	BSC	7.62	BSC
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	---	0.13	---

MEETS 1835 CASE "E"; D-2, CONFIGURATION #3

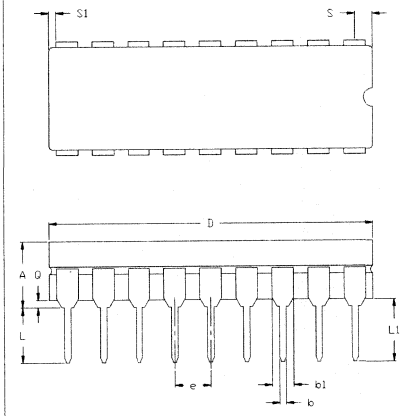
MAXIM
PROPRIETARY INFORMATION
TITLE: 16L SIDEBRAZE OUTLINE
APPROVAL | DWG: 21-0591 | REV: A



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.059	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	1.015	1.045	25.78	26.54
D1	0.040	0.070	1.02	1.78
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	BSC	2.54	BSC
eA	0.300	BSC	7.62	BSC
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010"
2. CONTROLLING DIMENSION: INCH
3. MEETS JEDEC MS-001 AE

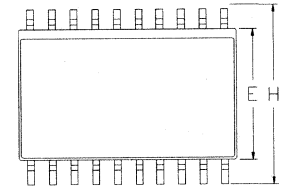
MAXIM
PROPRIETARY INFORMATION
TITLE: 20L PDIP OUTLINE
APPROVAL | DWG: 21-333 | REV: A



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
b	0.014	0.023	0.36	0.58
b1	0.038	0.065	0.97	1.65
c	0.008	0.015	0.20	0.38
D	---	0.960	---	24.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
L1	0.150	---	3.81	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---
α	0°	15°	0°	15°

MEETS 38510 CASE "V"; D-6, CONFIGURATION #1

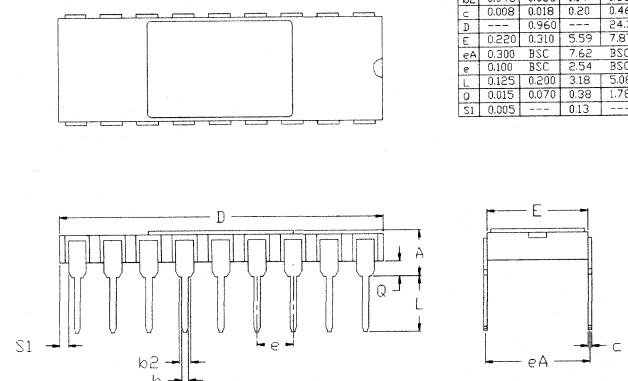
MAXIM
PROPRIETARY INFORMATION
TITLE: 18L CERDIP OUTLINE
APPROVAL | DWG: 21-594 | REV: B



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.496	0.512	12.60	13.00
e	0.050	BSC	1.27	BSC
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT
   TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-013 AC

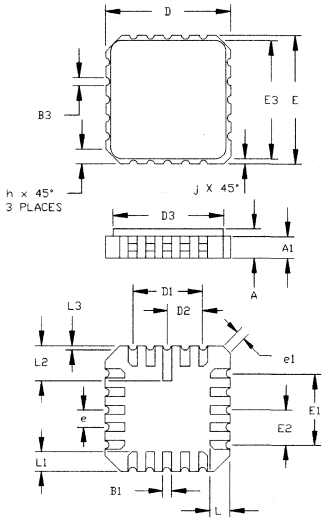
MAXIM
PROPRIETARY INFORMATION
TITLE: 20L SOIC OUTLINE
APPROVAL | DWG: 21-334 | REV: A



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
b	0.014	0.026	0.36	0.66
b2	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	---	0.960	---	24.38
E	0.220	0.310	5.59	7.87
eA	0.300	BSC	7.62	BSC
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	---	0.13	---

MEETS 1835 CASE "V"; D-6, CONFIGURATION #3

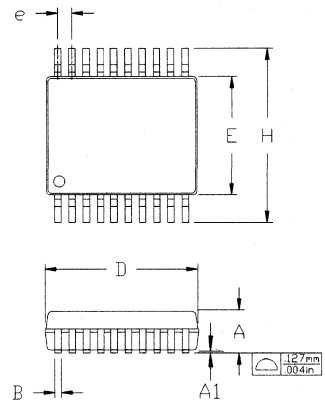
MAXIM
PROPRIETARY INFORMATION
TITLE: 18L SIDEBRAZE OUTLINE
APPROVAL | DWG: 21-0595 | REV: A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.342	0.358	8.69	9.09
D1/E1	0.200 BSC		5.08 BSC	
D2/E2	0.100 BSC		2.54 BSC	
D3/E3	---	0.350	---	9.09
e	0.050 BSC		1.27 BSC	
e1	0.015	---	0.38	---
h	0.040 REF		1.02 REF	
j	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 38510 C-2

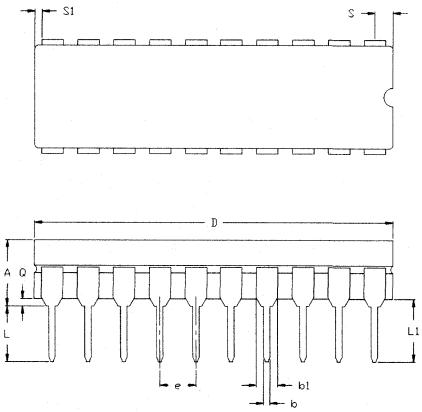
MAXIM — PROPRIETARY INFORMATION
TITLE: 20L LCC OUTLINE
APPROVAL | DWG 21-658 | REV A | 1/1



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
D	0.278	0.289	7.07	7.33
e	0.0256	BSC	0.65	BSC
E	0.205	0.212	5.20	5.38
H	0.301	0.311	7.65	7.9
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

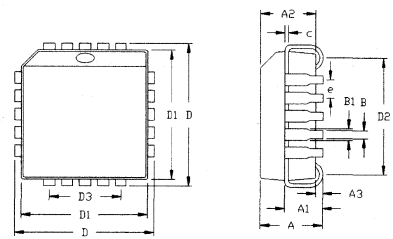
MAXIM — PROPRIETARY INFORMATION
TITLE: CASE OUTLINE, SSOP, 20L
APPROVAL | DWG 21-0003 | REV 0 | 1/1



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
b	0.014	0.023	0.36	0.58
b1	0.038	0.065	0.97	1.65
c	0.008	0.015	0.20	0.38
D	---	1.060	---	26.92
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
L1	0.150	---	3.81	---
Q	0.015	0.070	0.38	1.78
S	---	0.080	---	2.03
S1	0.005	---	0.13	---
α	0°	15°	0°	15°

MEETS 38510 CASE "R"; D-8, CONFIGURATION #1

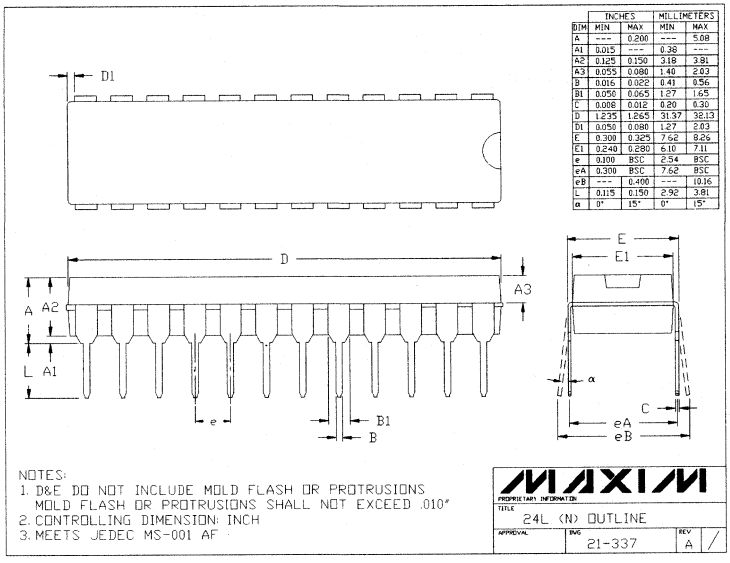
MAXIM — PROPRIETARY INFORMATION
TITLE: 20L CERDIP OUTLINE
APPROVAL | DWG 21-335 | REV B | /



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.100	0.110	2.54	2.79
A2	0.145	0.156	3.68	3.96
A3	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
D	0.385	0.395	9.78	10.03
D1	0.350	0.355	8.89	9.02
D2	0.290	0.330	7.37	8.38
D3	0.200 REF		5.08 REF	
e	0.050 REF		1.27 REF	

NOTES:
1. DIMENSION D1 DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .20mm(.008") PER SIDE.
3. CONTROLLING DIMENSION: INCH
4. MEETS JEDEC MO-047AA.

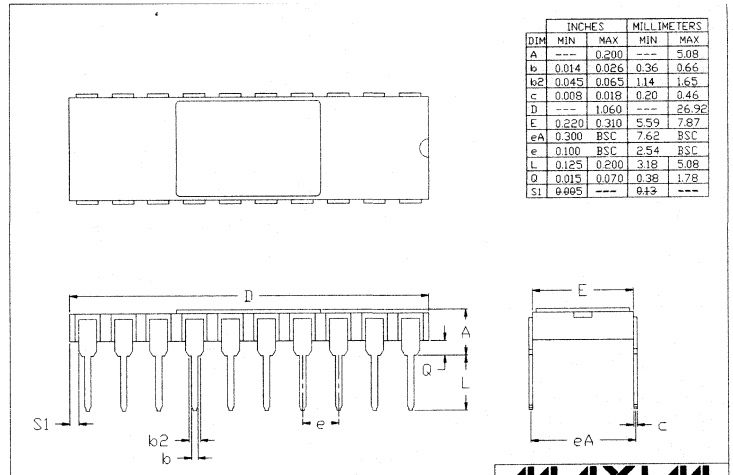
MAXIM — PROPRIETARY INFORMATION
TITLE: 20L PLCC PACKAGE OUTLINE
APPROVAL | DWG 21-981 | REV A | 1/1



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	1.235	1.265	31.37	32.13
D1	0.050	0.080	1.27	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100	BSC	2.54	BSC
eA	0.300	BSC	7.62	BSC
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010"
2. CONTROLLING DIMENSION: INCH
3. MEETS JEDEC MS-001 AF

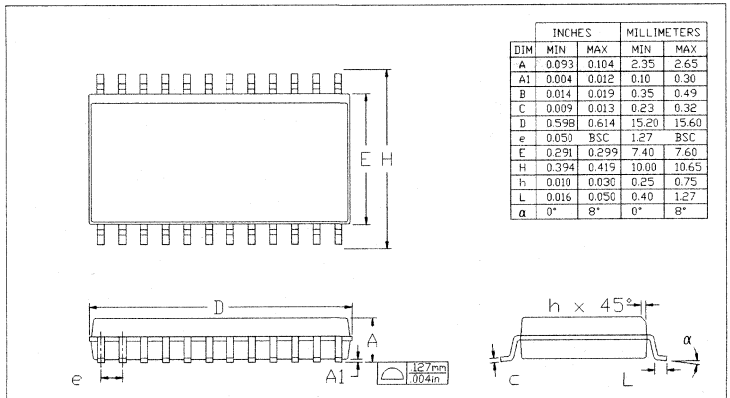
PROPRIETARY INFORMATION
TITLE: 24L (N) OUTLINE
APPROVAL | DWG 21-337 | REV A



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
b	0.014	0.026	0.36	0.66
b2	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	---	1.060	---	26.92
E	0.220	0.310	5.59	7.87
eA	0.300	BSC	7.62	BSC
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	---	0.13	---

MEETS 1835 CASE "R"; D-8, CONFIGURATION #3

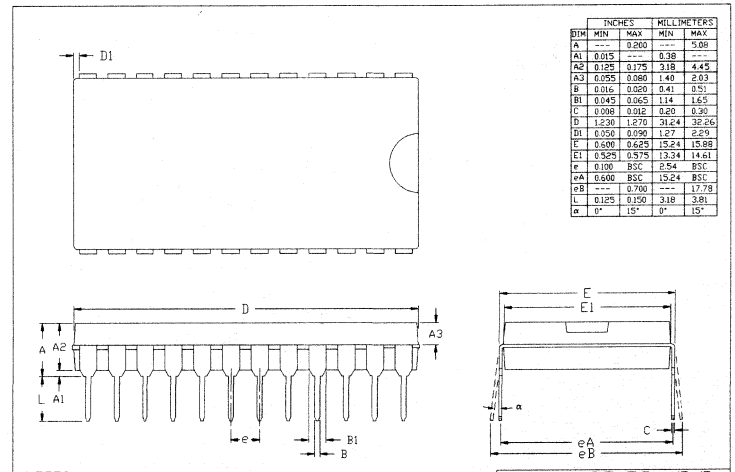
PROPRIETARY INFORMATION
TITLE: 20L SIDEBRAZE OUTLINE
APPROVAL | DWG 21-0336 | REV A



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.598	0.614	15.20	15.60
e	0.050	BSC	1.27	BSC
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT
   TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-013 AD

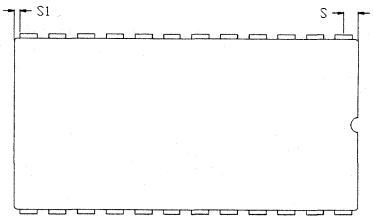
PROPRIETARY INFORMATION
TITLE: 24L SOIC OUTLINE
APPROVAL | DWG 21-338 | REV A



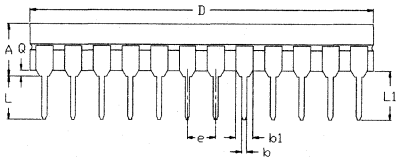
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D	1.230	1.270	31.24	32.26
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100	BSC	2.54	BSC
eA	0.600	BSC	15.24	BSC
eB	---	0.700	---	17.78
L	0.125	0.150	3.18	3.81
α	0°	15°	0°	15°

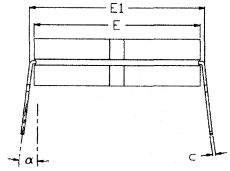
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010"
2. CONTROLLING DIMENSION: INCH
3. SIMILIAR TO JEDEC MO-015 AA

PROPRIETARY INFORMATION
TITLE: 24L PDIP OUTLINE
APPROVAL | DWG 21-1313 | REV A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.225	---	5.72
b	0.014	0.023	0.36	0.58
b1	0.038	0.065	0.97	1.65
c	0.008	0.015	0.20	0.38
D	---	1.290	---	32.77
E	0.500	0.610	12.70	15.49
E1	0.590	0.620	14.99	15.75
e	0.100	BSC	2.54	BSC
L	0.120	0.200	3.05	5.08
L1	0.150	---	3.81	---
Q	0.015	0.075	0.38	1.91
S	---	0.098	---	2.49
S1	0.005	---	0.13	---
α	0°	15°	0°	15°



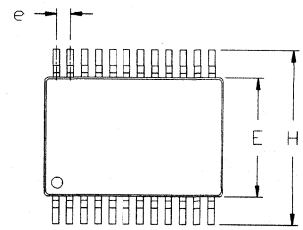


MEETS 38510 CASE "J"; D-3, CONFIGURATION #1

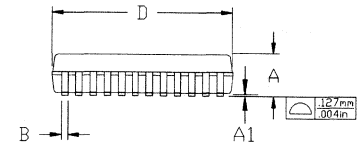
PROPRIETARY INFORMATION

TITLE: 24L CERDIP OUTLINE

APPROVAL	DWG	REV
	21-339	A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
D	0.278	0.328	8.07	8.33
e	0.0256	BSC	0.65	BSC
E	0.205	0.212	5.20	5.38
H	0.301	0.311	7.65	7.9
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°

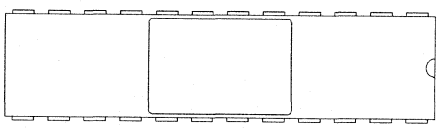


NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETER

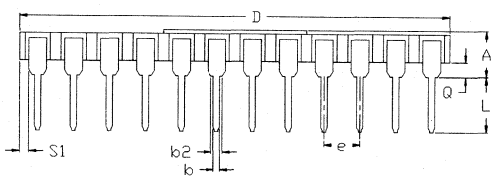
PROPRIETARY INFORMATION

TITLE: CASE OUTLINE, SSOP, 24L

APPROVAL	DWG	REV	
	21-0002	0	1/1



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
b	0.014	0.026	0.36	0.66
b2	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	---	1.280	---	32.51
E	0.220	0.310	5.59	7.87
eA	0.300	BSC	7.62	BSC
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	0.005	---	0.13	---

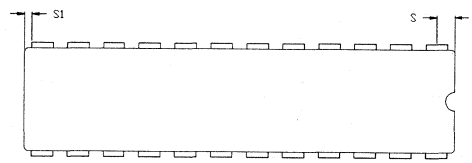


MEETS 1835 CASE "L"; D-9, CONFIGURATION #3

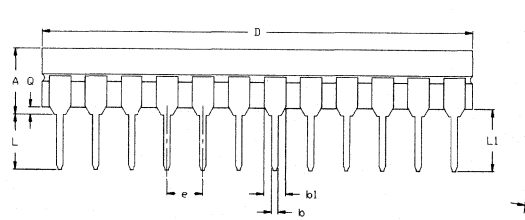
PROPRIETARY INFORMATION

TITLE: 24L (N) SIDEBRAZE OUTLINE

APPROVAL	DWG	REV
	21-0017	A



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
b	0.014	0.023	0.36	0.58
b1	0.038	0.065	0.97	1.65
c	0.008	0.015	0.20	0.38
D	---	1.280	---	32.51
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
L1	0.150	---	3.81	---
Q	0.015	0.060	0.38	1.52
S	---	0.098	---	2.49
S1	0.005	---	0.13	---
α	0°	15°	0°	15°

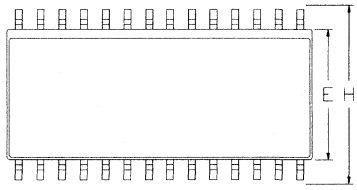


MEETS 38510 CASE "L"; D-9, CONFIGURATION #1

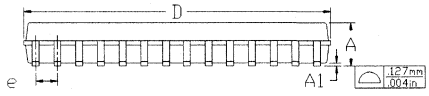
PROPRIETARY INFORMATION

TITLE: 24L (N) CERDIP OUTLINE

APPROVAL	DWG	REV
	21-340	B

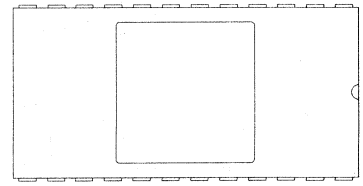


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.697	0.713	17.70	18.10
e	0.050	BSC	1.27	BSC
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

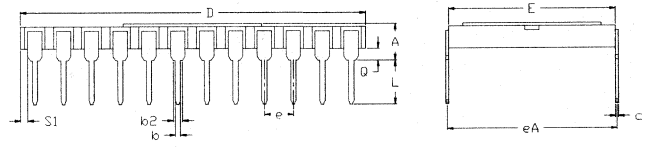


NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS-013 AE

MAXIM
PROPRIETARY INFORMATION
TITLE: 28L SOIC OUTLINE
APPROVAL | DWG: 21-343 | REV: A

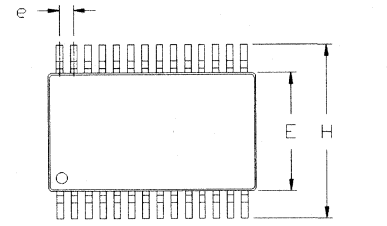


DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.225	---	5.72
b	0.014	0.026	0.36	0.66
b2	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	---	1.290	---	32.77
E	0.500	0.610	12.70	15.49
eA	0.600	BSC	15.24	BSC
e	0.100	BSC	2.54	BSC
L	0.120	0.200	3.05	5.08
Q	0.015	0.075	0.38	1.91
S1	0.005	---	0.13	---



MEETS 1835 CASE "J"; D-3, CONFIGURATION #3

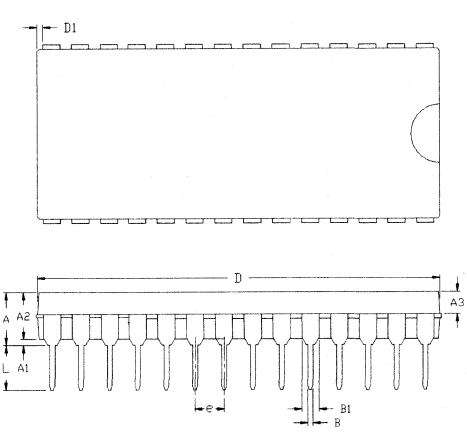
MAXIM
PROPRIETARY INFORMATION
TITLE: 24L SIDEBRAZE OUTLINE
APPROVAL | DWG: 21-0341 | REV: A



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
D	0.397	0.407	10.07	10.33
e	0.0256	BSC	0.65	BSC
E	0.205	0.212	5.20	5.38
H	0.301	0.311	7.65	7.9
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

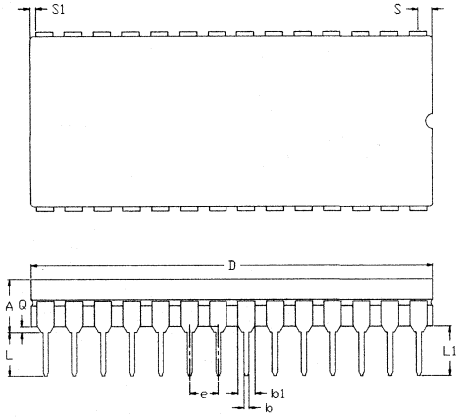
MAXIM
PROPRIETARY INFORMATION
TITLE: CASE OUTLINE, SSOP, 28L
APPROVAL | DWG: 21-0001 | REV: 0 | 1/1



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.055	1.14	1.65
C	0.008	0.012	0.20	0.30
D	1.430	1.470	36.32	37.34
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100	BSC	2.54	BSC
eA	0.600	BSC	15.24	BSC
eB	---	0.700	---	17.78
L	0.125	0.150	3.18	3.81
α	0°	15°	0°	15°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010"
2. CONTROLLING DIMENSION: INCH
3. SIMILIAR TO JEDEC MO-015 AL

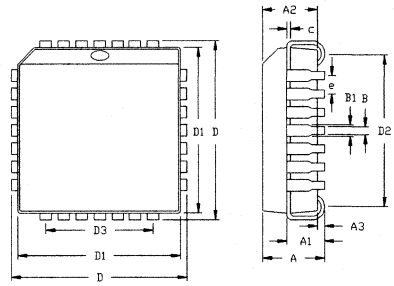
MAXIM
PROPRIETARY INFORMATION
TITLE: 28L PDIP OUTLINE
APPROVAL | DWG: 21-342 | REV: A



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.232	---	5.89
b	0.014	0.023	0.36	0.58
b1	0.038	0.065	0.97	1.65
c	0.008	0.015	0.20	0.38
D	---	1.490	---	37.85
E	0.500	0.610	12.70	15.49
E1	0.590	0.620	14.99	15.75
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
L1	0.150	---	3.81	---
Q	0.015	0.060	0.38	1.52
S	---	0.100	---	2.54
S1	0.005	---	0.13	---
α	0°	15°	0°	15°

MEETS 38510 D-10, CONFIGURATION #1

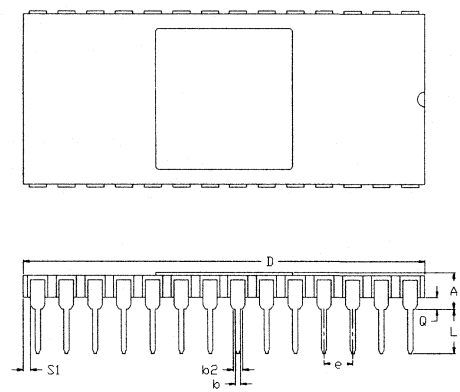
MAXIM
PROPRIETARY INFORMATION
TITLE: 28L CERDIP OUTLINE
APPROVAL | DWG 21-344 | REV B



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.165	0.180	4.19	4.57
A1	0.100	0.110	2.54	2.79
A2	0.145	0.156	3.68	3.96
A3	0.020	---	0.51	---
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
D	0.485	0.495	12.32	12.57
D1	0.450	0.455	11.43	11.56
D2	0.390	0.430	9.91	10.92
D3	0.300 REF		7.62 REF	
e	0.050 REF		1.27 REF	

NOTES:
1. DIMENSION D1 DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .20mm(.008") PER SIDE.
3. CONTROLLING DIMENSION: INCH
4. MEETS JEDEC MO-047AB.

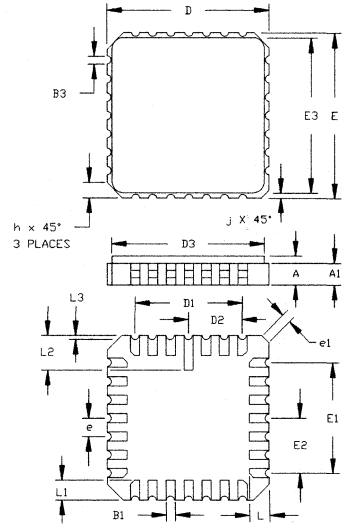
MAXIM
PROPRIETARY INFORMATION
TITLE: 28L PLCC PACKAGE OUTLINE
APPROVAL | DWG 21-346 | REV A | 1/1



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.232	---	5.89
b	0.014	0.026	0.36	0.66
b2	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	---	1.490	---	37.85
E	0.500	0.610	12.70	15.49
eA	0.600	BSC	15.24	BSC
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
Q	0.015	0.060	0.38	1.52
S1	---	---	---	---

MEETS 1835 D-10, CONFIGURATION #3

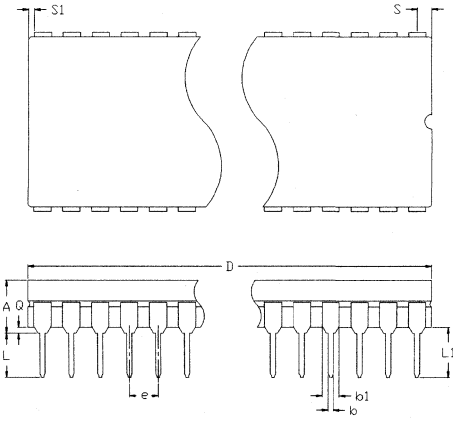
MAXIM
PROPRIETARY INFORMATION
TITLE: 28L SIZEBRAZE OUTLINE
APPROVAL | DWG 21-0345 | REV A



	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.060	0.100	1.52	2.54
A1	0.050	0.088	1.27	2.24
B1	0.022	0.028	0.56	0.71
B3	0.006	0.022	0.15	0.56
D/E	0.442	0.460	11.23	11.68
D1/E1	0.300 BSC		7.62 BSC	
D2/E2	0.150 BSC		3.81 BSC	
D3/E3	---	0.460	---	11.68
e	0.050 BSC		1.27 BSC	
e1	0.015	---	0.38	---
h	0.040 REF		1.02 REF	
j	0.020 REF		0.51 REF	
L	0.045	0.055	1.14	1.40
L1	0.045	0.055	1.14	1.40
L2	0.075	0.095	1.91	2.41
L3	0.003	0.015	0.08	0.38

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 38510 C-4

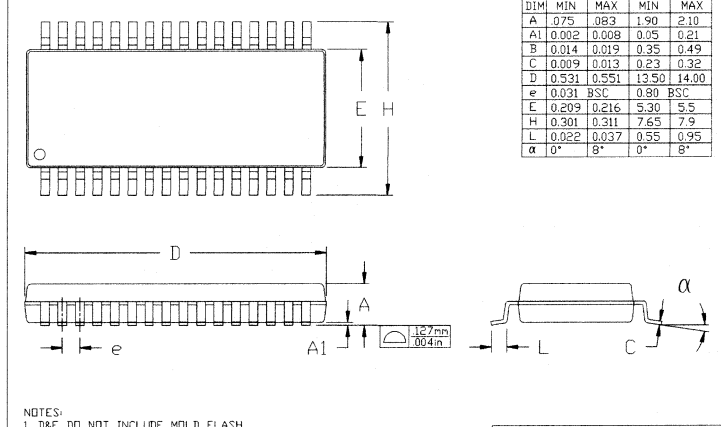
MAXIM
PROPRIETARY INFORMATION
TITLE: 28L LCC OUTLINE
APPROVAL | DWG 21-4497 | REV 0



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.225	---	5.72
b	0.014	0.023	0.36	0.58
b1	0.038	0.065	0.97	1.65
c	0.008	0.015	0.20	0.38
D	---	2.096	---	53.24
E	0.510	0.620	12.95	15.75
E1	0.590	0.630	14.99	16.00
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
L1	0.150	---	3.81	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---
α	0°	15°	0°	15°

MEETS 38510 CASE "Q", D-5, CONFIGURATION #1

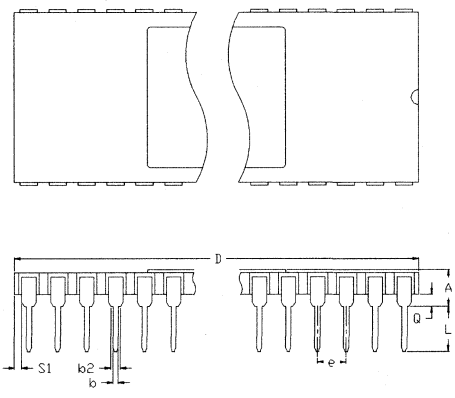
PROPRIETARY INFORMATION
TITLE: 40L CERDIP OUTLINE
APPROVAL | DWG 21-349 | REV B



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.075	.083	1.90	2.10
A1	0.002	0.008	0.05	0.21
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
D	0.531	0.551	13.50	14.00
e	0.031	BSC	0.80	BSC
E	0.209	0.216	5.30	5.5
H	0.301	0.311	7.65	7.9
L	0.022	0.037	0.55	0.95
α	0°	8°	0°	8°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER

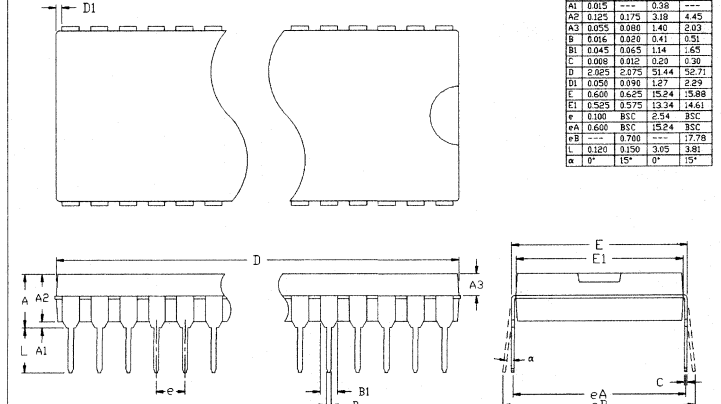
PROPRIETARY INFORMATION
TITLE: 32L SSOP OUTLINE
APPROVAL | DWG 21-0015 | REV A | 1/1



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.225	---	5.72
b	0.014	0.026	0.36	0.66
b2	0.045	0.065	1.14	1.65
c	0.008	0.018	0.20	0.46
D	---	2.096	---	53.24
E	0.510	0.620	12.95	15.75
eA	0.600	BSC	15.24	BSC
e	0.100	BSC	2.54	BSC
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	---	0.13	---

MEETS 1835 CASE "Q", D-5, CONFIGURATION #3

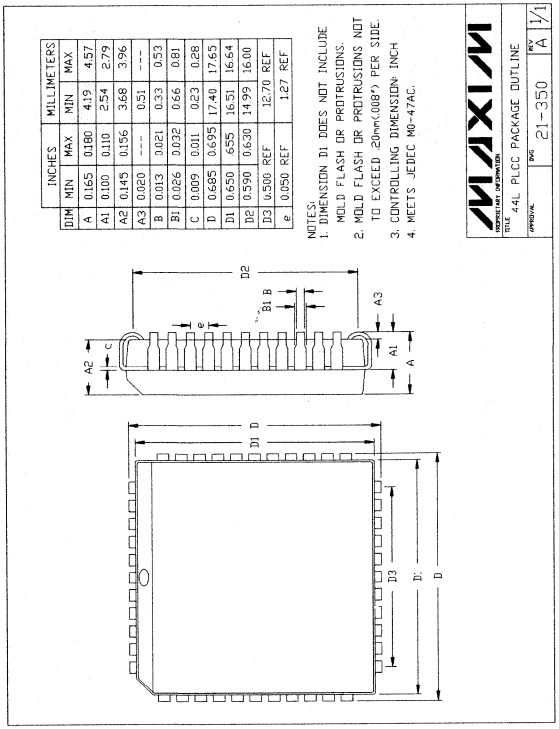
PROPRIETARY INFORMATION
TITLE: 40L SIDEBRAZE OUTLINE
APPROVAL | DWG 21-0018 | REV A



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.020	0.41	0.51
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D	2.025	2.075	51.44	52.71
D1	0.050	0.090	1.27	2.29
E	0.600	0.625	15.24	15.88
E1	0.525	0.575	13.34	14.61
e	0.100	BSC	2.54	BSC
eA	0.600	BSC	15.24	BSC
eB	---	0.700	---	17.78
L	0.120	0.150	3.05	3.81
α	0°	15°	0°	15°

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010"
2. CONTROLLING DIMENSION: INCH
3. SIMILAR TO JEDEC MO-015 AM

PROPRIETARY INFORMATION
TITLE: 40L PDIP OUTLINE
APPROVAL | DWG 21-348 | REV A



DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.165	0.180	4.19	4.57
A1	0.100	0.110	2.54	2.79
A2	0.145	0.156	3.68	3.96
A3	0.020	----	0.51	----
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
D	0.685	0.695	17.40	17.65
D1	0.650	655	16.51	16.64
D2	0.590	0.630	14.99	16.00
D3	0.500 REF		12.70 REF	
e	0.050 REF		1.27 REF	

NOTES:
1. DIMENSION D1 DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .20mm(.008") PER SIDE.
3. CONTROLLING DIMENSION: INCH
4. MEETS JEDEC MO-47AC.

MAXIM
PROPRIETARY INFORMATION
TITLE: 44L PLCC PACKAGE OUTLINE
APPROVAL | DWG: 21-350 | REV: A | 1/1

Edition Key:
93 NR Vol. II -1993 New Releases Data Book, Vol. II
92NR Vol. I -1992 New Releases Data Book, Vol. I
DS-Individual Data Sheet

Alpha Numeric Index

PART #	DS	1992 NR Vol I	93 NR Vol II
ADC0820	✔		
AM6012	✔		
BB3553	✔		
BB3554	✔		
DAC80	✔		
DAC8212	✔		
DG200A	✔		
DG201A	✔		
DG202	✔		
DG211	✔		
DG212	✔		
DG300A	✔		
DG301A	✔		
DG302A	✔		
DG303A	✔		
DG304A	✔		
DG305A	✔		
DG306A	✔		
DG307A	✔		
DG308	✔		
DG308A	✔		
DG309	✔		
DG381A	✔		
DG384A	✔		
DG387A	✔		
DG390A	✔		
DG401			✔*
DG403			✔*
DG405			✔*
DG406			✔*
DG407			✔*
DG408			✔*
DG409			✔*
DG411			✔
DG412			✔
DG413			✔
DG417			✔*
DG418			✔*
DG419			✔*
DG421			✔*
DG423			✔*
DG425			✔*
DG441			✔
DG442			✔
DG444			✔
DG445			✔

PART #	DS	1992 NR Vol I	93 NR Vol II
DG506	✔		
DG506A	✔		
DG507	✔		
DG507A	✔		
DG508A	✔		
DG509A	✔		
DG526	✔		
DG527	✔		
DG528	✔		
DG529	✔		
DGM181	✔		
DGM182	✔		
EL2004	✔		
EL2005	✔		
HI-201	✔		
HI-201HS	✔		
HI-508	✔		
HI-508A		✔	
HI-509	✔		
HI-509A		✔	
HI-674	✔		
ICL7106	✔		
ICL7107	✔		
ICL7109	✔		
ICL7116	✔		
ICL7117	✔		
ICL7126	✔		
ICL7129A	✔		
ICL7135	✔		
ICL7136	✔		
ICL7137	✔		
ICL7611	✔		
ICL7612	✔		
ICL7614	✔		
ICL7616	✔		
ICL7621	✔		
ICL7622	✔		
ICL7631	✔		
ICL7632	✔		
ICL7641	✔		
ICL7642	✔		
ICL7650B	✔		
ICL7652B	✔		
ICL7660			✔*
ICL7662	✔		
ICL7663	✔		

* Advance Information

Edition Key:
93 NR Vol. II -1993 New Releases Data Book, Vol. II
92NR Vol. I -1992 New Releases Data Book, Vol. I
DS-Individual Data Sheet

Alpha Numeric Index

PART #	DS	1992 NR Vol I	93 NR Vol II
ICL7664	✔		
ICL7665	✔		
ICL7667	✔		
ICL8069	✔		
ICM7211	✔		
ICM7211A	✔		
ICM7211AM	✔		
ICM7211M	✔		
ICM7212	✔		
ICM7212A	✔		
ICM7212AM	✔		
ICM7212M	✔		
ICM7217	✔		
ICM7218	✔		
ICM7224	✔		
ICM7225	✔		
ICM7228	✔		
ICM7240	✔		
ICM7242	✔		
ICM7250	✔		
ICM7260	✔		
ICM7555	✔		
ICM7556	✔		
IH5040	✔		
IH5041	✔		
IH5042	✔		
IH5043	✔		
IH5044	✔		
IH5045	✔		
IH5047	✔		
IH5047A	✔		
IH5048	✔		
IH5048A	✔		
IH5049	✔		
IH5050	✔		
IH5051	✔		
IH5108	✔		
IH5140	✔		
IH5141	✔		
IH5142	✔		
IH5143	✔		
IH5144	✔		
IH5145	✔		
IH5148	✔		
IH5208	✔		
IH5341	✔		
IH5352	✔		
IH6108	✔		
IH6116	✔		
IH6208	✔		
IH6216	✔		
LH0033A	✔		
LH0063	✔		
LH0101	✔		
LT1001	✔		
LT1019	✔		
LT1021	✔		
LT1028	✔		
LT1031	✔		
LTC1062		✔	
MAX038			✔*
MAX1000	✔		
MAX1025	✔		
MAX1044			✔*
MAX1074	✔		
MAX120			✔*
MAX120EVKit	✔		
MAX121			✔*
MAX122			✔*
MAX123	✔		
MAX1232		✔	
MAX1259		✔	
MAX1260	✔		
MAX130	✔		
MAX130A	✔		
MAX131	✔		
MAX131A	✔		
MAX132			✔
MAX132EVKit	✔		
MAX133	✔		
MAX134	✔		
MAX135			✔
MAX136	✔		
MAX138	✔		
MAX139	✔		
MAX140	✔		
MAX141	✔		
MAX142	✔		
MAX143	✔		
MAX150	✔		
MAX151		✔	
MAX152	✔		

* Advance Information

Edition Key:
93 NR Vol. II -1993 New Releases Data Book, Vol. II
92NR Vol. I -1992 New Releases Data Book, Vol. I
DS-Individual Data Sheet

Alpha Numeric Index

PART #	DS	1992 NR Vol I	93 NR Vol II
MAX153			✔*
MAX154	✔		
MAX155			✔
MAX155EVKit	✔		
MAX156			✔
MAX158	✔		
MAX160	✔		
MAX161	✔		
MAX162		✔	
MAX163		✔	
MAX164		✔	
MAX165			✔
MAX166			✔
MAX167		✔	
MAX168			✔*
MAX170	✔		
MAX171		✔	
MAX172		✔	
MAX173	✔		
MAX174		✔	
MAX1743	✔		
MAX176			✔*
MAX176EVKit	✔		
MAX177	✔		
MAX178		✔	
MAX179	✔		
MAX180		✔	
MAX180EVKit	✔		
MAX181		✔	
MAX182		✔	
MAX183		✔	
MAX184		✔	
MAX185		✔	
MAX186			✔*
MAX187	✔*		
MAX188			✔*
MAX190			✔
MAX190EVKit	✔		
MAX191			✔*
MAX195			✔*
MAX200			✔*
MAX201	✔		
MAX202			✔*
MAX203			✔*
MAX204			✔*
MAX205			✔*

PART #	DS	1992 NR Vol I	93 NR Vol II
MAX206			✔*
MAX207			✔*
MAX208			✔*
MAX210			✔*
MAX211			✔*
MAX220		✔	✔
MAX222		✔	✔
MAX223			✔
MAX230		✔	✔
MAX230/234	✔		
MAX231		✔	✔
MAX232		✔	✔
MAX232A		✔	✔
MAX233		✔	✔
MAX233A		✔	✔
MAX234		✔	✔
MAX235		✔	✔
MAX236		✔	✔
MAX237		✔	✔
MAX238		✔	✔
MAX239		✔	✔
MAX240		✔	✔
MAX241		✔	✔
MAX242		✔	✔
MAX243		✔	✔
MAX244		✔	✔
MAX245		✔	✔
MAX246		✔	✔
MAX247		✔	✔
MAX248		✔	✔
MAX249		✔	✔
MAX250		✔	
MAX251		✔	
MAX252		✔	
MAX260		✔	
MAX261		✔	
MAX262		✔	
MAX263		✔	
MAX264		✔	
MAX265		✔	
MAX266		✔	
MAX267		✔	
MAX268		✔	
MAX270		✔	
MAX271		✔	
MAX274			✔

* Advance Information

Edition Key:
93 NR Vol. II -1993 New Releases Data Book, Vol. II
92NR Vol. I -1992 New Releases Data Book, Vol. I
DS-Individual Data Sheet

Alpha Numeric Index

PART #	DS	1992 NR Vol I	93 NR Vol II
MAX274EVKit	✔		✔
MAX274/5Soft	✔		✔
MAX275			✔
MAX280		✔	
MAX281		✔	
MAX282	✔		
MAX283	✔		
MAX284	✔		
MAX290	✔		
MAX291			✔
MAX292			✔
MAX293			✔
MAX294			✔
MAX295			✔
MAX296			✔
MAX297			✔
MAX310		✔	
MAX311		✔	
MAX312	✔		
MAX313	✔		
MAX319	✔		
MAX320	✔		
MAX3211	✔		
MAX322	✔		
MAX323	✔		
MAX324	✔		
MAX325	✔		
MAX326		✔	
MAX327		✔	
MAX328		✔	
MAX329		✔	
MAX331	✔		
MAX332	✔		
MAX333	✔		
MAX334	✔		
MAX341	✔		
MAX343	✔		
MAX345	✔		
MAX348	✔		
MAX358		✔	
MAX359		✔	
MAX368		✔	
MAX369		✔	
MAX378		✔	
MAX379		✔	
MAX380	✔		

PART #	DS	1992 NR Vol I	93 NR Vol II
MAX381	✔		
MAX382	✔		
MAX383	✔		
MAX388			✔
MAX389			✔
MAX390	✔		
MAX391	✔		
MAX392	✔		
MAX400	✔		
MAX401	✔		
MAX402		✔	
MAX403		✔	
MAX404	✔		
MAX405		✔	
MAX406			✔
MAX407			✔
MAX408	✔		
MAX409	✔*		
MAX410			✔*
MAX412			✔
MAX414			✔*
MAX4193		✔	
MAX420	✔		
MAX421	✔		
MAX422	✔		
MAX423	✔		
MAX424	✔		
MAX425		✔	
MAX426		✔	
MAX427	✔		
MAX428	✔		
MAX429	✔		
MAX430	✔		
MAX431	✔		
MAX432	✔		
MAX435			✔*
MAX436			✔*
MAX438			✔*
MAX439			✔*
MAX4391		✔	
MAX440			✔
MAX441			✔
MAX442			✔
MAX4426	✔		
MAX4427	✔		
MAX4428	✔		

* Advance Information

Edition Key:
93 NR Vol. II -1993 New Releases Data Book, Vol. II
92NR Vol. I -1992 New Releases Data Book, Vol. I
DS-Individual Data Sheet

Alpha Numeric Index

PART #	DS	1992 NR Vol I	93 NR Vol II
MAX448	✔		
MAX450	✔		
MAX451	✔		
MAX452		✔	
MAX453		✔	
MAX454		✔	
MAX455		✔	
MAX456			✔
MAX457		✔	
MAX460	✔		
MAX480		✔	
MAX482	✔		
MAX484	✔		
MAX485	✔		
MAX486	✔		
MAX492	✔		
MAX494	✔		
MAX500		✔	
MAX501			✔
MAX502			✔
MAX505			✔
MAX506			✔
MAX507			✔
MAX508			✔
MAX512	✔		
MAX514			✔
MAX516			✔
MAX526			✔
MAX527			✔
MAX528			✔
MAX529			✔
MAX530	✔		
MAX531	✔		
MAX532			✔*
MAX543		✔	
MAX550	✔		
MAX560			✔
MAX561			✔
MAX600	✔		
MAX601	✔		
MAX602	✔		
MAX610	✔		
MAX611	✔		
MAX612	✔		
MAX615	✔		
MAX616	✔		

PART #	DS	1992 NR Vol I	93 NR Vol II
MAX617	✔		
MAX620		✔	
MAX621		✔	
MAX622		✔	
MAX623		✔	
MAX625			✔
MAX626	✔		
MAX627	✔		
MAX628	✔		
MAX630/4193		✔	
MAX631		✔	
MAX632		✔	
MAX633		✔	
MAX634/4391		✔	
MAX635		✔	
MAX636		✔	
MAX637		✔	
MAX638		✔	
MAX639			✔
MAX639EVKit	✔		
MAX641		✔	
MAX642		✔	
MAX643		✔	
MAX644	✔		
MAX645	✔		
MAX646	✔		
MAX647	✔		
MAX648	✔		
MAX649	✔		
MAX650	✔		
MAX651	✔		
MAX654		✔	
MAX655		✔	
MAX656		✔	
MAX657		✔	
MAX658		✔	
MAX659	✔		
MAX660		✔	
MAX661			✔*
MAX662	✔		
MAX663		✔	
MAX664		✔	
MAX665			✔
MAX666		✔	
MAX667		✔	
MAX670	✔		

* Advance Information

Edition Key:
93 NR Vol. II -1993 New Releases Data Book, Vol. II
92NR Vol. I -1992 New Releases Data Book, Vol. I
DS-Individual Data Sheet

Alpha Numeric Index

PART #	DS	1992 NR Vol I	93 NR Vol II
MAX671	✔		
MAX672	✔		
MAX673	✔		
MAX674	✔		
MAX675	✔		
MAX676	✔		
MAX677	✔		
MAX678	✔		
MAX680		✔	
MAX681		✔	
MAX681B	✔		
MAX690		✔	
MAX690A			✔
MAX691		✔	
MAX691A			✔*
MAX692		✔	
MAX692A			✔
MAX693		✔	
MAX693A			✔*
MAX694		✔	
MAX695		✔	
MAX696		✔	
MAX697		✔	
MAX698		✔	
MAX699		✔	
MAX700		✔	
MAX701		✔	
MAX702		✔	
MAX703			✔*
MAX704			✔*
MAX705			✔
MAX706			✔
MAX707			✔
MAX708			✔
MAX712			✔*
MAX7129	✔		
MAX713			✔*
MAX714			✔
MAX715			✔
MAX716			✔
MAX716EVKit	✔		
MAX717			✔*
MAX718			✔*
MAX718EVKit	✔		
MAX719			✔*
MAX720			✔*

PART #	DS	1992 NR Vol I	93 NR Vol II
MAX721			✔*
MAX7217	✔		
MAX7219		✔	
MAX722			✔
MAX722EVKit			✔
MAX7220	✔		
MAX723			✔
MAX7231/A/B/C/D	✔		
MAX7232/A/B/C/D	✔		
MAX7233/A/B	✔		
MAX7234/A/B	✔		
MAX724			✔*
MAX726			✔*
MAX727			✔*
MAX728			✔*
MAX729			✔*
MAX730			✔
MAX731			✔
MAX731EVKit	✔		
MAX732			✔
MAX732EVKit	✔		✔
MAX733			✔
MAX734			✔*
MAX735			✔
MAX735EVKit	✔		
MAX736			✔
MAX736EVKit	✔		
MAX737			✔
MAX738			✔
MAX738EVKit	✔		
MAX739			✔
MAX739EVKit	✔		
MAX740	✔		
MAX741			✔*
MAX742		✔	
MAX743		✔	
MAX743EVKit	✔		
MAX744	✔		
MAX750			✔
MAX751			✔*
MAX752			✔
MAX752EVKit	✔		✔
MAX755			✔*
MAX758			✔
MAX758EVKit	✔		
MAX759			✔

* Advance Information

Edition Key:
93 NR Vol. II -1993 New Releases Data Book, Vol. II
92NR Vol. I -1992 New Releases Data Book, Vol. I
DS-Individual Data Sheet

Alpha Numeric Index

PART #	DS	1992 NR Vol I	93 NR Vol II
MAX760	✔		
MAX761	✔		
MAX762	✔		
MAX7624	✔		
MAX764	✔		
MAX7645	✔		
MAX765	✔		
MAX766	✔		
MAX770	✔		
MAX771	✔		
MAX772	✔		
MAX773	✔		
MAX774	✔		
MAX775	✔		
MAX776	✔		
MAX7821	✔		
MAX790		✔	
MAX791			✔*
MAX8211	✔		
MAX8212	✔		
MAX872			✔
MAX873			✔*
MAX874			✔*
MAX900		✔	
MAX901		✔	
MAX902		✔	
MAX903		✔	
MAX905			✔
MAX906			✔
MAX907			✔*
MAX910			✔
MAX911			✔
MAX912	✔		
MAX913	✔		
MAX9685	✔		
MAX9686	✔		
MAX9687	✔		
MAX9690	✔		
MAX9698	✔		
MAXC001		✔	
MAXL001		✔	
MF10	✔		
MM74C945	✔		
MM74C947	✔		
MX2700	✔		
MX2701	✔		

PART #	DS	1992 NR Vol I	93 NR Vol II
MX2710	✔		
MX390	✔		
MX3554	✔		
MX536A	✔		
MX565A	✔		
MX566A	✔		
MX574	✔		
MX574A		✔	
MX578	✔		
MX580	✔		
MX581	✔		
MX584	✔		
MX586	✔		
MX587	✔		
MX588	✔		
MX590	✔		
MX592	✔		
MX594	✔		
MX595	✔		
MX596	✔		
MX597	✔		
MX636	✔		
MX650	✔		
MX667	✔		
MX674A		✔	
MX767	✔		
MX7224	✔		
MX7225	✔		
MX7226	✔		
MX7228	✔		
MX7245	✔		
MX7248	✔		
MX7501	✔		
MX7502	✔		
MX7503	✔		
MX7506	✔		
MX7507	✔		
MX7510	✔		
MX7511	✔		
MX7512	✔		
MX7520	✔		
MX7521	✔		
MX7523	✔		
MX7524	✔		
MX7528	✔		
MX7530	✔		

* Advance Information

Edition Key:
93 NR Vol. II -1993 New Releases Data Book, Vol. II
92NR Vol. I -1992 New Releases Data Book, Vol. I
DS-Individual Data Sheet

Alpha Numeric Index

PART #	DS	1992 NR Vol I	93 NR Vol II
MX7531	✔		
MX7533	✔		
MX7534	✔		
MX7535	✔		
MX7536	✔		
MX7537	✔		
MX7538	✔		
MX7541	✔		
MX7541A	✔		
MX7542	✔		
MX7543	✔		
MX7545	✔		
MX7545A	✔		
MX7547	✔		
MX7548	✔		
MX7549	✔		
MX7569	✔		
MX7572		✔	
MX7574	✔		
MX7575	✔		
MX7576	✔		
MX7578	✔		
MX7581	✔		
MX7582	✔		
MX7628	✔		
MX7672	✔		
MX7820	✔		
MX7821		✔	
MX7824	✔		
MX7828	✔		
MX7837	✔		
MX7845	✔		
MX7846	✔		
MX7847	✔		
MX9500	✔		
OP07	✔		
OP27	✔		
OP37	✔		
OP90	✔		
OP290	✔		
OP490	✔		
PGA100	✔		
REF01	✔		
REF02	✔		
Si7661	✔		
TSC426	✔		
TSC427	✔		
TSC428	✔		
TSC800	✔		
VFC32	✔		

* Advance Information